

MEMORY Mobile FCRAM™

CMOS

16 Mbit (1 M word × 16 bit)
Mobile Phone Application Specific Memory

MB82DS01181E-70L-A

■ DESCRIPTION

MB82DS01181E is a Fast Cycle Random Access Memory (FCRAM) with asynchronous Static Random Access Memory (SRAM) interface containing 16,777,216 storages accessible in a 16-bit format. MB82DS01181E is suited for mobile applications such as Cellular Handset and PDA.

Note: FCRAM is a trademark of Fujitsu Limited, Japan.

■ FEATURES

- Asynchronous SRAM Interface
- 1 M word × 16-bit Organization
- Low-voltage Operating Conditions : $V_{DD} = +1.7 \text{ V to } +1.95 \text{ V}$
- Wide Operating Temperature : $T_A = -30 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$
- Read/Write Cycle Time : $t_{RC} = t_{WC} = 80 \text{ ns Min}$
- Fast Random Access Time : $t_{AA} = t_{CE} = 70 \text{ ns Max}$
- Active current : $I_{DDA1} = 20 \text{ mA Max}$
- Standby current : $I_{DD S1} = 100 \text{ } \mu\text{A Max}$
- Power down current : $I_{DDPS} = 10 \text{ } \mu\text{A Max}$
- Byte Control
- Shipping Form : Wafer / Chip

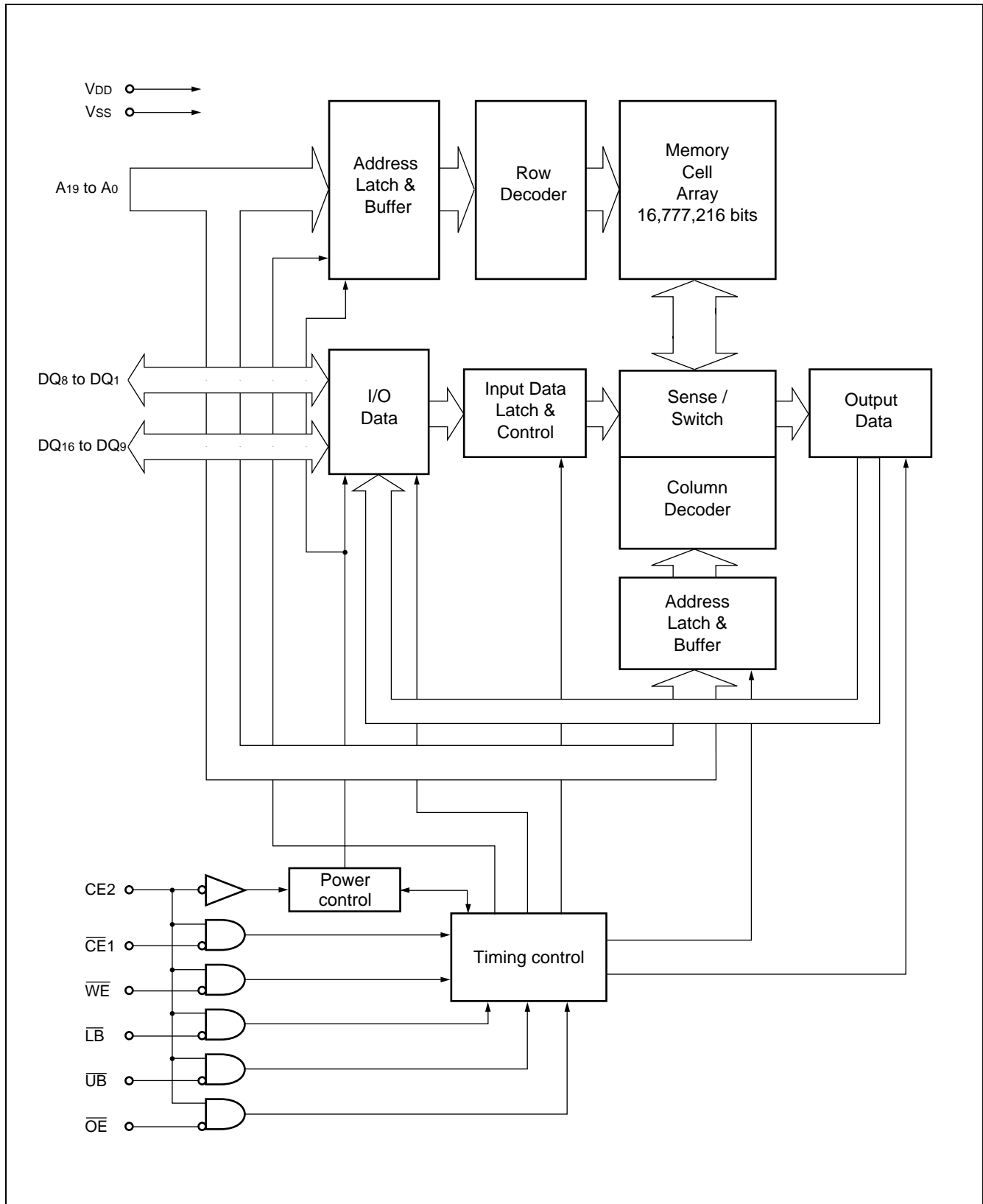
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■ PIN DESCRIPTION

Pin Name	Description
A ₁₉ to A ₀	Address Input
$\overline{\text{CE}}1$	Chip Enable 1 (Low Active)
CE2	Chip Enable 2 (High Active)
$\overline{\text{WE}}$	Write Enable (Low Active)
$\overline{\text{OE}}$	Output Enable (Low Active)
$\overline{\text{LB}}$	Lower Byte Control (Low Active)
$\overline{\text{UB}}$	Upper Byte Control (Low Active)
DQ ₈ to DQ ₁	Lower Byte Data Input/Output
DQ ₁₆ to DQ ₉	Upper Byte Data Input/Output
V _{DD}	Power Supply
V _{SS}	Ground

■ BLOCK DIAGRAM



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■ FUNCTION TRUTH TABLE

Mode	CE2	$\overline{CE}1$	\overline{WE}	\overline{OE}	\overline{LB}	\overline{UB}	A ₁₉ to A ₀	DQ ₈ to DQ ₁	DQ ₁₆ to DQ ₉	I _{DD}	Data Retention
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z	I _{DDs}	Yes
Output Disable* ¹		L	H	H	X	X	*3	High-Z	High-Z	I _{DDA}	
No Read			H	L	H	H	Valid	High-Z	High-Z		
Read (Upper Byte)					H	L	Valid	High-Z	Output Valid		
Read (Lower Byte)					L	H	Valid	Output Valid	High-Z		
Read (Word)					L	L	Valid	Output Valid	Output Valid		
No Write			L	H	H	H	Valid	Invalid	Invalid		
Write (Upper Byte)					H	L	Valid	Invalid	Input Valid		
Write (Lower Byte)					L	H	Valid	Input Valid	Invalid		
Write (Word)					L	L	Valid	Input Valid	Input Valid		
Power Down * ²			L	X	X	X	X	X	X		

Note : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High impedance

*1 : Should not be kept this logic condition longer than 1 μ s.

*2 : Power down mode can be entered from standby state and all DQ pins are in High-Z state.

*3 : Can be either V_{IL} or V_{IH} but must be valid before read or write.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply Voltage*	V_{DD}	-0.5	+3.6	V
Input Voltage*	V_{IN}	-0.5	+3.6	V
Output voltage*	V_{OUT}	-0.5	+3.6	V
Short Circuit Output Current	I_{OUT}	-50	+50	mA
Storage Temperature	T_{STG}	-55	+125	°C

* : All voltages are referenced to $V_{SS} = 0$ V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Supply Voltage *1	V_{DD}	1.7	1.95	V
	V_{SS}	0	0	V
High Level Input Voltage *1, *2	V_{IH}	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Low Level Input Voltage *1, *3	V_{IL}	-0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	T_A	-30	+ 85	°C

*1 : All voltages are referenced to $V_{SS} = 0$ V.

*2 : Overshoot spec. ($V_{IH (Max)} = V_{DD} + 1.0$ V, pulse width ≤ 5.0 ns)

*3 : Undershoot spec. ($V_{IL (Min)} = -1.0$ V, pulse width ≤ 5.0 ns)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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■ PIN CAPACITANCE

(f = 1.0 MHz, T_A = +25 °C)

Parameter	Pin name	Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Input Capacitance	A ₁₉ to A ₀	C _{IN1}	V _{IN} = 0 V	—	—	5	pF
	$\overline{\text{CE1}}$, CE2, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$	C _{IN2}	V _{IN} = 0 V	—	—	5	pF
Input/Output Capacitance	DQ ₁₆ to DQ ₁	C _{IO}	V _{IO} = 0 V	—	—	8	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Conditions		Value		Unit
				Min	Max	
Input Leakage Current	I _{LI}	V _{SS} ≤ V _{IN} ≤ V _{DD}		−1.0	+1.0	μA
Output Leakage Current	I _{LO}	V _{SS} ≤ V _{OUT} ≤ V _{DD} , Output High impedance		−1.0	+1.0	μA
Output High Voltage Level	V _{OH}	V _{DD} = V _{DD} Min, I _{OH} = −0.5 mA		1.4	—	V
Output Low Voltage Level	V _{OL}	I _{OL} = 1 mA		—	0.4	V
V _{DD} Power Down Current	I _{DDPS}	V _{DD} = V _{DD} Max, V _{IN} = V _{IH} or V _{IL} , CE2 ≤ 0.2 V		—	10	μA
V _{DD} Standby Current	I _{DDS}	V _{DD} = V _{DD} Max, V _{IN} = V _{IH} or V _{IL} , CE1 = CE2 = V _{IH}		—	1	mA
	I _{DDS1}	V _{DD} = V _{DD} Max, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{DD} − 0.2 V, CE1 = CE2 ≥ V _{DD} − 0.2 V		—	100	μA
V _{DD} Active Current	I _{DDA1}	V _{DD} = V _{DD} Max, V _{IN} = V _{IH} or V _{IL} , CE1 = V _{IL} and CE2 = V _{IH} , I _{OUT} = 0 mA	t _{RC} / t _{WC} = Min	—	20	mA
	I _{DDA2}		t _{RC} / t _{WC} = 1 μs	—	3.0	

Notes: • All voltages are referenced to V_{SS} = 0 V.

- DC Characteristics are measured after following POWER-UP timing.
- I_{OUT} depends on the output load conditions.

2. AC Characteristics

(1) Read Operation

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	t_{RC}	80	1000	ns	*1, *2
$\overline{CE}1$ Access Time	t_{CE}	—	70	ns	*3
\overline{OE} Access Time	t_{OE}	—	45	ns	*3
Address Access Time	t_{AA}	—	70	ns	*3, *5
\overline{LB} , \overline{UB} Access Time	t_{BA}	—	30	ns	*3
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}1$ Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
\overline{OE} Low to Output Low-Z	t_{OLZ}	0	—	ns	*4
\overline{LB} , \overline{UB} Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}1$ High to Output High-Z	t_{CHZ}	—	20	ns	*3
\overline{OE} High to Output High-Z	t_{OHZ}	—	20	ns	*3
\overline{LB} , \overline{UB} High to Output High-Z	t_{BHZ}	—	20	ns	*3
Address Setup Time to $\overline{CE}1$ Low	t_{ASC}	-5	—	ns	
Address Setup Time to \overline{OE} Low	t_{ASO}	10	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5
Address Hold Time from $\overline{CE}1$ High	t_{CHAH}	-5	—	ns	*6
Address Hold Time from \overline{OE} High	t_{OHAH}	-5	—	ns	
\overline{WE} High to \overline{OE} Low Time for Read	t_{WHOL}	15	1000	ns	*7
$\overline{CE}1$ High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE}1$ is kept at Low without any address change.

*2 : Address should not be changed within minimum t_{RC} .

*3 : The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*4 : The output load 5 pF without any other load.

*5 : Applicable when $\overline{CE}1$ is kept at Low.

*6 : t_{RC} (Min) must be satisfied.

*7 : If the actual value of t_{WHOL} is shorter than specified minimum value, the actual t_{AA} of following Read may become longer by the amount of subtracting actual value from specified minimum value.

Note : AC characteristics are measured after following power-up timing.

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(2) Write Operation

(At recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	t_{WC}	80	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*2
$\overline{CE1}$ Write Pulse Width	t_{CW}	45	—	ns	*3
\overline{WE} Write Pulse Width	t_{WP}	45	—	ns	*3
\overline{LB} , \overline{UB} Write Pulse Width	t_{BW}	45	—	ns	*3
\overline{LB} , \overline{UB} Byte Mask Setup Time	t_{BS}	−5	—	ns	*4
\overline{LB} , \overline{UB} Byte Mask Hold Time	t_{BH}	−5	—	ns	*5
Write Recovery Time	t_{WR}	0	—	ns	*6
$\overline{CE1}$ High Pulse Width	t_{CP}	15	—	ns	
\overline{WE} High Pulse Width	t_{WHP}	15	1000	ns	
\overline{LB} , \overline{UB} High Pulse Width	t_{BHP}	15	1000	ns	
Data Setup Time	t_{DS}	20	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
\overline{OE} High to $\overline{CE1}$ Low Setup Time for Write	t_{OHCL}	−5	—	ns	*7
\overline{OE} High to Address Setup Time for Write	t_{OES}	0	—	ns	*8
\overline{LB} and \overline{UB} Write Pulse Overlap	t_{BWO}	20	—	ns	

*1 : Maximum value is applicable if $\overline{CE1}$ is kept at Low without any address change.

*2 : Minimum value must be equal or greater than the sum of write pulse width (t_{CW} , t_{WP} or t_{BW}) and write recovery time (t_{WR}) .

*3 : Write pulse width is defined from High to Low transition of $\overline{CE1}$, \overline{WE} , \overline{LB} or \overline{UB} , whichever occurs last.

*4 : Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of $\overline{CE1}$ or \overline{WE} whichever occurs last.

*5 : Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of $\overline{CE1}$ or \overline{WE} whichever occurs first.

*6 : Write recovery time is defined from Low to High transition of $\overline{CE1}$, \overline{WE} , \overline{LB} or \overline{UB} , whichever occurs first.

*7 : If \overline{OE} is Low after minimum t_{OHCL} , read cycle is initiated. In other words, \overline{OE} must be brought to High within 5 ns after $\overline{CE1}$ is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

*8 : If \overline{OE} is Low after new address input, read cycle is initiated. In other words, \overline{OE} must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

Note : AC Characteristics are measured after following POWER-UP timing.

(At recommended operating conditions unless otherwise noted.)

* : Applicable also to power-up.

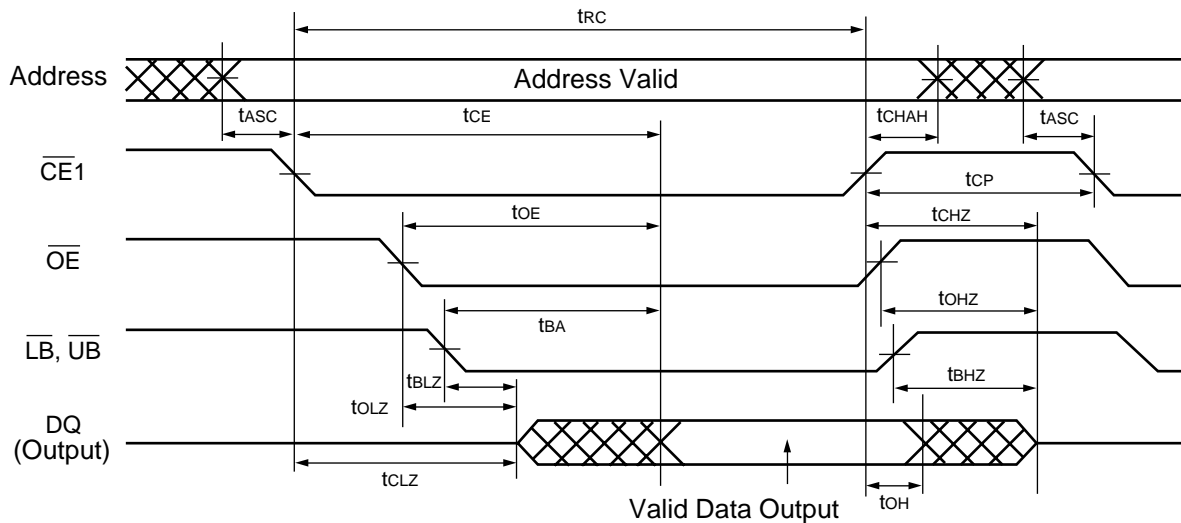
(At recommended operating conditions unless otherwise noted.)

*2: The Input Transition Time (t_r) at AC testing is 5 ns as shown in below. If actual t_r is longer than 5 ns, it may violate AC specifications of some timing parameters.

The diagram shows a 'Device Under Test' (DUT) block. The input of the DUT is connected to a voltage divider. The voltage divider consists of a $50\ \Omega$ resistor connected to $V_{DD} \times 0.5\text{ V}$ and a 50 pF capacitor connected to ground. The output of the DUT is connected to a $0.1\ \mu\text{F}$ capacitor, which is then connected to V_{DD} and V_{SS} .

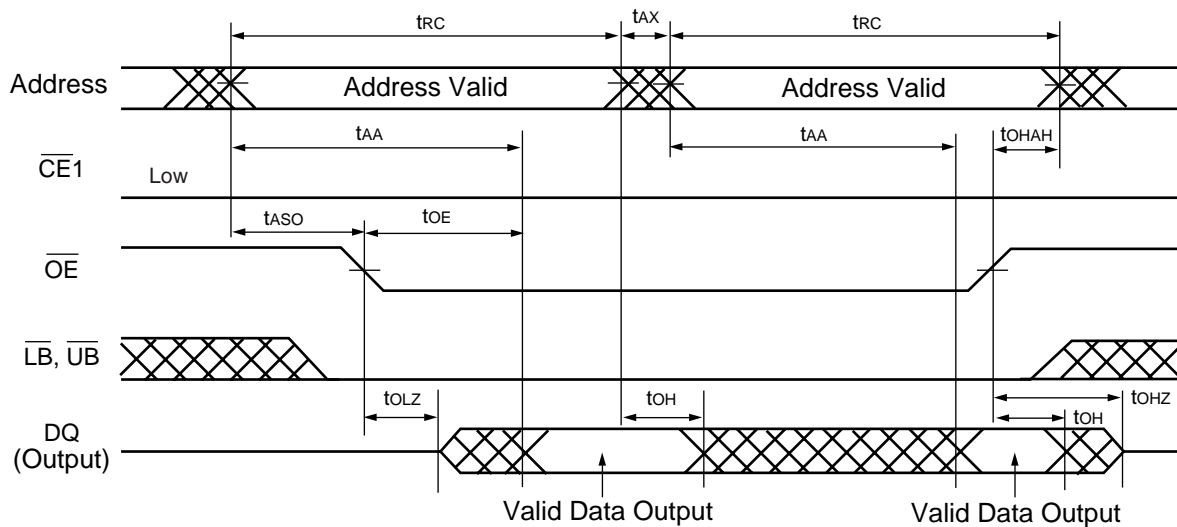
■ TIMING DIAGRAM

1. READ Timing 1 (Basic Timing)



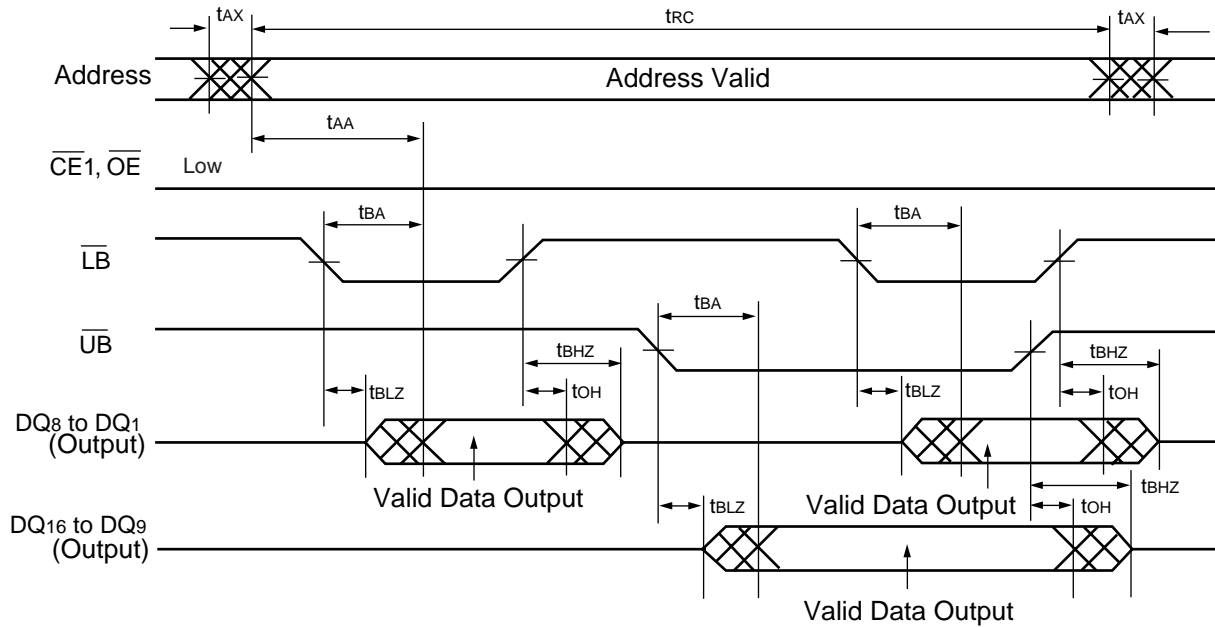
Note : This timing diagram assumes $CE2 = "H"$ and $\overline{WE} = "H"$.

2. READ Timing 2 (\overline{OE} & Address Access)



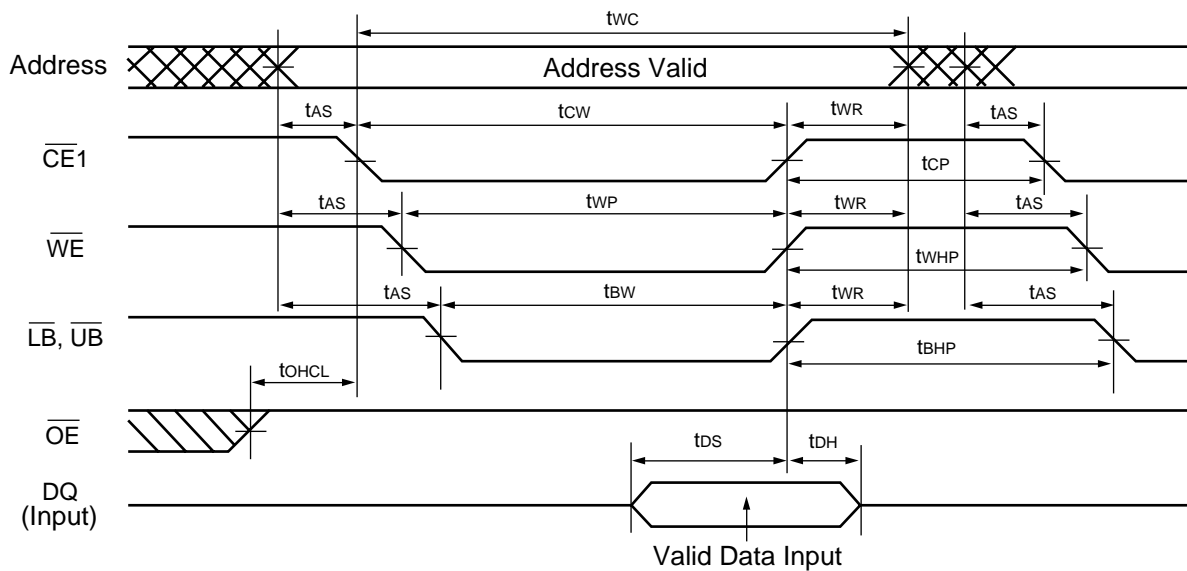
Note : This timing diagram assumes $CE2 = "H"$ and $\overline{WE} = "H"$.

3. READ Timing 3 ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Access)



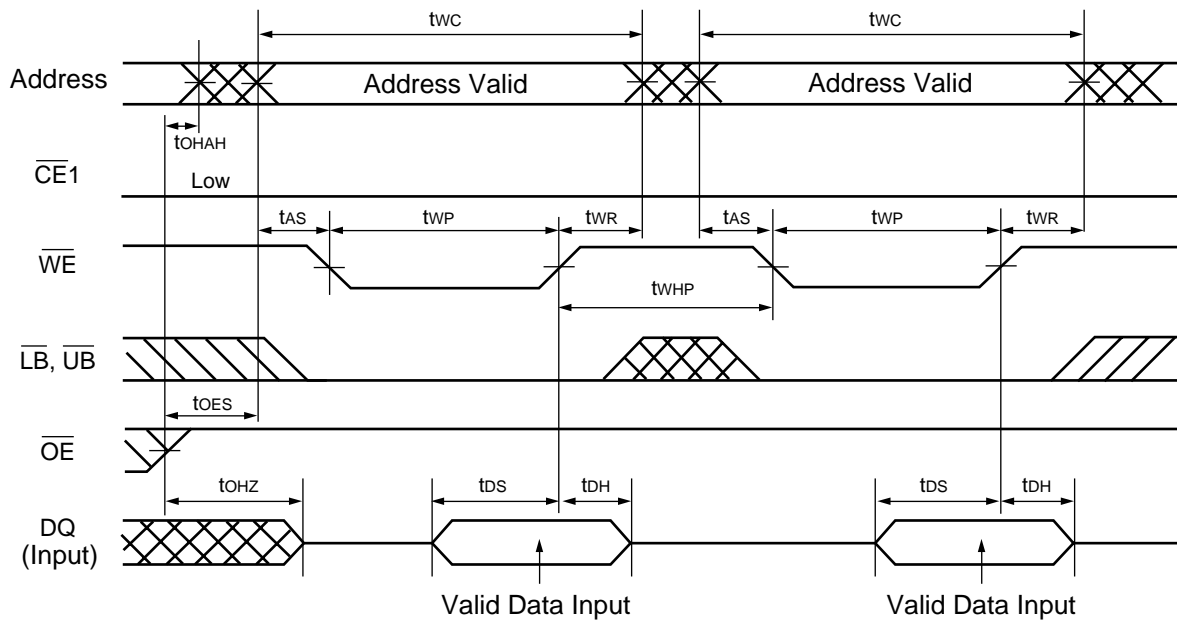
Note : This timing diagram assumes $\text{CE2} = \text{"H"}$ and $\overline{\text{WE}} = \text{"H"}$.

4. WRITE Timing 1 (Basic Timing)



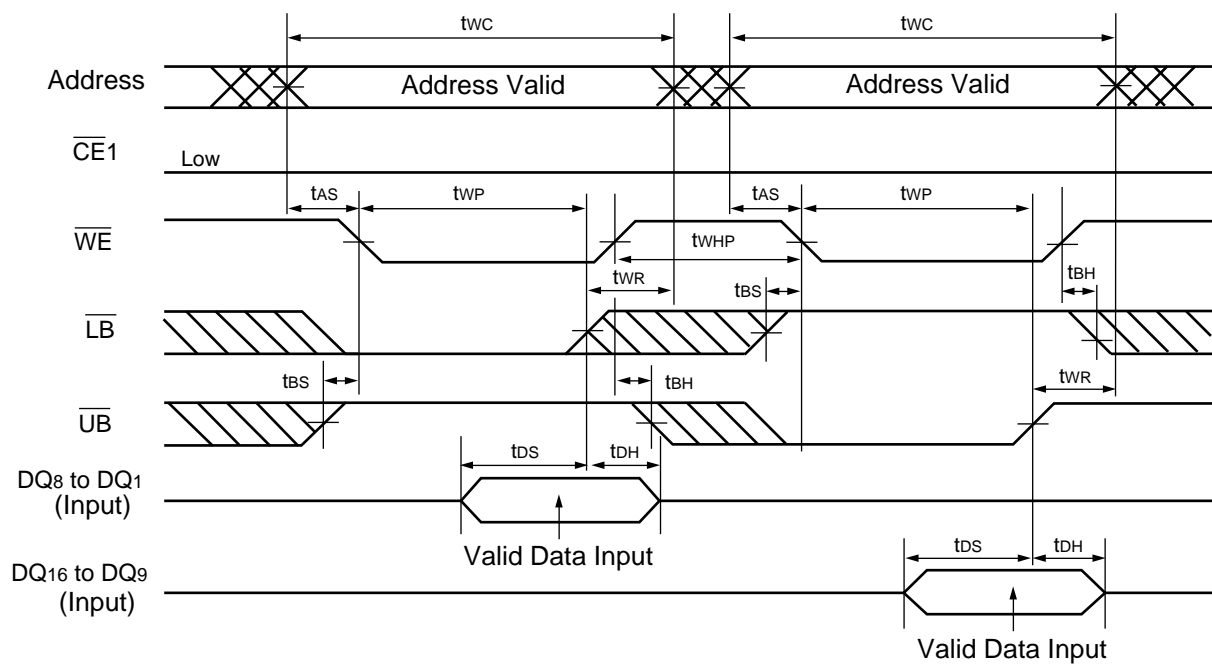
Note : This timing diagram assumes $\text{CE2} = \text{"H"}$.

5. WRITE Timing 2 ($\overline{\text{WE}}$ Control)



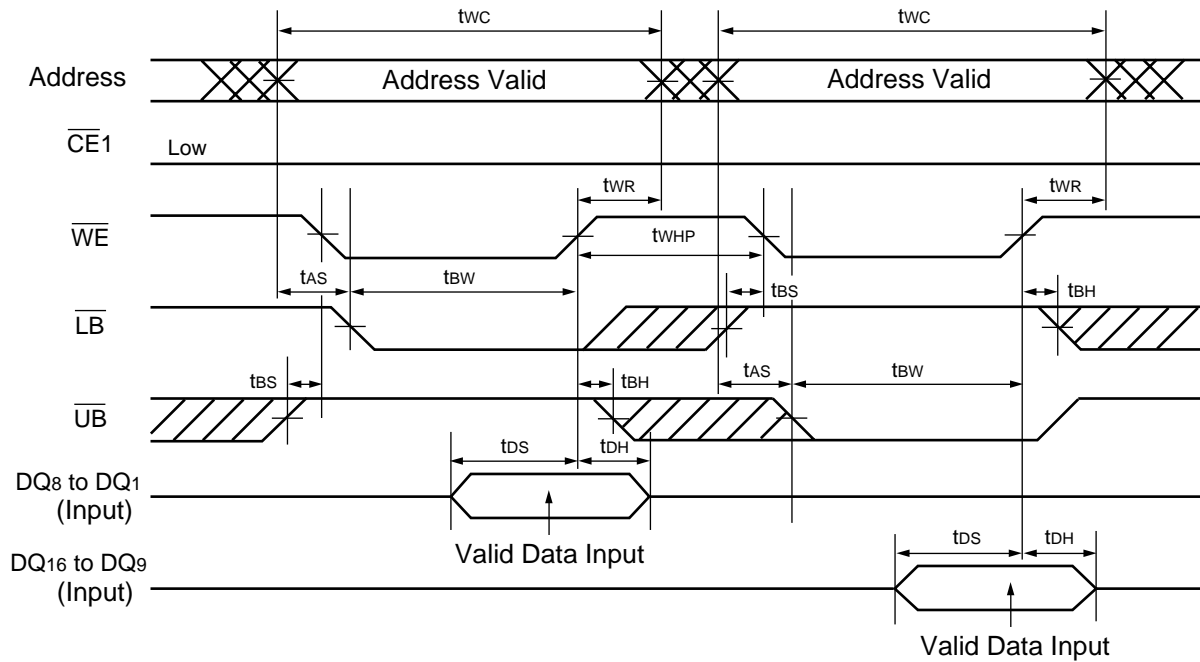
Note : This timing diagram assumes $\text{CE2} = \text{"H"}$.

6. WRITE Timing 3-1 ($\overline{\text{WE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Write Control)



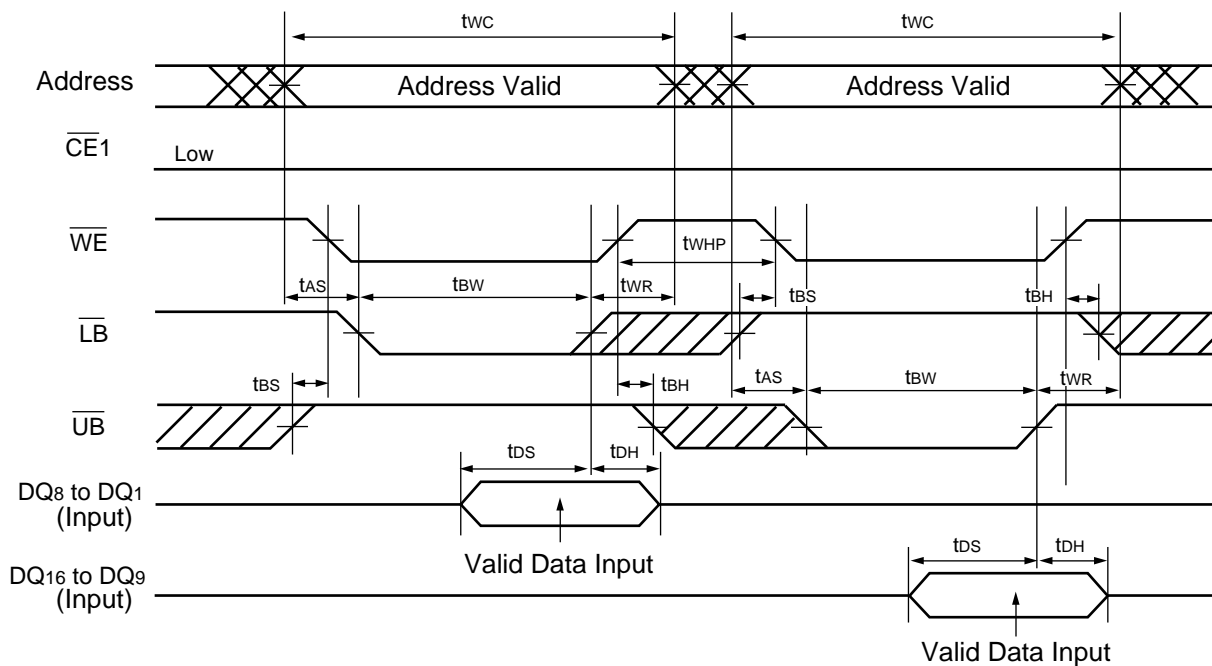
Note : This timing diagram assumes $\text{CE2} = \text{"H"}$ and $\overline{\text{OE}} = \text{"H"}$.

7. WRITE Timing 3-2 ($\overline{\text{WE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Write Control)



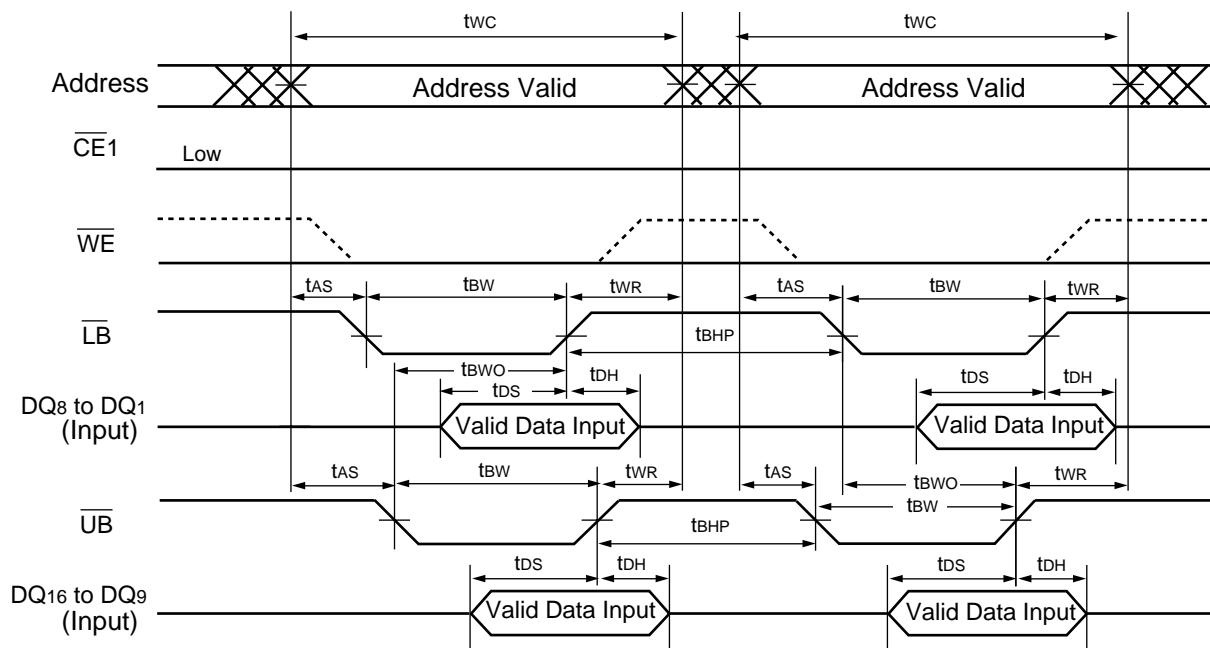
Note : This timing diagram assumes $\text{CE2} = \text{"H"}$ and $\overline{\text{OE}} = \text{"H"}$.

8. WRITE Timing 3-3 ($\overline{\text{WE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Write Control)



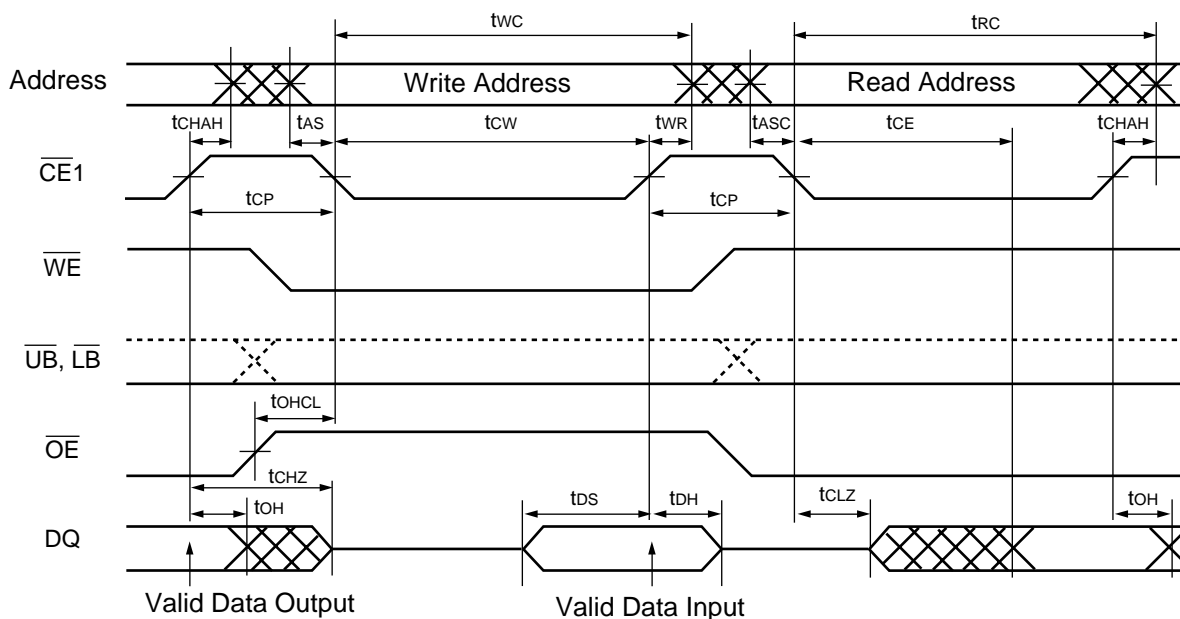
Note : This timing diagram assumes $\text{CE2} = \text{"H"}$ and $\overline{\text{OE}} = \text{"H"}$.

9. WRITE Timing 3-4 (\overline{WE} , \overline{LB} , \overline{UB} Byte Write Control)



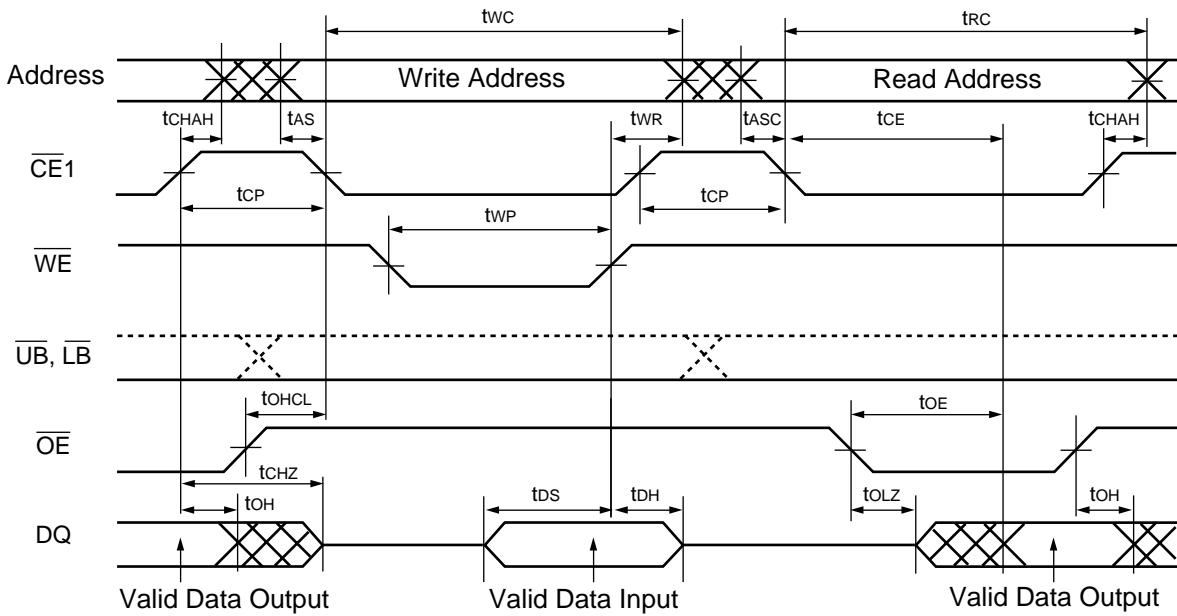
Note : This timing diagram assumes $\overline{CE2} = "H"$ and $\overline{OE} = "H"$.

10. READ/WRITE Timing 1-1 ($\overline{CE1}$ Control)



Note : This timing diagram assumes $\overline{CE2} = "H"$.
Write address is valid from either $\overline{CE1}$ or \overline{WE} of last falling edge.

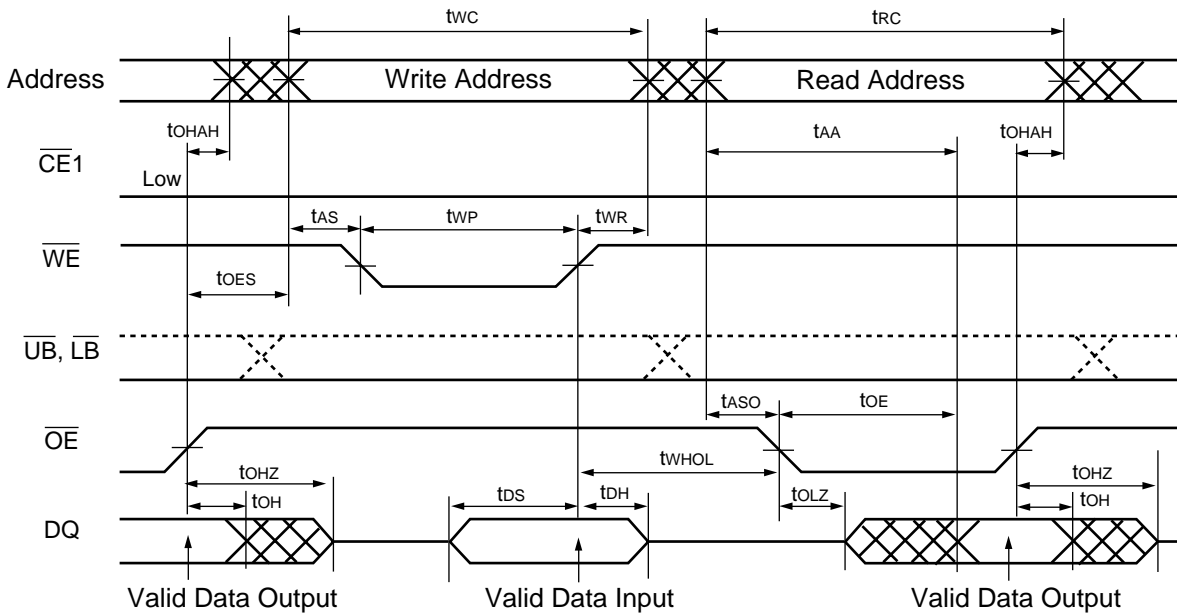
11. READ/WRITE Timing 1-2 ($\overline{CE1}$, \overline{WE} , \overline{OE} Control)



Note : This timing diagram assumes $CE2 = "H"$.

\overline{OE} can be fixed Low during write operation if it is $\overline{CE1}$ controlled write at Read-Write-Read sequence.

12. READ/WRITE Timing 2 (\overline{OE} , \overline{WE} Control)



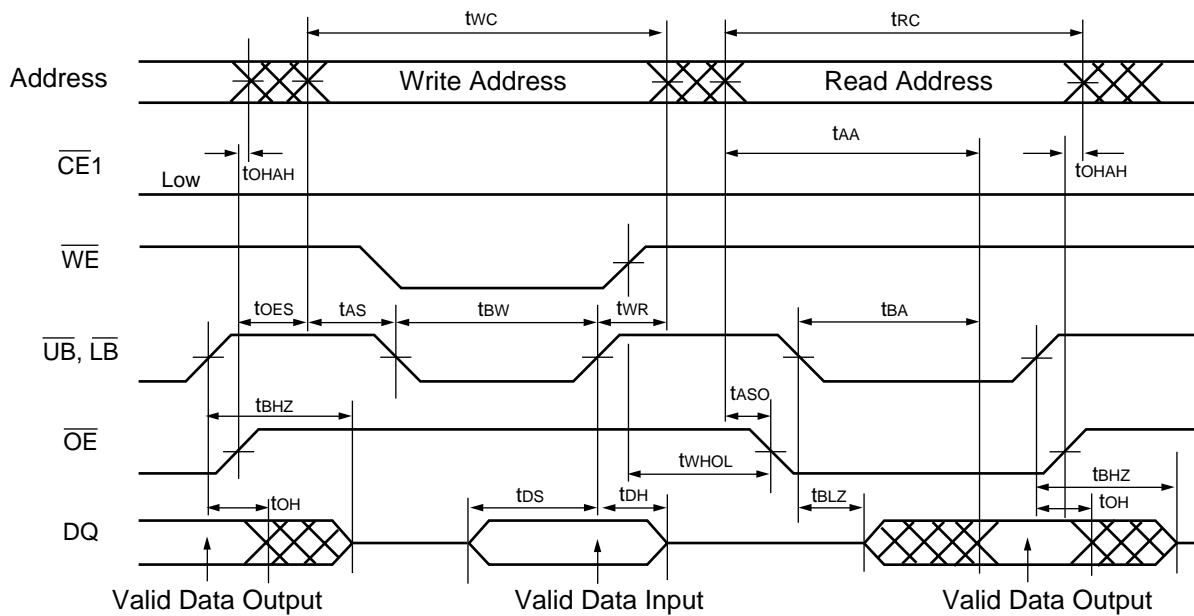
Note : This timing diagram assumes $CE2 = "H"$.

$\overline{CE1}$ can be tied to Low for \overline{WE} and \overline{OE} controlled operation.

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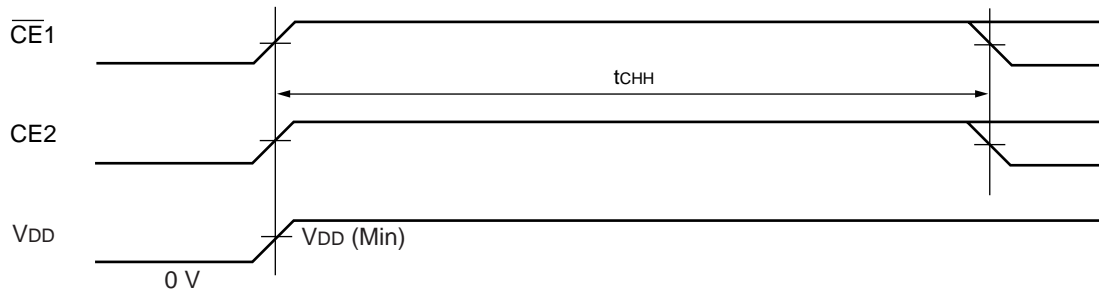
13. READ/WRITE Timing 3 (\overline{OE} , \overline{WE} , \overline{LB} , \overline{UB} Control)



Note : This timing diagram assumes $CE2 = "H"$.

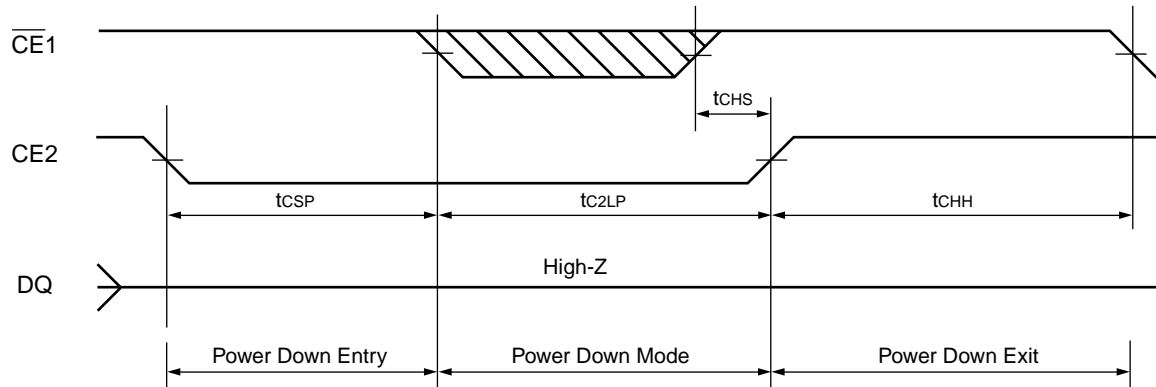
$\overline{CE1}$ can be tied to Low for \overline{WE} and \overline{OE} controlled operation.

14. POWER-UP Timing



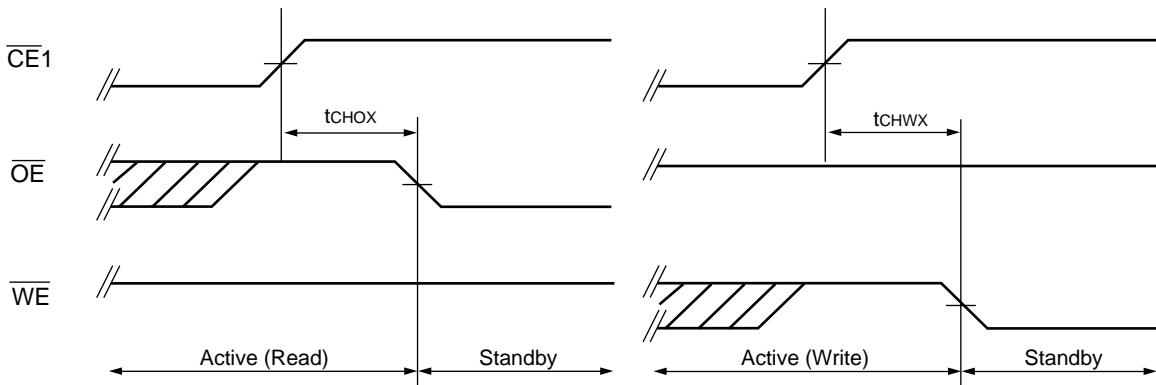
Note : t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both $\overline{CE1}$ and $CE2$.

15. POWER DOWN Entry and Exit Timing



Note : This Power Down mode can be also used as a reset timing if POWER-UP timing above could not be satisfied and Power Down program was not performed prior to this reset.

16. Standby Entry Timing after Read or Write



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.
If either of timing is not satisfied, it takes t_{RC} (Min) period for Standby mode from $\overline{CE1}$ Low to High transition.

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■ BONDING PAD INFORMATION

Please contact local FUJITSU representative for pad layout and pad coordinate information.

■ ORDERING INFORMATION

Part Number	Shipping Form	Remarks
MB82DS01181E-70LWT-A	Wafer	

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