



查询"24C01A-E/P"供应商

MICROCHIP

24C01A/02A/04A

1K/2K/4K 5.0V I²C™ Serial EEPROMs

FEATURES

- Low power CMOS technology
- Hardware write protect
- Two wire serial interface bus, I²C™ compatible
- 5.0V only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer
- 1ms write cycle time for single byte
- 1,000,000 Erase/Write cycles guaranteed
- Data retention >200 years
- 8-pin DIP/SOIC packages
- Available for extended temperature ranges
 - Commercial (C): 0°C to +70°C
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C

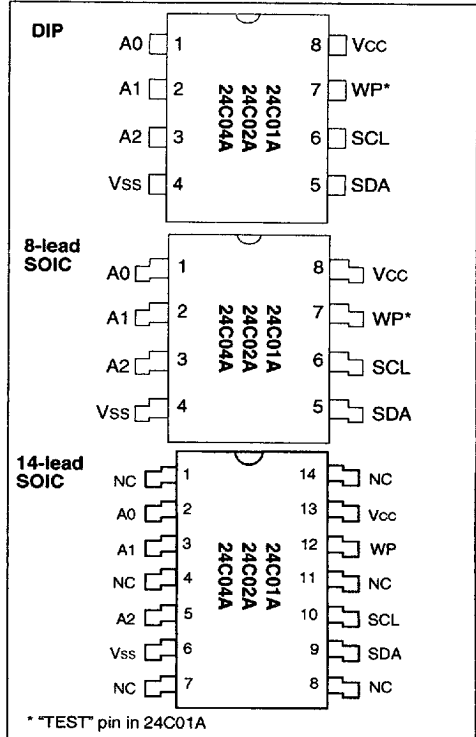
DESCRIPTION

The Microchip Technology Inc. 24C01A/02A/04A is a 1K/2K/4K bit Electrically Erasable PROM. The device is organized as shown, with a standard two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature in the 24C02A and 24C04A provides hardware write protection for the upper half of the block. The 24C01A and 24C02A have a page write capability of two bytes and the 24C04A has a page length of eight bytes. Up to eight 24C01A or 24C02A devices and up to four 24C04A devices may be connected to the same two wire bus.

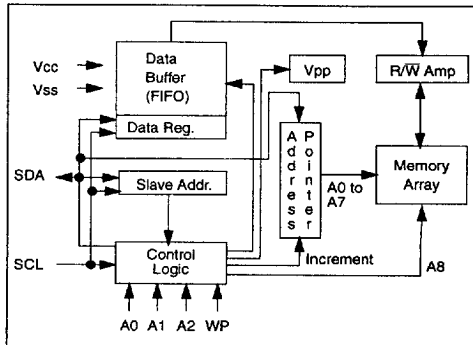
This device offers fast (1ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 24LCXXB.

	24C01A	24C02A	24C04A
Organization	128 x 8	256 x 8	2 x 256 x 8
Write Protect	None	080-0FF	100-1FF
Page Write Buffer	2 Bytes	2 Bytes	8 Bytes

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

24C01A/02A/04A

1.0 ELECTRICAL CHARACTERISTICS

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1.1 Maximum Ratings*

V_{CC} 7.0V
 All inputs and outputs w.r.t. V_{SS} -0.6V to V_{CC} +1.0V
 Storage temperature -65°C to +150°C
 Ambient temp. with power applied..... -65°C to +125°C
 Soldering temperature of leads (10 seconds) +300°C
 ESD protection on all pins..... 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0	No Function for 24C04A only, Must be connected to V _{CC} or V _{SS}
A0, A1, A2	Chip Address Inputs
V _{SS}	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
TEST	(24C01A only) V _{CC} or V _{SS}
WP	Write Protect Input
V _{CC}	+5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

V _{CC} = +5V (±10%)		Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C			
Parameter	Symbol	Min.	Max.	Units	Conditions
V _{CC} detector threshold	V _{TH}	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	V _{IH}	V _{CC} x 0.7	V _{CC} + 1	V	I _{OL} = 3.2 mA (SDA only)
Low level input voltage	V _{IL}	-0.3	V _{CC} x 0.3	V	
Low level output voltage	V _{OL}		0.4	V	
A1 & A2 pins:					
High level input voltage	V _{IH}	V _{CC} - 0.5	V _{CC} + 0.5	V	
Low level input voltage	V _{IL}	-0.3	0.5	V	
Input leakage current	I _{LI}	—	10	µA	V _{IN} = 0V to V _{CC}
Output leakage current	I _{LO}	—	10	µA	V _{OUT} = 0V to V _{CC}
Pin capacitance (all inputs/outputs)	C _{IN} , C _{OUT}	—	7.0	pF	V _{IN} /V _{OUT} = 0V (Note) Tamb = +25°C, f = 1 MHz
Operating current	I _{CC} Write	—	3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, V _{CC} = 5V, Tamb = 0°C to +70°C
	I _{CC} Write	—	4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, V _{CC} = 5V, Tamb = (I) and (E)
	I _{CC} Read	—	750	µA	V _{CC} = 5V, Tamb = (C), (I) and (E)
	I _{CC} Read	—			
Standby current	I _{CCS}	—	100	µA	SDA=SCL=V _{CC} =5V (no PROGRAM active)

Note: This parameter is periodically sampled and not 100% tested

FIGURE 1-1: BUS TIMING START/STOP

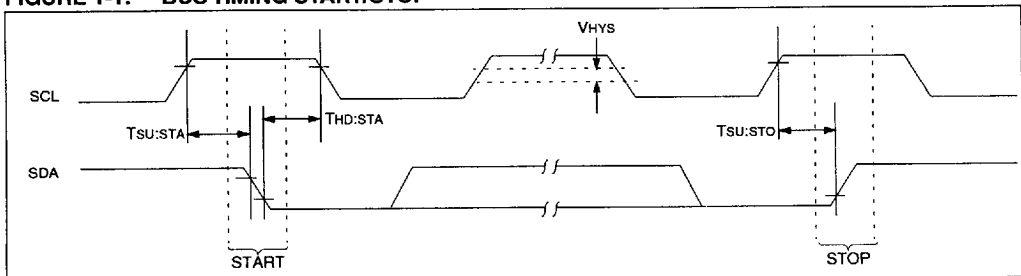


TABLE 1-3: AC CHARACTERISTICS

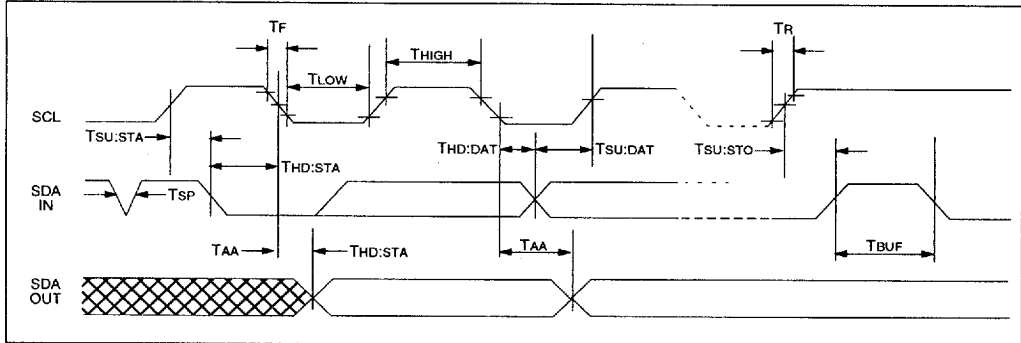
Parameter	Symbol	Min.	Typ	Max.	Units	Remarks
Clock frequency	FCLK	—	—	100	kHz	
Clock high time	THIGH	4000	—	—	ns	
Clock low time	TLOW	4700	—	—	ns	
SDA and SCL rise time	Tr	—	—	1000	ns	
SDA and SCL fall time	Tf	—	—	300	ns	
START condition hold time	THD:STA	4000	—	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	—	ns	
Data input setup time	TSU:DAT	250	—	—	ns	
Data output delay time	TAA	300	—	3500		(Note 1)
STOP condition setup time	TSU:STO	4700	—	—	ns	
Bus free time	TBUF	4700	—	—	ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	Ti	—	—	100	ns	
Program cycle time	TWC	—	.4 .4N	1 N	ms ms	Byte mode Page mode, N=# of bytes
Endurance	—	1M	—	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 2)

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

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FIGURE 1-2: BUS TIMING DATA



24C01A/02A/04A

2.0 FUNCTIONAL DESCRIPTION

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The 24C01A/02A/04A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C01A/02A/04A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24C01/24C02s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Up to four 24C04As can be connected to the bus, selected by A1 and A2 chip address inputs. A0 must be tied to Vcc or Vss for the 24C04A. Other devices can be connected to the bus but require different device codes than the 24C01A/02A/04A (refer to section Slave Address).

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C01A/02A/04A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

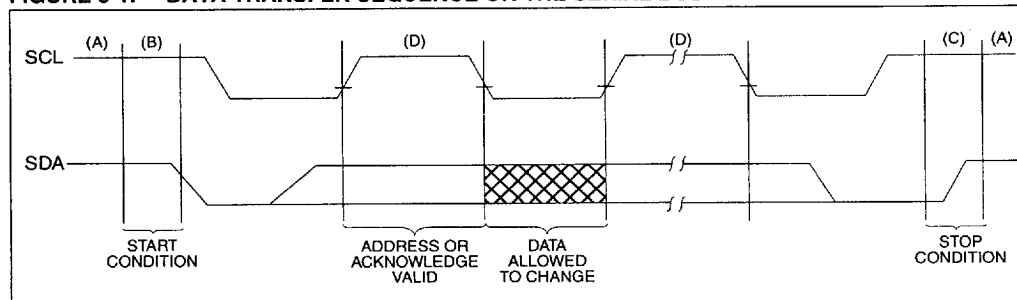


FIGURE 6-1: BYTE WRITE

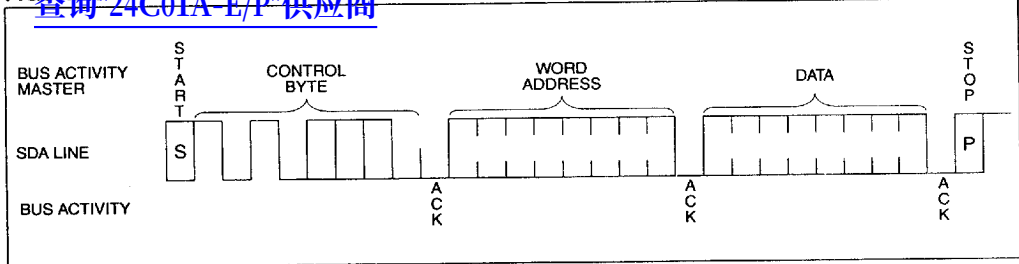
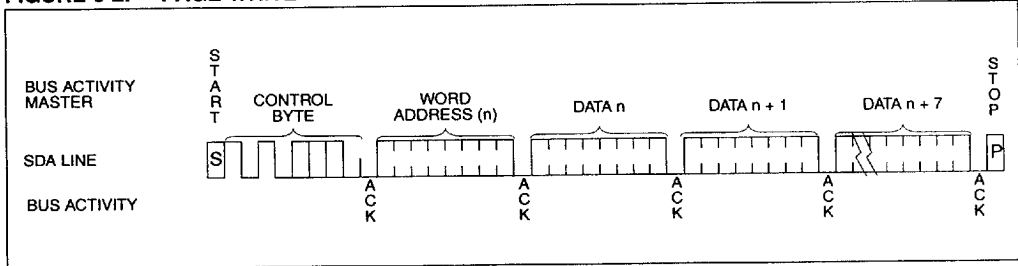


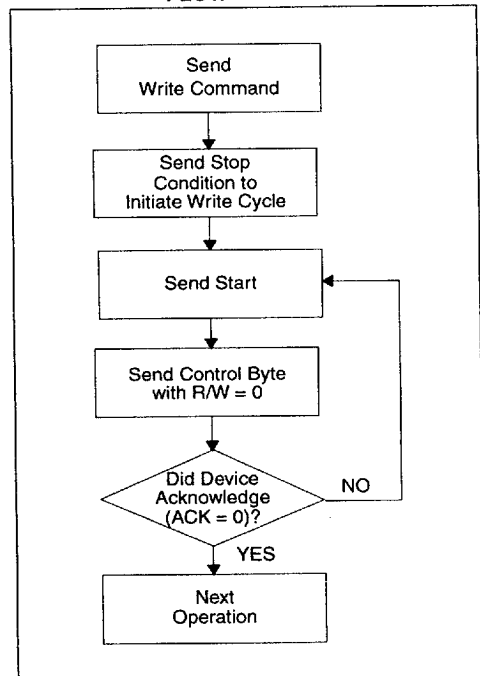
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\bar{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the 24C02A or 24C04A is connected to Vcc (+5.0V). The device will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C02A/04A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted. Polarity of the WP pin has no effect on the 24C01A.

9.0 READ MODE

This mode illustrates master device reading data from the 24C01A/02A/04A.

As can be seen from Figure 9-2 and Figure 9-3, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to). During this period the 24C01A/02A/04A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This auto-increment sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note 1: If the master knows where the address pointer is, it can begin the read sequence at the current address (Figure 9-1) and save time transmitting the slave and word addresses.

Note 2: In all modes, the address pointer will not increment through a block (256 byte) boundary, but will rotate back to the first location in that block.

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FIGURE 9-1: CURRENT ADDRESS READ

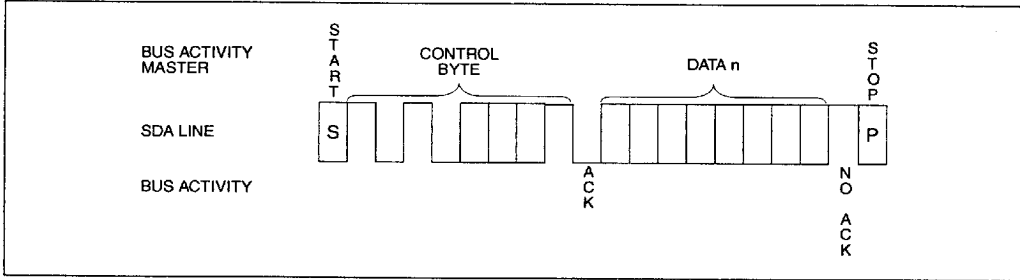


FIGURE 9-2: RANDOM READ

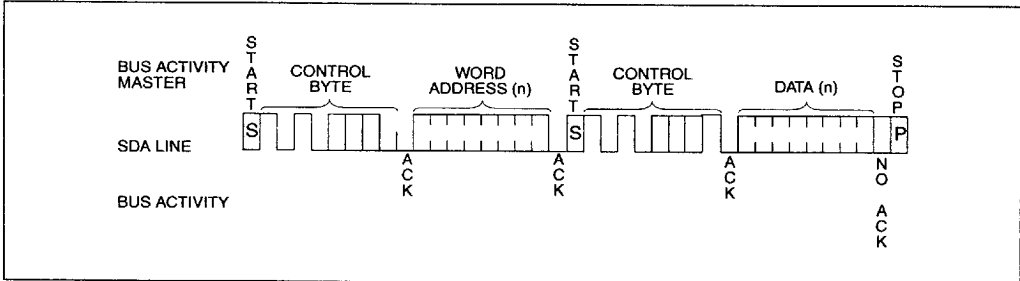
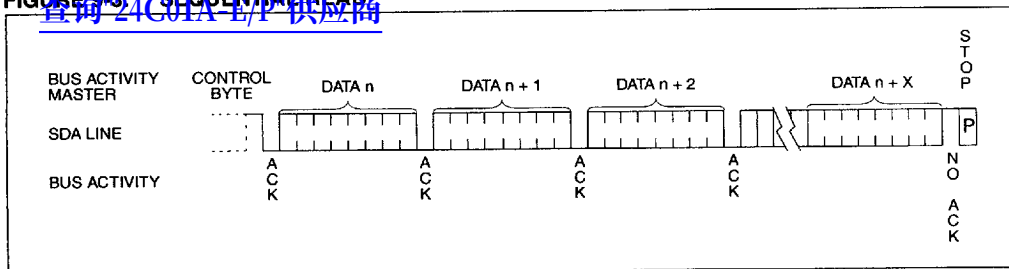


FIGURE 9-3: SEQUENTIAL READ



10.0 PIN DESCRIPTION

10.1 A0, A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. For 24C04 A0 is no function.

Up to eight 24C01A/02A's or up to four 24C04A's can be connected to the bus.

These inputs must be connected to either VSS or VCC.

10.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10K Ω).

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

10.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

10.4 WP Write Protection

This pin must be connected to either Vcc or VSS for 24C02A or 24C04A. It has no effect on 24C01A.

If tied to Vcc, PROGRAM operations onto the upper memory block will not be executed. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Note 1: A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C04A page is 8 bytes long; the 24C01A/02A page is 2 bytes long.

Note 2: A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C04A has two blocks, 256 bytes each. The 24C01A and 24C02A each have only one block.

NOTES:

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24C01A/02A/04A

24C01A/02A/04A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24C01A/02A/04A -		/P	
		Package:	P = Plastic DIP SN = Plastic SOIC (150 mil Body), 8-lead SM = Plastic SOIC (207 mil Body), 8-lead SL = Plastic SOIC (150 mil Body), 14-lead, 24C04A only
		Temperature Range:	Blank = 0°C to +70°C I = -40°C to +85°C E = -40°C to +125°C
		Device:	24C01A 1K I ² C Serial EEPROM 24C01AT 1K I ² C Serial EEPROM (Tape and Reel) 24C02A 2K I ² C Serial EEPROM 24C02AT 2K I ² C Serial EEPROM (Tape and Reel) 24C04A 4K I ² C Serial EEPROM 24C04AT 4K I ² C Serial EEPROM (Tape and Reel)