14-Bit, 400MSPS Digital-to-Analog Converter

FEATURES

- 400MSPS Update Rate
- LVDS-Compatible Input Interface
- Spurious-Free Dynamic Range (SFDR) to Nyquist:
  - 69dBc at 70MHz IF, 400MSPS
- W-CDMA Adjacent Channel Power Ratio (ACPR):
  - 73dBc at 30.72MHz IF, 122.88MSPS
  - 71dBc at 61.44MHz IF, 245.76MSPS
- Differential Scalable Current Sink Outputs: 2mA to 20mA
- On-Chip 1.2V Reference
- Single 3.3V Supply Operation
- Power Dissipation: 660mW at f_{CLK} = 400MSPS, f_{OUT} = 20MHz
- Package: 48-Pin HTQFP PowerPad™, T_{JA} = 28.8°C/W

APPLICATIONS

- Cellular Base Transceiver Station Transmit Channel:
  - CDMA: WCDMA, CDMA2000, IS-95
  - TDMA: GSM, IS-136, EDGE/GPRS
  - Supports Single-Carrier and Multicarrier Applications
- Test and Measurement: Arbitrary Waveform Generation
- Direct Digital Synthesis (DDS)
- Cable Modem Headend

DESCRIPTION

The DAC5675A is a 14-bit resolution high-speed digital-to-analog converter. The DAC5675A is designed for high-speed digital data transmission in wired and wireless communication systems, high-frequency direct-digital synthesis (DDS), and waveform reconstruction in test and measurement applications. The DAC5675A has excellent spurious-free dynamic range (SFDR) at high intermediate frequencies, which makes the DAC5675A well-suited for multicarrier transmission in TDMA- and CDMA-based cellular base transceiver stations (BTSs).

The DAC5675A operates from a single-supply voltage of 3.3V. Power dissipation is 660mW at f_{CLK} = 400MSPS, f_{OUT} = 70MHz. The DAC5675A provides a nominal full-scale differential current output of 20mA, supporting both single-ended and differential applications. The output current can be directly fed to the load with no additional external output buffer required. The output is referred to the analog supply voltage AV_{DD}.

The DAC5675A comprises a low-voltage differential signaling (LVDS) interface for high-speed digital data input. LVDS features a low differential voltage swing with a low constant power consumption across frequency, allowing for high-speed data transmission with low noise levels; that is, with low electromagnetic interference (EMI). LVDS is typically implemented in low-voltage digital CMOS processes, making it the ideal technology for high-speed interfacing between the DAC5675A and high-speed low-voltage CMOS ASICs or FPGAs. The DAC5675A current-sink-array architecture supports update rates of up to 400MSPS. On-chip edge-triggered input latches provide for minimum setup and hold times, thereby relaxing interface timing.

The DAC5675A has been specifically designed for a differential transformer-coupled output with a 50Ω doubly-terminated load. With the 20mA full-scale output current, both a 4:1 impedance ratio (resulting in an output power of 4dBm) and 1:1 impedance ratio transformer (–2dBm) are supported. The last configuration is preferred for optimum performance at high output frequencies and update rates. The outputs are terminated to AVDD and have voltage compliance ranges from AV_{DD} – 1 to AV_{DD} + 0.3V.

An accurate on-chip 1.2V temperature-compensated bandgap reference and control amplifier allows the user to adjust this output current from 20mA down to 2mA. This provides 20dB gain range control capabilities. Alternatively, an external reference voltage may be applied. The DAC5675A features a SLEEP mode, which reduces the standby power to approximately 18mW.

The DAC5675A is available in a 48-pin HTQFP thermally-enhanced PowerPad package. This package increases thermal efficiency in a standard size IC package. The device is characterized for operation over the industrial temperature range of –40°C to +85°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		DAC5675A	UNIT
Supply voltage range	AV_{DD}(2)	–0.3 to +3.6	V
	DV_{DD}(3)	–0.3 to +3.6	V
	AV_{DD} to DV_{DD}	–3.6 to +3.6	V
Voltage between AGND and DGND		–0.3 to +0.5	V
CLK, CLKC(2)		–0.3 to AV_{DD} + 0.3	V
Digital input D[13:0]A, D[13:0]B(3), SLEEP		–0.3 to DV_{DD} + 0.3	V
IOUT1, IOUT2(2)		–1.0 to AV_{DD} + 0.3	V
EXTIO, BIAS(2)		–1.0 to AV_{DD} + 0.3	V
Peak input current (any input)		20	mA
Peak total input current (all inputs)		-30	mA
Operating free-air temperature range, T_A		–40 to +85	°C
Storage temperature range		–65 to +150	°C
Lead temperature 1,6mm (1/16in) from the case for 10s		+260	°C

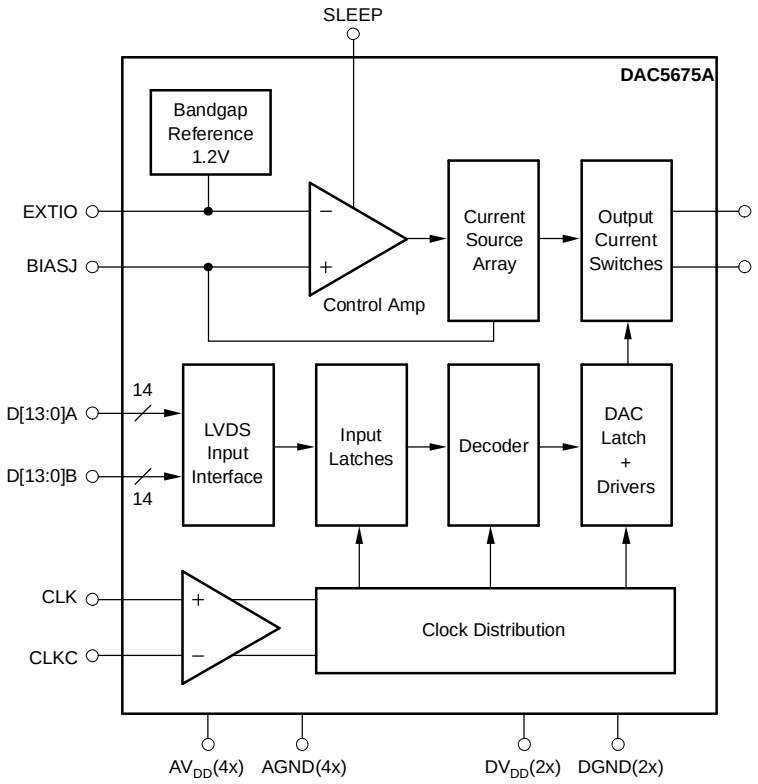
(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure outside of absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND.
(3) Measured with respect to DGND.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC5675A	48-HTQFP	PHP	–40°C to +85°C	DAC5675A	DAC5675AIPHP	Tray, 250
					DAC5675AIPHPR	Tray, 1000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

Functional Block Diagram



DC ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range. Typical values at +25°C, AV_{DD} = 3.3V, DV_{DD} = 3.3V, $I_{O(FS)}$ = 20mA, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DAC5675A			
			MIN	TYP	MAX	UNIT
Resolution			14			Bit
DC Accuracy(1)						
INL	Integral nonlinearity	T_{MIN} to T_{MAX}	–4	±1.5	4	LSB
DNL	Differential nonlinearity		–2	±0.6	2	LSB
Monotonicity			Monotonic 12b Level			
Analog Output						
$I_{O(FS)}$	Full-scale output current		2		20	mA
	Output compliance range	AV_{DD} = 3.15V to 3.45V, $I_{O(FS)}$ = 20mA	AV_{DD}– 1		AV_{DD} +0.3	V
	Offset error			0.01		%FSR
	Gain error	Without internal reference	–10	5	10	%FSR
		With internal reference	–10	2.5	10	%FSR
	Output resistance			300		kΩ
	Output capacitance			5		pF
Reference Output						
$V_{(EXTIO)}$	Reference voltage		1.17	1.23	1.29	V
	Reference output current(2)			100		nA
Reference Input						
$V_{(EXTIO)}$	Input reference voltage		0.6	1.2	1.25	V
	Input resistance			1		MΩ
	Small-signal bandwidth			1.4		MHz
	Input capacitance			100		pF
Temperature Coefficients						
	Offset drift			12		ppm of FSR/°C
$\Delta V_{(EXTIO)}$	Reference voltage drift			±50		ppm/°C
Power Supply						
AV_{DD}	Analog supply voltage		3.15	3.3	3.6	V
DV_{DD}	Digital supply voltage		3.15	3.3	3.6	V
$I_{(AVDD)}$	Analog supply current(3)			115		mA
$I_{(DVDD)}$	Digital supply current(3)			85		mA
P_D	Power dissipation	Sleep mode		18		mW
P_D	Power dissipation	AV_{DD} = 3.3V, DV_{DD} = 3.3V		660	900	mW
APSRR	Analog and digital power-supply rejection ratio	AV_{DD} = 3.15V to 3.45V	–0.5	±0.1	0.5	%FSR/V
DPSRR			–0.5	±0.1	0.5	%FSR/V

(1) Measured differential at I_{OUT1} and I_{OUT2}; 25Ω to AV_{DD}.
(2) Use an external buffer amplifier with high impedance input to drive any external load.
(3) Measured at f_{CLK} = 400MSPS and f_{OUT} = 70MHz.

AC ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range. Typical values at +25°C, AV_{DD} = 3.3V, DV_{DD} = 3.3V, $I_{O(FS)}$ = 20mA, differential transformer-coupled output, 50Ω doubly-terminated load, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DAC5675A			
			MIN	TYP	MAX	UNIT
Analog Output						
f_{CLK}	Output update rate				400	MSPS
$t_{s(DAC)}$	Output setting time to 0.1%	Transition: code x2000 to $x23_{FF}$		12		ns
t_{PD}	Output propagation delay			1		ns
$t_{r(IOUT)}$	Output rise time, 10% to 90%			300		ps
$t_{f(IOUT)}$	Output fall time, 90% to 10%			300		ps
	Output noise(1)	$IOUT_{FS}$ = 20mA		55		pA/√Hz
		$IOUT_{FS}$ = 2mA		30		pA/√Hz
AC Linearity						
THD	Total harmonic distortion	f_{CLK} = 100MSPS, f_{OUT} = 19.9MHz		73		dBc
		f_{CLK} = 160MSPS, f_{OUT} = 41MHz		72		dBc
		f_{CLK} = 200MSPS, f_{OUT} = 70MHz		68		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 20.1MHz		72		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 70MHz		71		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 140MHz		58		dBc
SFDR	Spurious-free dynamic range to Nyquist	f_{CLK} = 100MSPS, f_{OUT} = 19.9MHz		73		dBc
		f_{CLK} = 160MSPS, f_{OUT} = 41MHz		73		dBc
		f_{CLK} = 200MSPS, f_{OUT} = 70MHz		70		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 20.1MHz		73		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 70MHz		74		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 140MHz		60		dBc
SFDR	Spurious-free dynamic range within a window, 5MHz span	f_{CLK} = 100MSPS, f_{OUT} = 19.9MHz		88		dBc
		f_{CLK} = 160MSPS, f_{OUT} = 41MHz		87		dBc
		f_{CLK} = 200MSPS, f_{OUT} = 70MHz		82		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 20.1MHz		87		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 70MHz		82		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 140MHz		75		dBc
ACPR	Adjacent channel power ratio WCDMA with 3.84MHz BW, 5MHz channel spacing	f_{CLK} = 122.88MSPS, IF = 30.72MHz(2)		73		dB
		f_{CLK} = 245.76MSPS, IF = 61.44MHz(3)		71		dB
		f_{CLK} = 399.32MSPS, IF = 153.36MHz(4)		65		dB
IMD	Two-tone intermodulation to Nyquist (each tone at -6dBfs)	f_{CLK} = 400MSPS, f_{OUT1} = 70MHz, f_{OUT2} = 71MHz		73		dBc
		f_{CLK} = 400MSPS, f_{OUT1} = 140MHz, f_{OUT2} = 141MHz		62		dBc
	Four-tone intermodulation, 15MHz span, missing center tone (each tone at -16dBfs)	f_{CLK} = 156MSPS, f_{OUT} = 15.6, 15.8, 16.2, 16.4MHz		82		dBc
		f_{CLK} = 400MSPS, f_{OUT} = 68.1, 69.3, 71.2, 72MHz		74		dBc

(1) Noise averaged up to 400MHz when operating at 400MSPS.
(2) See Figure 9.
(3) See Figure 10.
(4) See Figure 12

DIGITAL SPECIFICATIONS

Over operating free-air temperature range. Typical values at +25°C, AV_{DD} = 3.3V, DV_{DD} = 3.3V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DAC5675A			
			MIN	TYP	MAX	UNIT
LVDS Interface: nodes D[13:0]A, D[13:0]B						
V_{ITH+}	Positive-going differential input voltage threshold	See LVDS min/max threshold voltages table		100		mV
V_{ITH-}	Negative-going differential input voltage threshold			-100		mV
Z_T	Internal termination impedance		90	110	132	Ω
C_I	Input capacitance			2		pF
CMOS Interface (SLEEP):						
V_{IH}	High-level input voltage		2	3.3		V
V_{IL}	Low-level input voltage			0	0.8	V
I_{IH}	High-level input current		–100		100	µA
I_{IL}	Low-level input current		–10		10	µA
	Input capacitance			2		pF
Clock Interface (CLK, CLKC):						
|CLK-CLKC|	Clock differential input voltage		0.4		0.8	V_{PP}
	Clock duty cycle		40		60	%
V_{CM}	Common-mode voltage range			2 ±20%		V
	Input resistance	Node CLK, CLKC		670		Ω
	Input capacitance	Node CLK, CLKC		2		pF
	Input resistance	Differential		1.3		kΩ
	Input capacitance	Differential		1		pF
Timing						
t_{SU}	Input setup time		1.5			ns
t_H	Input hold time		0			ns
t_{DD}	Digital delay time (DAC latency)			3		clk

Timing Information

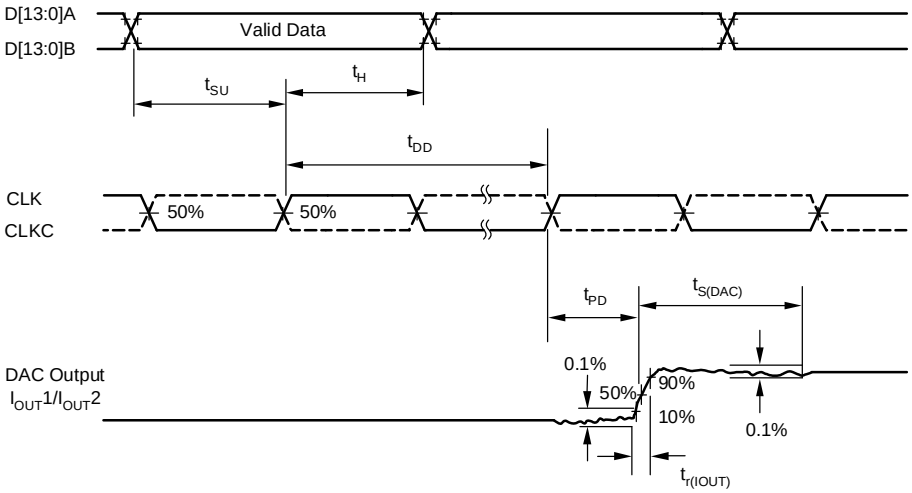


Figure 1. Timing Diagram

ELECTRICAL CHARACTERISTICS(1)

Over operating free-air temperature range, AV_{DD} = 3.3V, DV_{DD} = 3.3V, $I_{O(FS)}$ = 20mA, unless otherwise noted.

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	LOGICAL BIT BINARY EQUIVALENT	COMMENT
V_A [V]	V_B [V]	$V_{A,B}$ [mV]	V_{COM} [V]		
1.25	1.15	100	1.2	1	Operation with minimum differential voltage (±100mV) applied to the complementary inputs versus common-mode range
1.15	1.25	–100	1.2	0	
2.4	2.3	100	2.35	1	
2.3	2.4	–100	2.35	0	
0.1	0	100	0.05	1	
0	0.1	–100	0.05	0	
1.5	0.9	600	1.2	1	Operation with maximum differential voltage (±600mV) applied to the complementary inputs versus common-mode range
0.9	1.5	–600	1.2	0	
2.4	1.8	600	2.1	1	
1.8	2.4	–600	2.1	0	
0.6	0	600	0.3	1	
0	0.6	–600	0.3	0	

(1) Specifications subject to change.

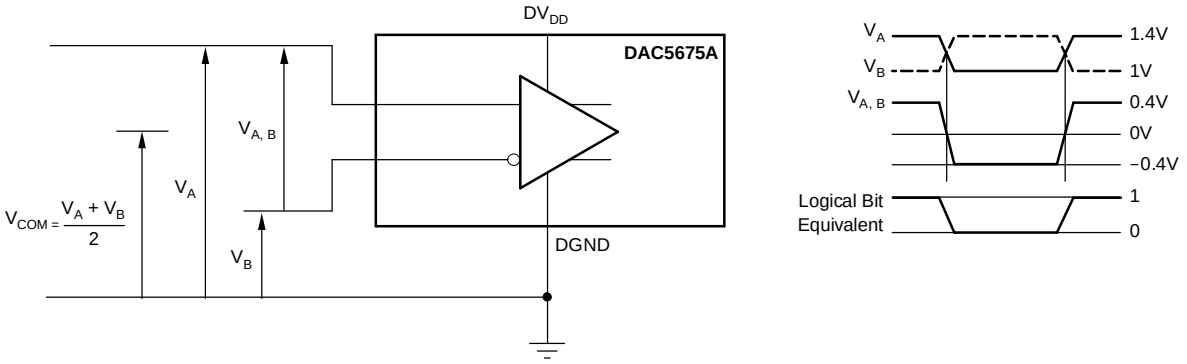


Figure 2. LVDS Timing Test Circuit and Input Test Levels

DEVICE INFORMATION

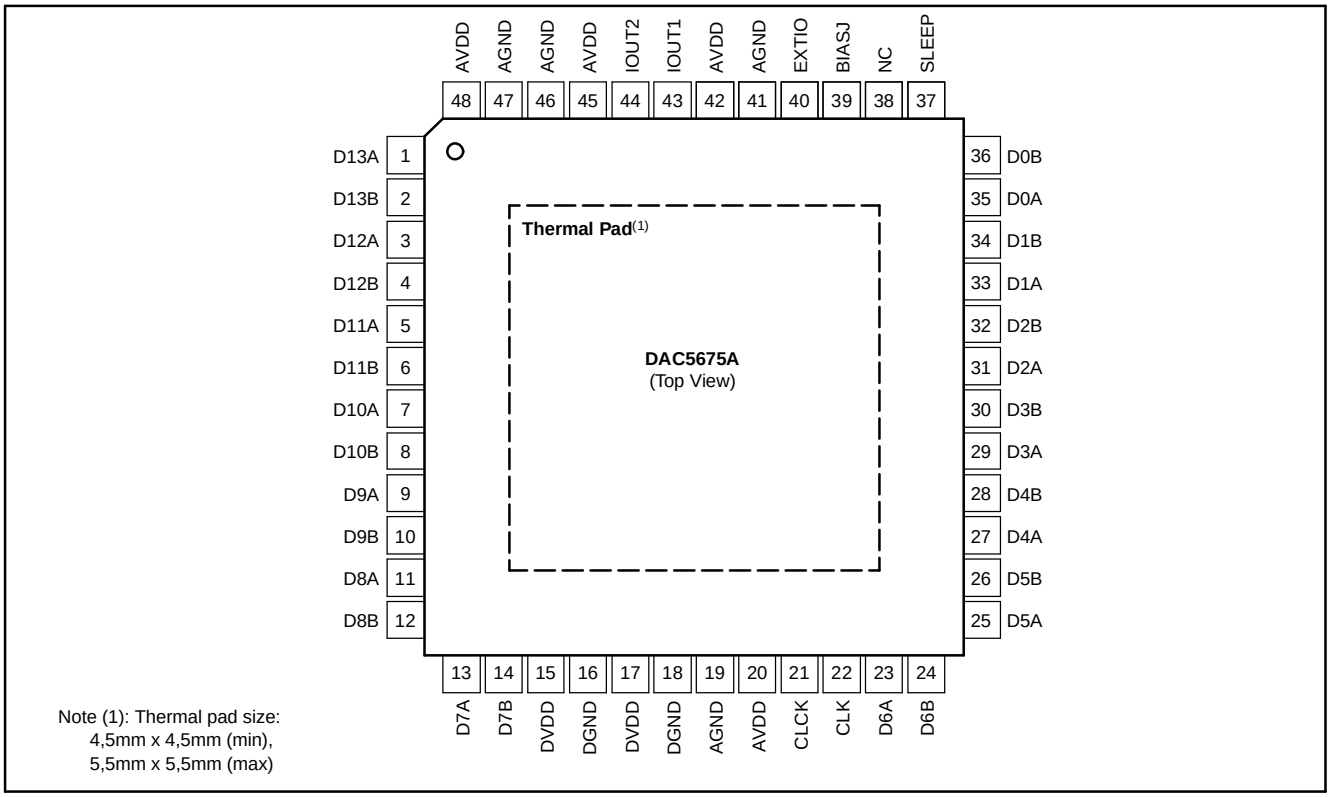


Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	19, 41, 46, 47	I	Analog negative supply voltage (ground); pin 47 internally connected to PowerPAD.
AV_{DD}	20, 42, 45, 48	I	Analog positive supply voltage.
BIASJ	39	O	Full-scale output current bias.
CLK	22	I	External clock input.
CLKC	21	I	Complementary external clock input.
D[13:0]A	1, 3, 5, 7, 9, 11, 13, 23, 25, 27, 29, 31, 33, 35	I	LVDS positive input, data bits 0 through 13. D13A is most significant data bit (MSB). D0A is least significant data bit (MSB).
D[13:0]B	2, 4, 6, 8, 10, 12, 14, 24, 26, 28, 30, 32, 34, 36	I	LVDS negative input, data bits 0 through 13. D13B is most significant data bit (MSB). D0B is least significant data bit (MSB).
DGND	16, 18	I	Digital negative supply voltage (ground).
NC	38	-—	Not connected in chip. Can be high or low.
DV_{DD}	15, 17	I	Digital positive supply voltage.
EXTIO	40	I/O	Internal reference output or external reference input. Requires a 0.1µF decoupling capacitor to AGND when used as reference output.
IOUT1	43	O	DAC current output. Full-scale when all input bits are set to '0'. Connect reference side of DAC load resistors to AV_{DD}.
IOUT2	44	O	DAC complementary current output. Full-scale when all input bits are set to '1'. Connect reference side of DAC load resistors to AV_{DD}.
SLEEP	37	I	Asynchronous hardware power down input. Active high. Internal pulldown.

TYPICAL CHARACTERISTICS

DIFFERENTIAL NON-LINEARITY (DNL) vs INPUT CODE

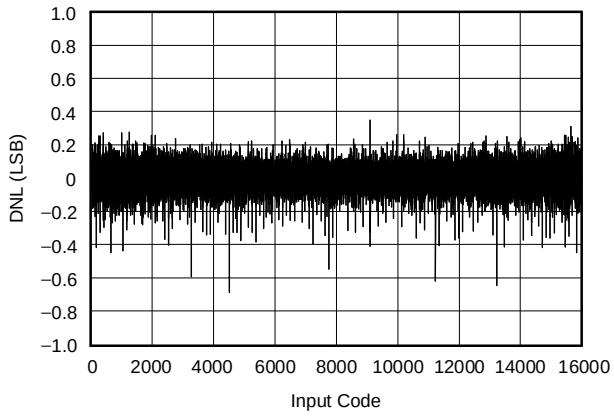


Figure 3.

INTEGRAL NON-LINEARITY (INL) vs INPUT CODE

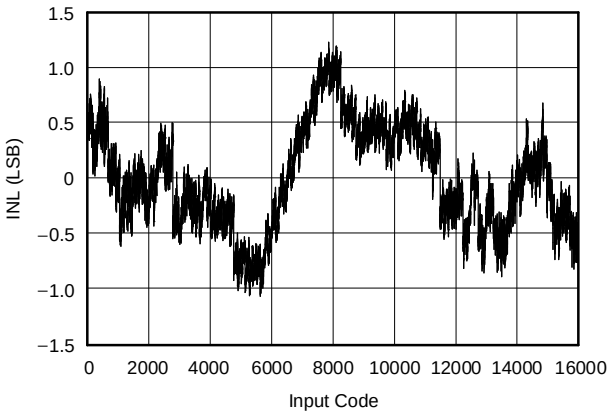


Figure 4.

TWO-TONE IMD (POWER) vs FREQUENCY

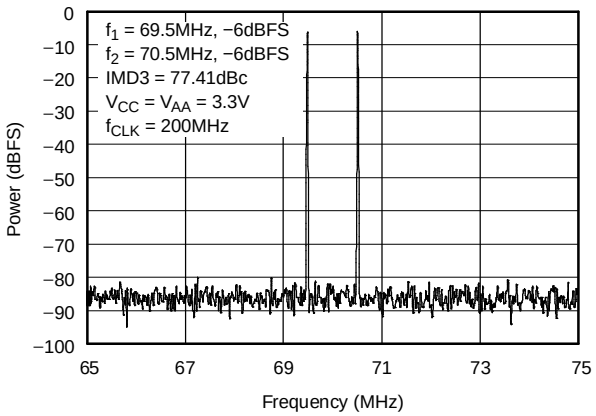


Figure 5.

TWO-TONE IMD3 vs FREQUENCY

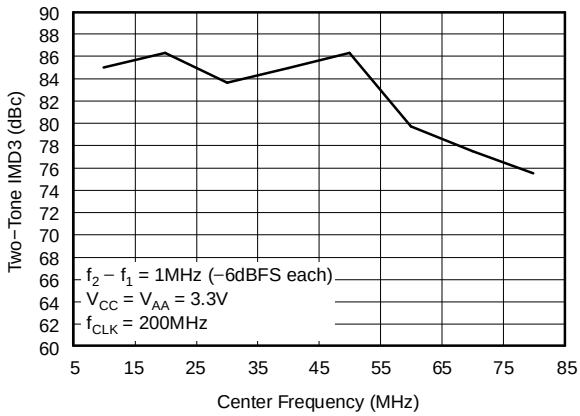


Figure 6.

SINGLE-TONE SPECTRUM POWER vs FREQUENCY

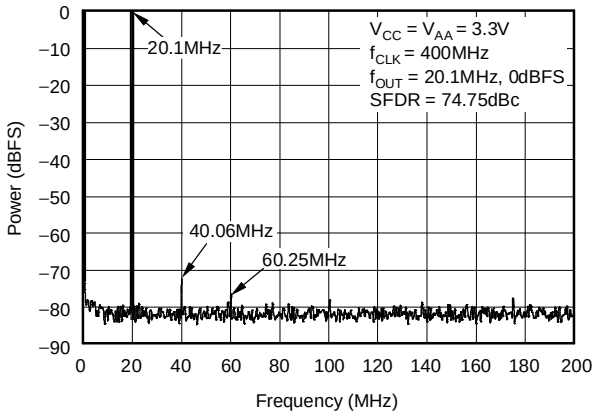


Figure 7.

SPURIOUS-FREE DYNAMIC RANGE vs FREQUENCY

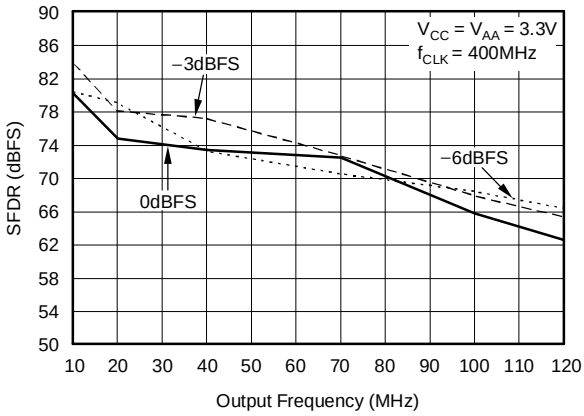


Figure 8.

TYPICAL CHARACTERISTICS (continued)

SPURIOUS-FREE DYNAMIC RANGE vs FREQUENCY

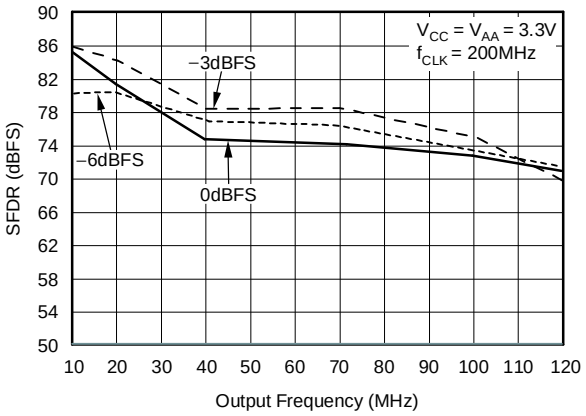


Figure 9.

W-CDMA TM1 SINGLE CARRIER POWER vs FREQUENCY

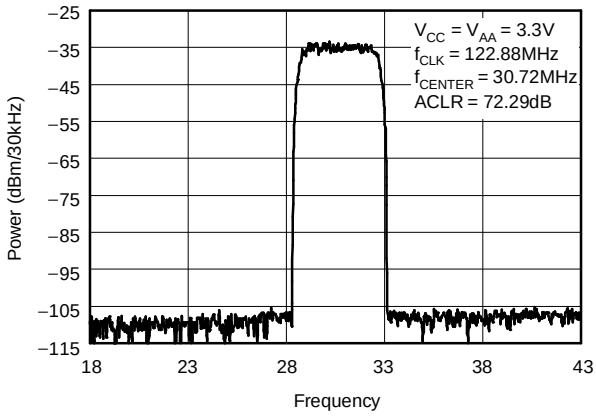


Figure 10.

W-CDMA TM1 DUAL CARRIER POWER vs FREQUENCY

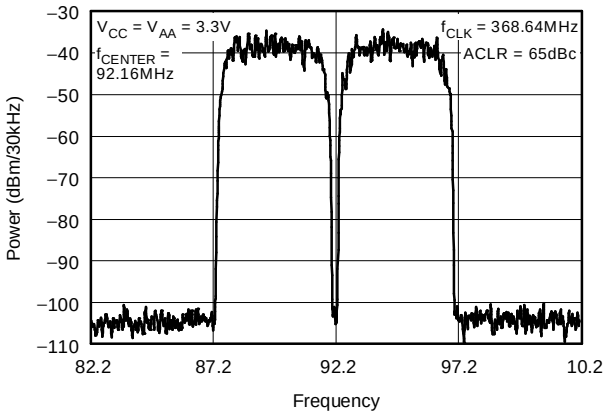


Figure 11.

W-CDMA TM1 SINGLE CARRIER ACLR vs OUTPUT FREQUENCY

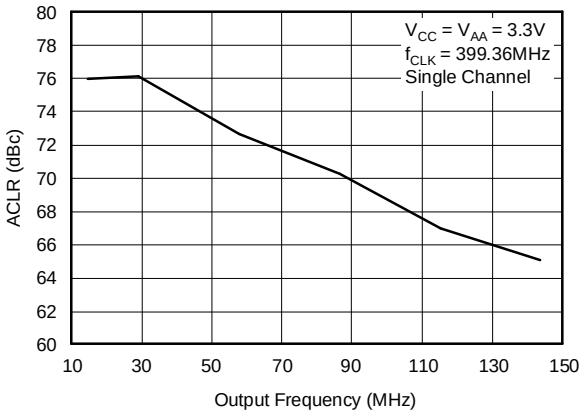


Figure 12.

APPLICATION INFORMATION

Detailed Description

Figure 13 shows a simplified block diagram of the current steering DAC5675A. The DAC5675A consists of a segmented array of NPN-transistor current sinks, capable of delivering a full-scale output current up to 20mA. Differential current switches direct the current of each current sink to either one of the complementary output nodes IOUT1 or IOUT2. The complementary current output enables differential operation, canceling out common-mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, and even-order distortion components, and doubling signal output power.

The full-scale output current is set using an external resistor (R_{BIAS}) in combination with an on-chip bandgap voltage reference source (1.2V) and control amplifier. The current (I_{BIAS}) through resistor R_{BIAS} is mirrored internally to provide a full-scale output current equal to 16 times I_{BIAS}. The full-scale current is adjustable from 20mA down to 2mA by using the appropriate bias resistor value.

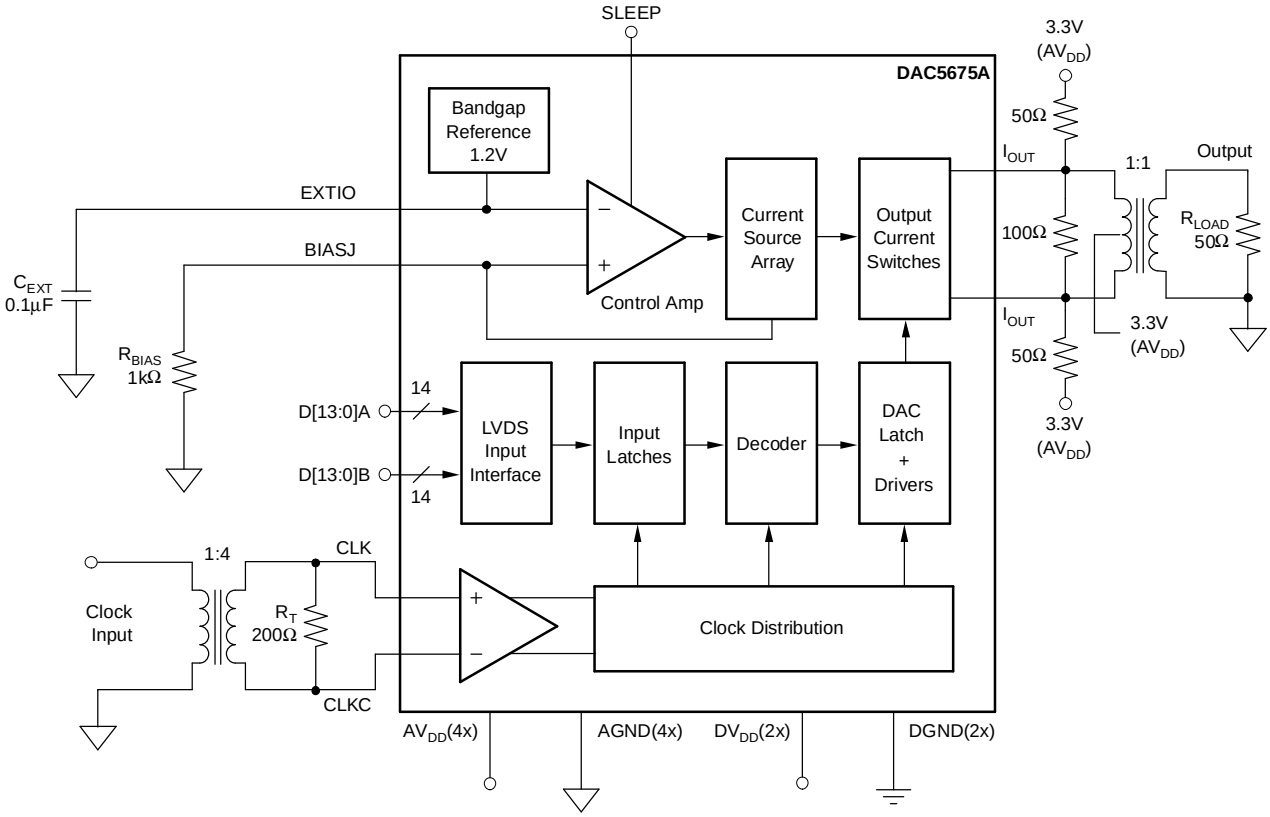


Figure 13. Application Schematic

APPLICATION INFORMATION (continued)

Digital Inputs

The DAC5675A uses a low voltage differential signaling (LVDS) bus input interface. The LVDS features a low differential voltage swing with low constant power consumption (≈4mA per complementary data input) across frequency. The differential characteristic of LVDS allows for high-speed data transmission with low electromagnetic interference (EMI) levels. The LVDS input minimum and maximum input threshold table lists the LVDS input levels. Figure 14 shows the equivalent complementary digital input interface for the DAC5675A, valid for pins D[13:0]A and D[13:0]B. Note that the LVDS interface features internal 110Ω resistors for proper termination. Figure 2 shows the LVDS input timing measurement circuit and waveforms. A common-mode level of 1.2V and a differential input swing of $0.8V_{PP}$ is applied to the inputs.

Figure 15 shows a schematic of the equivalent CMOS/TTL-compatible digital inputs of the DAC5675A, valid for the SLEEP pin.

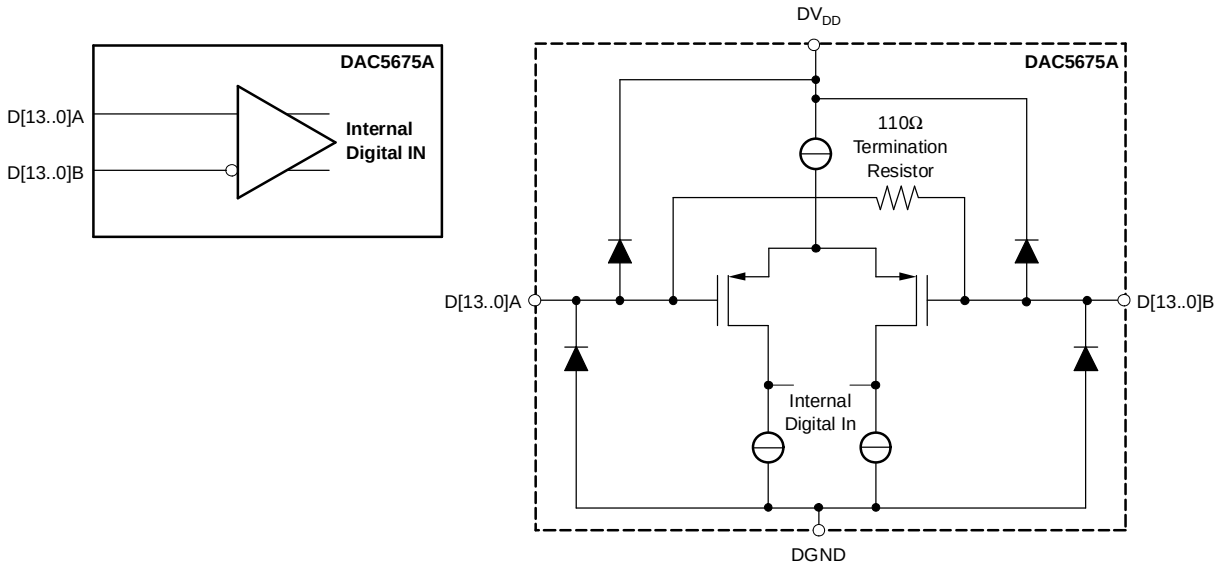


Figure 14. LVDS Digital Equivalent Input

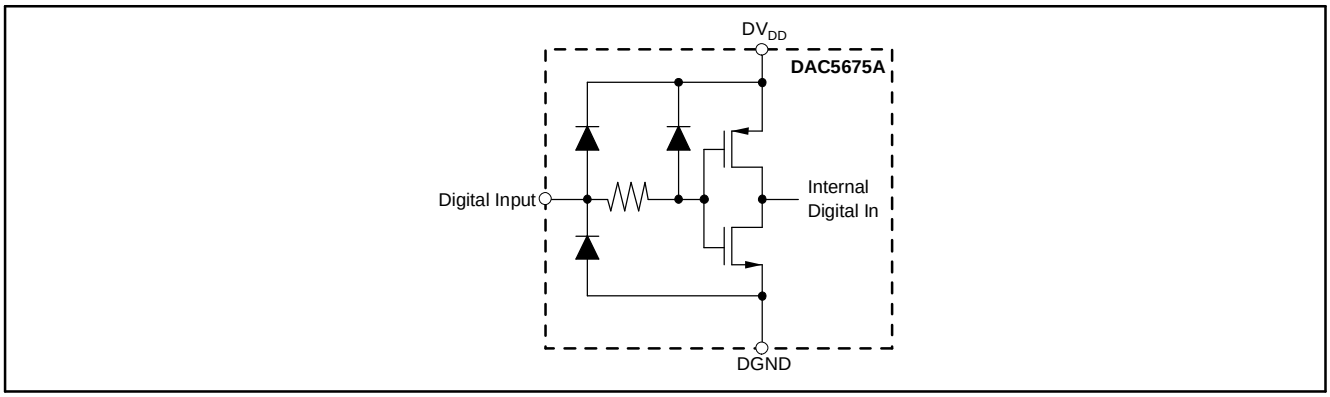


Figure 15. CMOS/TTL Digital Equivalent Input

Clock Input

The DAC5675A features differential, LVPECL compatible clock inputs (CLK, CLKC). Figure 16 shows the equivalent schematic of the clock input buffer. The internal biasing resistors set the input common-mode voltage to approximately 2V, while the input resistance is typically 670Ω. A variety of clock sources can be ac-coupled to the device, including a sine wave source (see Figure 17).

APPLICATION INFORMATION (continued)

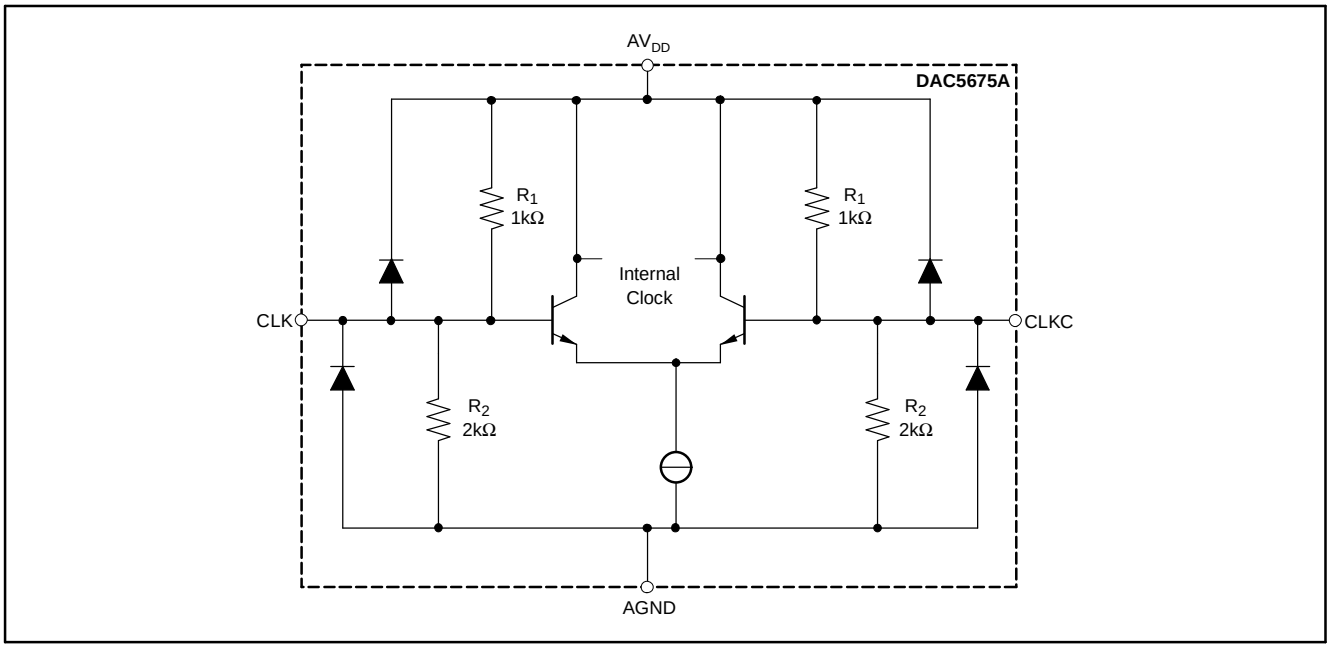


Figure 16. Clock Equivalent Input

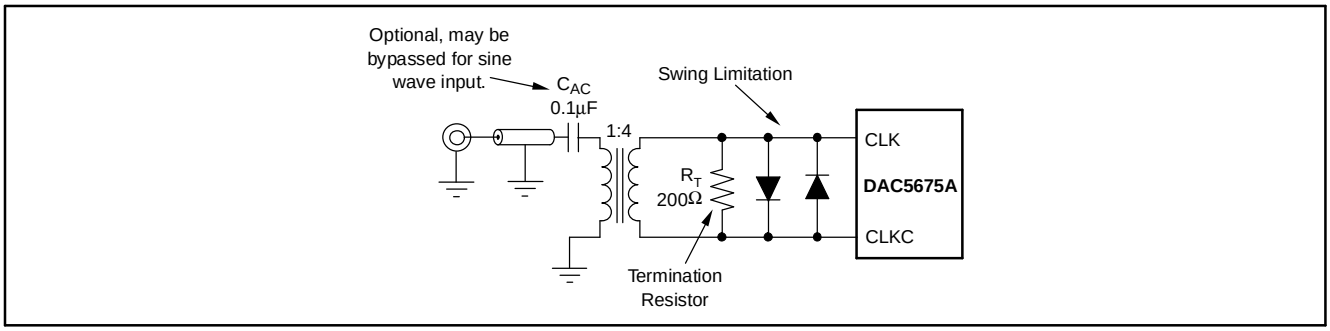


Figure 17. Driving the DAC5675A with a Single-Ended Clock Source Using a Transformer

To obtain best ac performance the DAC5675A clock input should be driven with a differential LVPECL or sine wave source as shown in Figure 18 and Figure 19. Here, the potential of V_{TT} should be set to the termination voltage required by the driver along with the proper termination resistors (R_T). The DAC5675A clock input can also be driven single-ended; this is shown in Figure 20.

APPLICATION INFORMATION (continued)

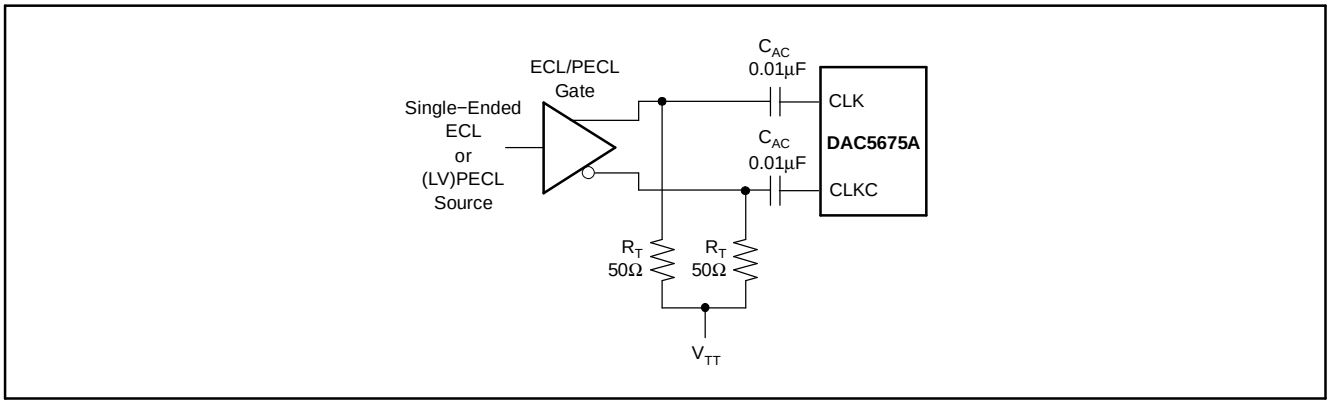


Figure 18. Driving the DAC5675A with a Single-Ended ECL/PECL Clock Source

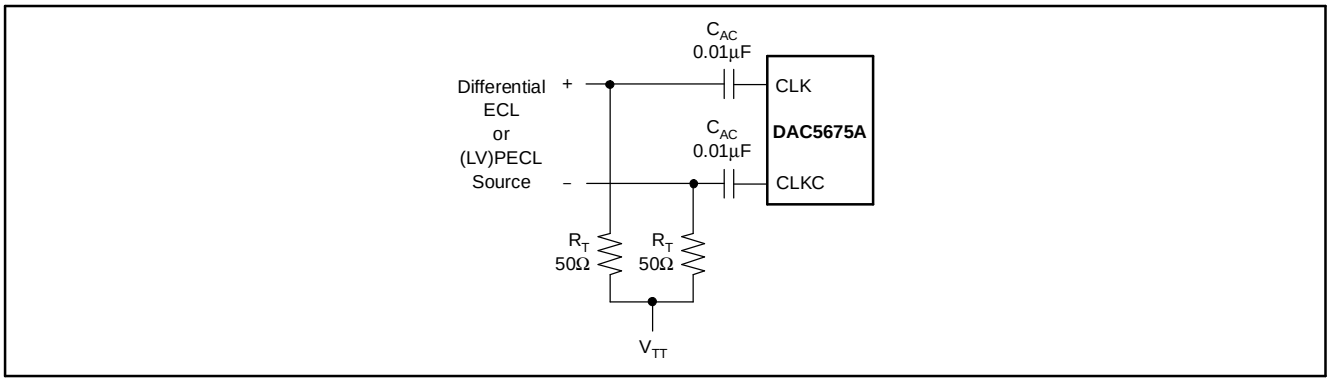


Figure 19. Driving the DAC5675A with a Differential ECL/PECL Clock Source

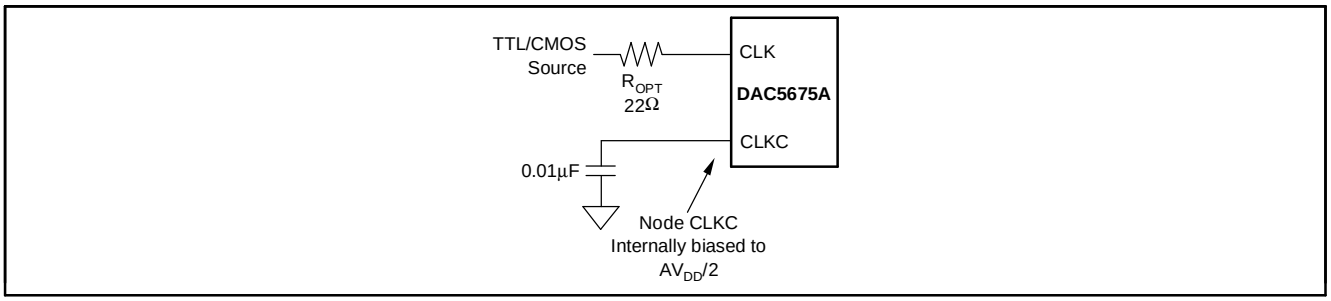


Figure 20. Driving the DAC5675A with a Single-Ended TTL/CMOS Clock Source

APPLICATION INFORMATION (continued)

Supply Inputs

The DAC5675A comprises separate analog and digital supplies, that is, AV_{DD} and DV_{DD}, respectively. These supply inputs can be set independently from 3.6V down to 3.15V.

DAC Transfer Function

The DAC5675A has a current sink output. The current flow through IOUT1 and IOUT2 is controlled by D[13:0]A and D[13:0]B. For ease of use, we denote D[13:0] as the logical bit equivalent of D[13:0]A and its complement D[13:0]B. The DAC5675A supports straight binary coding with D13 being the MSB and D0 the LSB. Full-scale current flows through IOUT2 when all D[13:0] inputs are set high and through IOUT1 when all D[13:0] inputs are set low. The relationship between IOUT1 and IOUT2 can be expressed asEquation 1:

$$IOUT1 = IO_{(FS)} - IOUT2 \quad (1)$$

$IO_{(FS)}$ is the full-scale output current sink (2mA to 20mA). Since the output stage is a current sink, the current can only flow from AV_{DD} through the load resistors R_L into the IOUT1 and IOUT2 pins.

The output current flow in each pin driving a resistive load can be expressed as shown in Figure 21, as well as in Equation 2 and Equation 3.

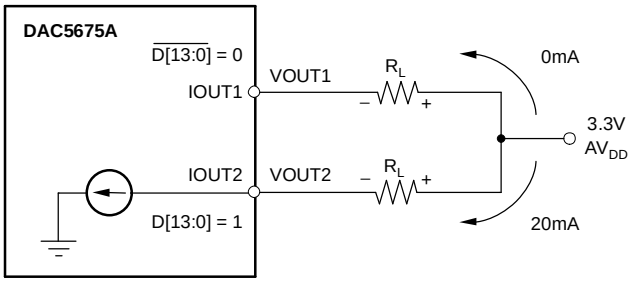


Figure 21. Relationship Between D[13:0], IOUT1 and IOUT2

$$IOUT1 = \frac{IO_{(FS)} \times (16383 - CODE)}{16384} \quad (2)$$

$$IOUT2 = \frac{IO_{(FS)} \times CODE}{16384} \quad (3)$$

where CODE is the decimal representation of the DAC input word. This would translate into single-ended voltages at IOUT1 and IOUT2, as shown in Equation 4 and Equation 5:

$$VOUT1 = AVDD - IOUT1 \times R_L \quad (4)$$

$$VOUT2 = AVDD - IOUT2 \times R_L \quad (5)$$

Assuming that D[13:0] = 1 and the R_L is 50Ω, the differential voltage between pins IOUT1 and IOUT2 can be expressed as shown in Equation 6 through Equation 8:

$$VOUT1 = 3.3V - 0mA \times 50 = 3.3V \quad (6)$$

$$VOUT2 = AVDD - 20mA \times 50 = 2.3V \quad (7)$$

$$VDIFF = VOUT1 - VOUT2 = 1V \quad (8)$$

If D[13:0] = 0, then IOUT2 = 0mA and IOUT1 = 20mA and the differential voltage VDIFF = –1V.

The output currents and voltages in IOUT1 and IOUT2 are complementary. The voltage, when measured differentially, will be doubled compared to measuring each output individually. Care must be taken not to exceed the compliance voltages at the IOUT1 and IOUT2 pins in order to keep signal distortion low.

APPLICATION INFORMATION (continued)

Reference Operation

The DAC5675A has a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS}. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The full-scale output current equals 16 times this bias current. The full-scale output current $IO_{(FS)}$ is thus expressed as Equation 9:

$$I_{O(FS)} = 16 \times I_{BIAS} = \frac{16 \times V_{EXTIO}}{R_{BIAS}} \quad (9)$$

where V_{EXTIO} is the voltage at terminal EXTIO. The bandgap reference voltage delivers a stable voltage of 1.2V. This reference can be overridden by applying an external voltage to terminal EXTIO. The bandgap reference can additionally be used for external reference operation. In such a case, an external buffer amplifier with high impedance input should be selected in order to limit the bandgap load current to less than 100nA. The capacitor C_{EXT} may be omitted. Terminal EXTIO serves as either an input or output node. The full-scale output current is adjustable from 20mA down to 2mA by varying resistor R_{BIAS}.

Analog Current Outputs

Figure 22 shows a simplified schematic of the current sink array output with corresponding switches. Differential NPN switches direct the current of each individual NPN current sink to either the positive output node IOUT1 or its complementary negative output node IOUT2. D[13:0] controls the S(N)C current switches and $\overline{D[13:0]}$ controls the S(N) current switches, as explained in the previous ***DAC Transfer Function*** section (see Figure 21). The output impedance is determined by the stack of the current sinks and differential switches, and is > 300kΩ in parallel with an output capacitance of 5pF.

The external output resistors are referred to the positive supply AV_{DD}.

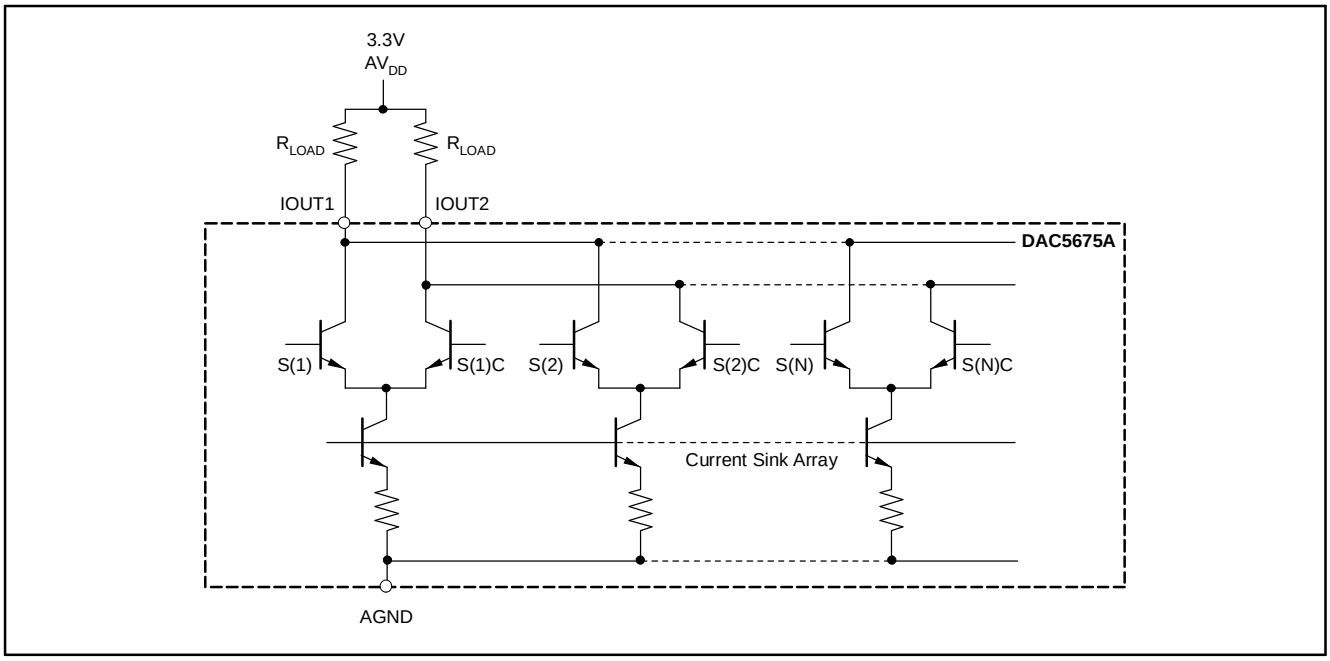


Figure 22. Equivalent Analog Current Output

The DAC5675A can easily be configured to drive a doubly-terminated 50Ω cable using a properly selected transformer. Figure 23 and Figure 24 show the 1:1 and 4:1 impedance ratio configuration, respectively. These configurations provide maximum rejection of common-mode noise sources and even-order distortion components, thereby doubling the power of the DAC to the output. The center tap on the primary side of the transformer is terminated to AV_{DD}, enabling a dc current flow for both IOUT1 and IOUT2. Note that the ac performance of the DAC5675A is optimum and specified using a 1:1 differential transformer-coupled output.

APPLICATION INFORMATION (continued)

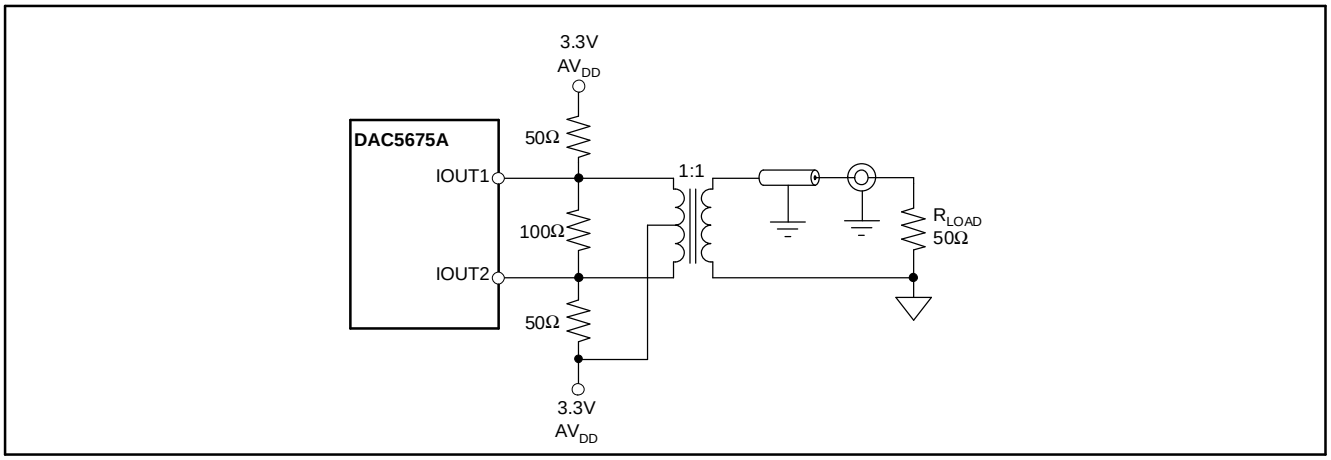


Figure 23. Driving a Doubly-Terminated 50Ω Cable Using a 1:1 Impedance Ratio Transformer

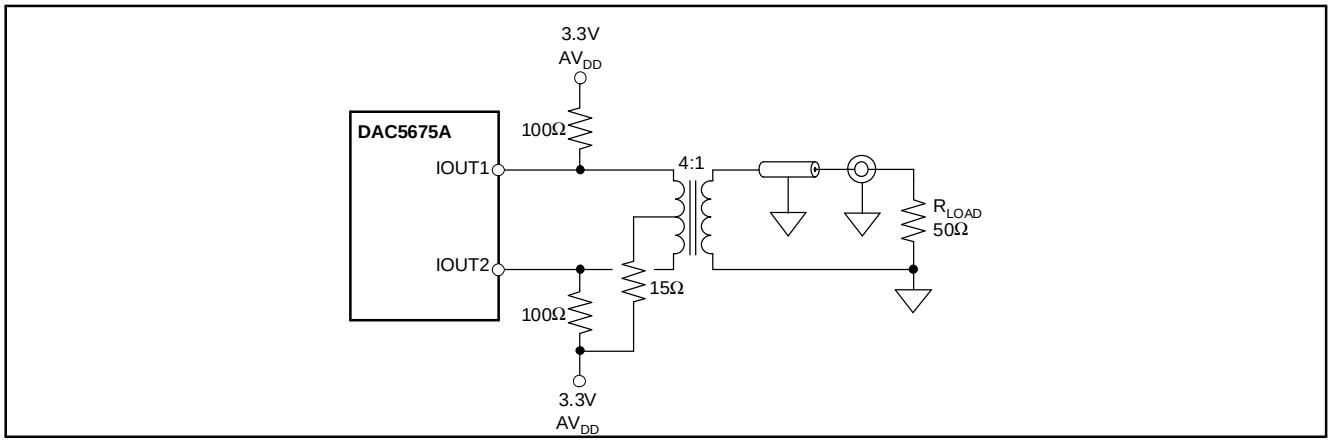


Figure 24. Driving a Doubly-Terminated 50Ω Cable Using a 4:1 Impedance Ratio Transformer

Figure 25(a) shows the typical differential output configuration with two external matched resistor loads. The nominal resistor load of 25Ω gives a differential output swing of $1V_{PP}$ ($0.5–V_{PP}$ single-ended) when applying a 20mA full-scale output current. The output impedance of the DAC5675A slightly depends on the output voltage at nodes IOUT1 and IOUT2. Consequently, for optimum dc-integral nonlinearity, the configuration of Figure 25(b) should be chosen. In this current/voltage (I-V) configuration, terminal IOUT1 is kept at AV_{DD} by the inverting operational amplifier. The complementary output should be connected to AV_{DD} to provide a dc-current path for the current sources switched to IOUT1. The amplifier maximum output swing and the full-scale output current of the DAC determine the value of the feedback resistor (R_{FB}). The capacitor (C_{FB}) filters the steep edges of the DAC5675A current output, thereby reducing the operational amplifier slew-rate requirements. In this configuration, the op amp should operate at a supply voltage higher than the resistor output reference voltage AV_{DD} as a result of its positive and negative output swing around AV_{DD}. Node IOUT1 should be selected if a single-ended unipolar output is desired.

APPLICATION INFORMATION (continued)

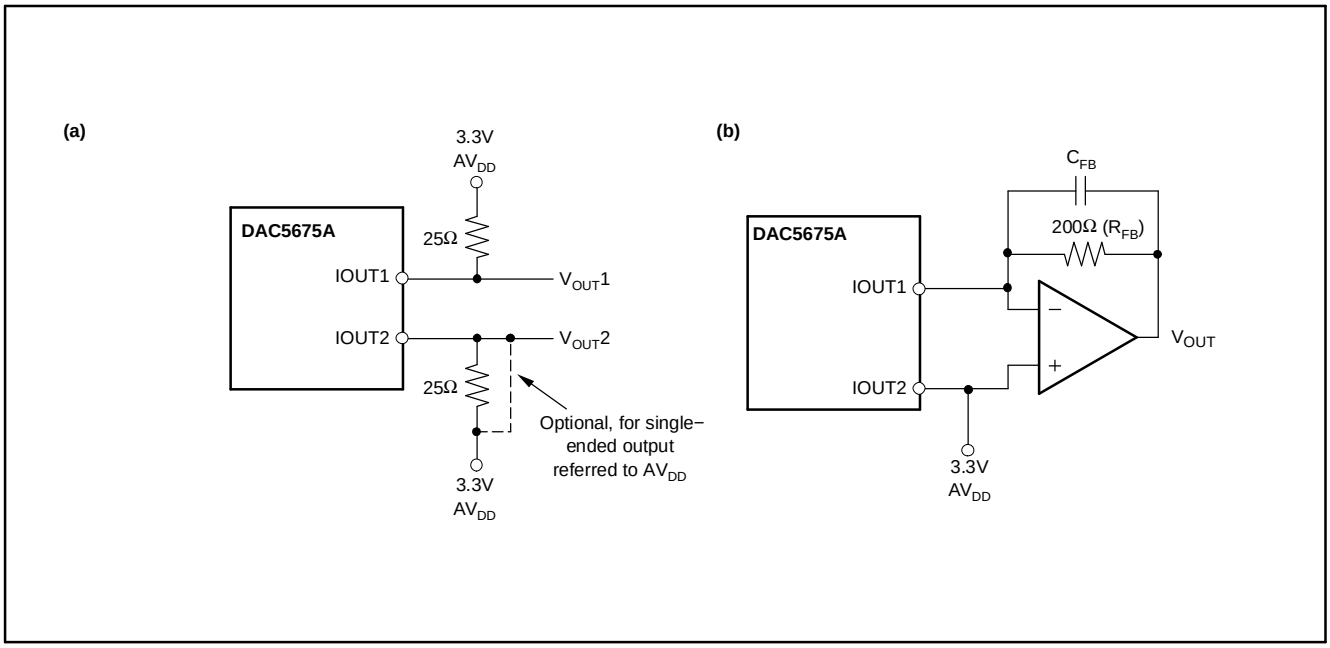


Figure 25. Output Configurations

Sleep Mode

The DAC5675A features a power-down mode that turns off the output current and reduces the supply current to approximately 6mA. The power-down mode is activated by applying a logic level 1 to the SLEEP pin pulled down internally.

Definitions

Definitions of Specifications and Terminology

Gain error is defined as the percentage error in the ratio between the measured full-scale output current and the value of 16 x $V_{(EXTIO)}/R_{BIAS}$. A $V_{(EXTIO)}$ of 1.25V is used to measure the gain error with an external reference voltage applied. With an internal reference, this error includes the deviation of $V_{(EXTIO)}$ (internal bandgap reference voltage) from the typical value of 1.25V.

Offset error is defined as the percentage error in the ratio of the differential output current (IOUT1–IOUT2) and the half of the full-scale output current for input code 8192.

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental output signal.

SNR is the ratio of the rms value of the fundamental output signal to the rms sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

SINAD is the ratio of the rms value of the fundamental output signal to the rms sum of all other spectral components below the Nyquist frequency, including noise and harmonics, but excluding dc.

ACPR or adjacent channel power ratio is defined for a 3.84Mcps 3GPP W-CDMA input signal measured in a 3.84MHz bandwidth at a 5MHz offset from the carrier with a 12dB peak-to-average ratio.

APSSR or analog power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the analog power supply AV_{DD} from the nominal. This is a dc measurement.

DPSSR or digital power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the digital power supply DV_{DD} from the nominal. This is a dc measurement.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
DAC5675AIPHP	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260
DAC5675AIPHPG4	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260
DAC5675AIPHPR	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260
DAC5675AIPHPRG4	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF DAC5675A :

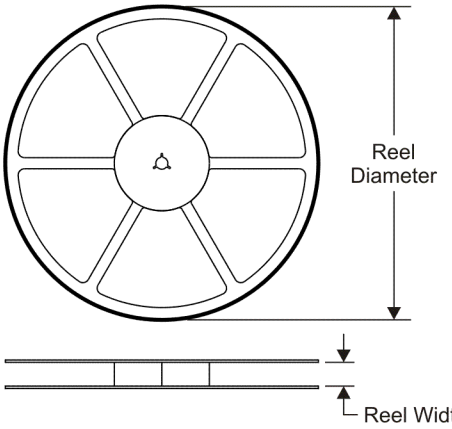
- Space: DAC5675A-SP

NOTE: Qualified Version Definitions:

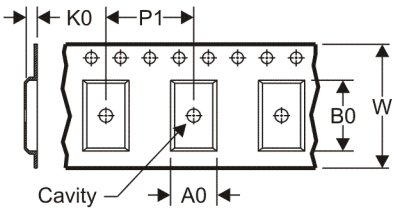
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

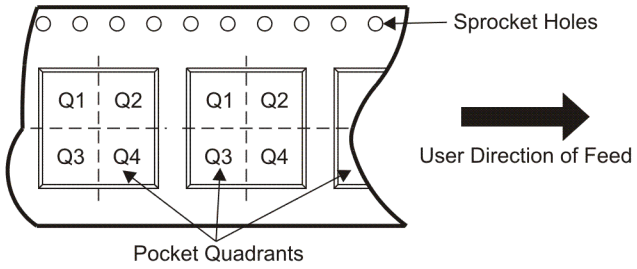


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

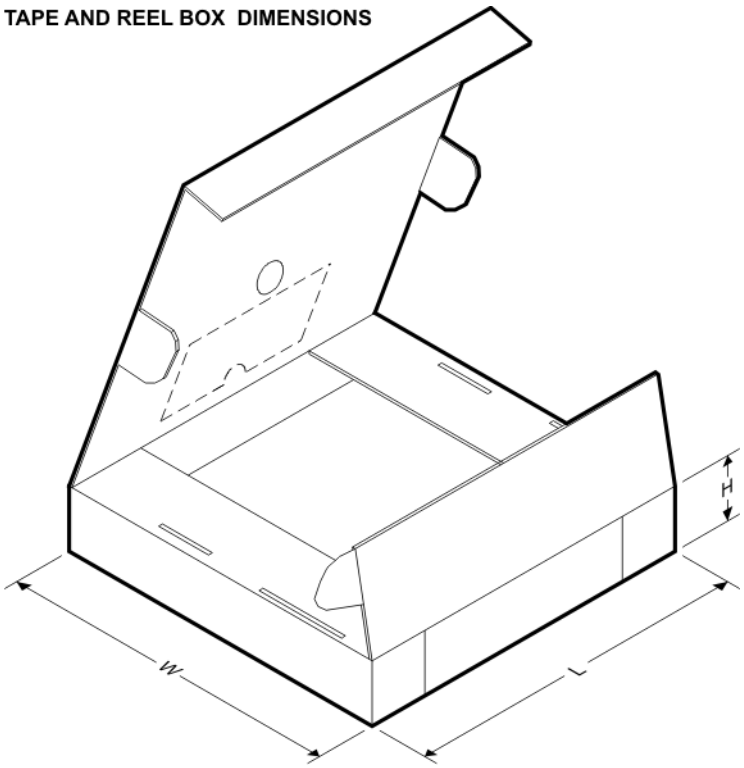
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5675AIPHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

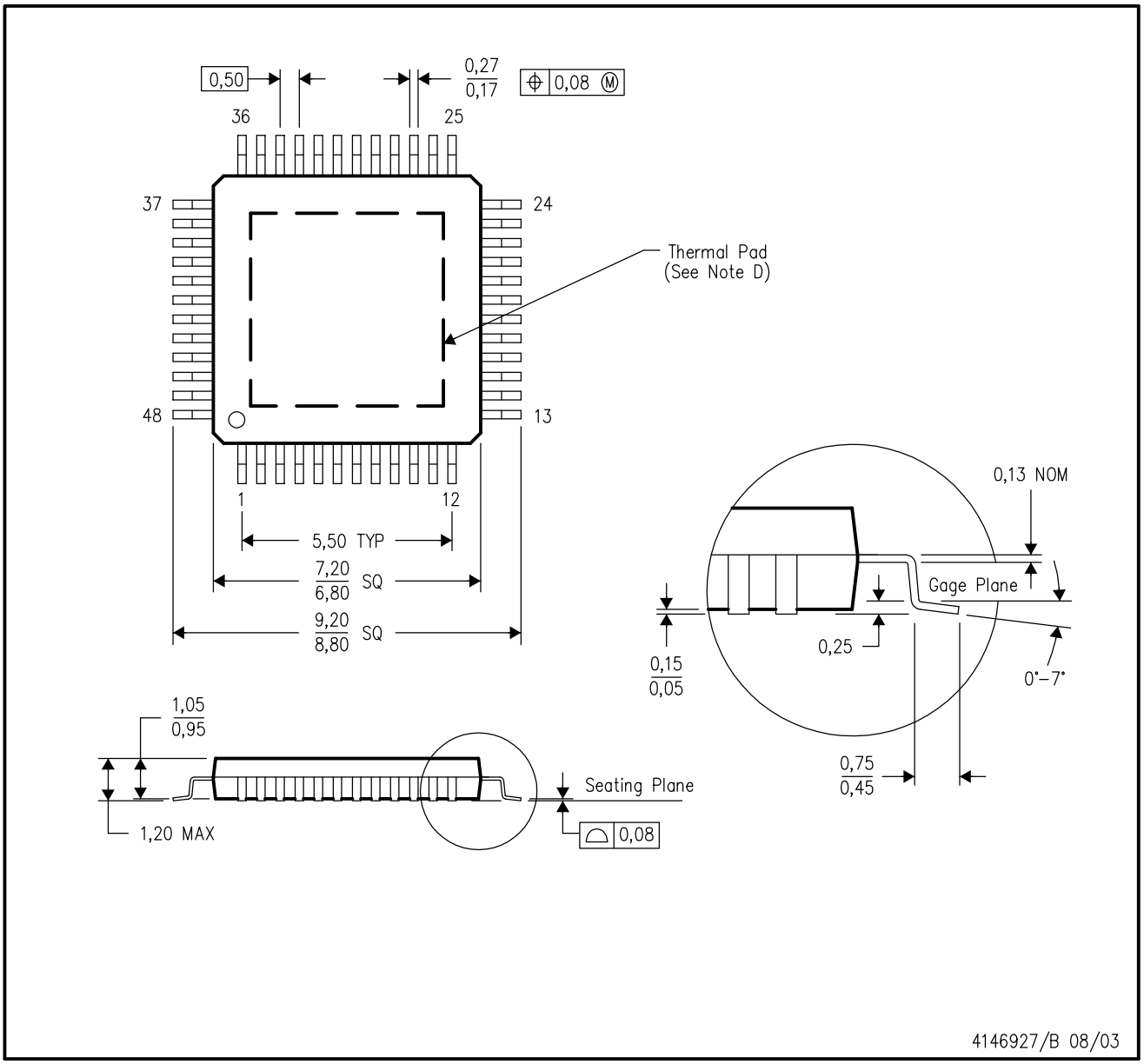
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5675AIPHPR	HTQFP	PHP	48	1000	346.0	346.0	33.0

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

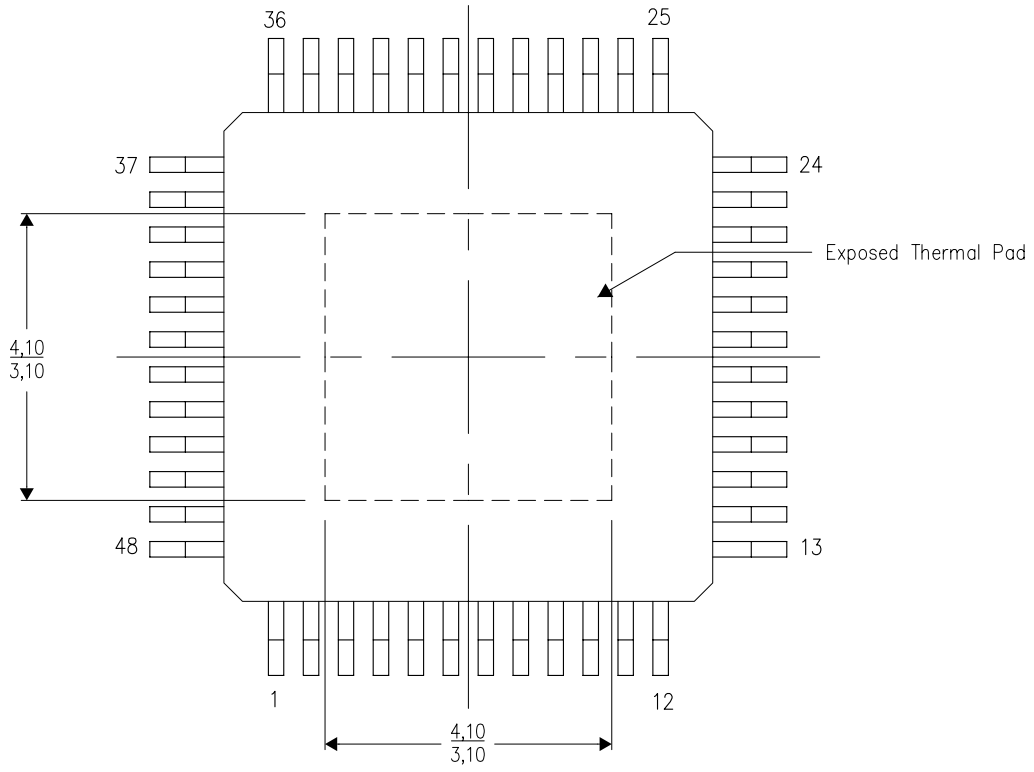
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206329–3/L 10/10

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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