

查询"74HC374D"供应商

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I²C category: MSI

GENERAL DESCRIPTION

The 74HC/HCT374 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT374 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications.

A clock (CP) and an output enable (\overline{OE}) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When \overline{OE} is LOW, the contents of the 8 flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

The "374" is functionally identical to the "534", but has non-inverting outputs.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|---|---|---------|-----|------|
| | | | HC | HCT | |
| t_{PHL}/t_{PLH} | propagation delay CP to Q_n | $C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$ | 15 | 13 | ns |
| f_{max} | maximum clock frequency | | 77 | 48 | MHz |
| C_I | input capacitance | | 3.5 | 3.5 | pF |
| CPD | power dissipation capacitance per flip-flop | notes 1 and 2 | 17 | 17 | pF |

GND = 0 V; $T_{amb} = 25 \text{ }^\circ\text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF
 f_o = output frequency in MHz V_{CC} = supply voltage in V

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
 For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

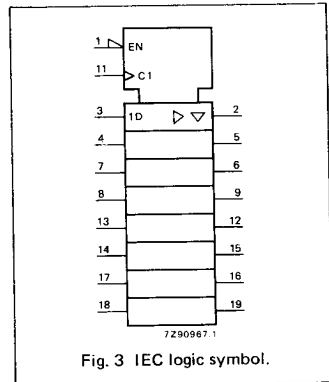
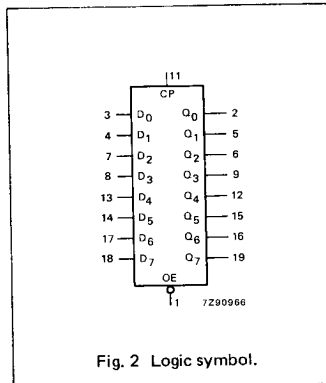
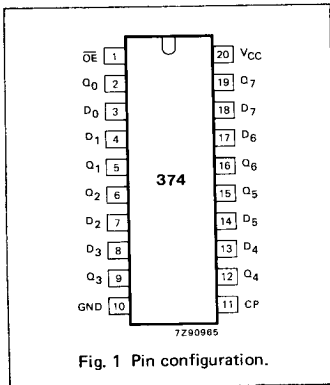
PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

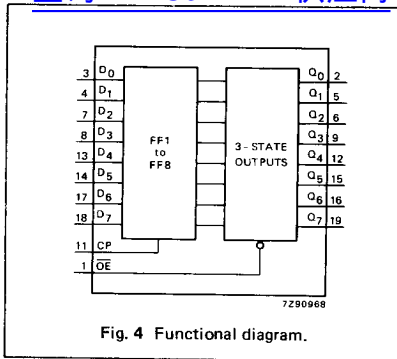
20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|----------------------------|-----------------|---|
| 1 | \overline{OE} | 3-state output enable input (active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q_0 to Q_7 | 3-state flip-flop outputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | D_0 to D_7 | data inputs |
| 10 | GND | ground (0 V) |
| 11 | CP | clock input (LOW-to-HIGH, edge-triggered) |
| 20 | V_{CC} | positive supply voltage |



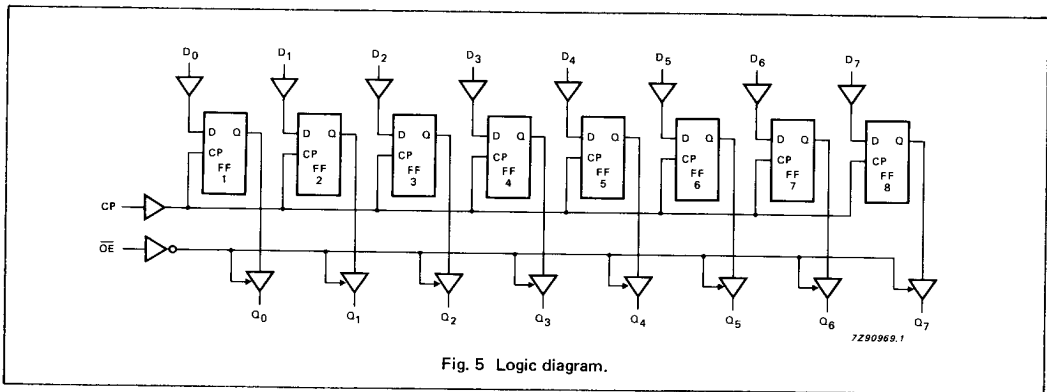
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FUNCTION TABLE

| OPERATING MODES | INPUTS | | | INTERNAL FLIP-FLOPS | OUTPUTS Q ₀ to Q ₇ |
|-----------------------------------|--------|--------|----------------|---------------------|---|
| | OE | CP | D _n | | |
| load and read register | L L | ↑ ↑ | l h | L H | L H |
| load register and disable outputs | H H | ↑ ↑ | l h | L H | Z Z |

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition



[查询"74HC374D-T"供应商](#)**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|--|---|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------------|-------------------|--------|
| | | 74HC | | | | | | | V _{CC} V | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay CP to Q _n | | 50 18 14 | 165 33 28 | | 205 41 35 | | 250 50 43 | ns | 2.0 4.5 6.0 | Fig. 6 |
| t _{PZH} / t _{PZL} | 3-state output enable time OE to Q _n | | 41 15 12 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig. 7 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time OE to Q _n | | 50 18 14 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig. 7 |
| t _{THL} / t _{TLH} | output transition time | | 14 5 4 | 60 12 10 | | 75 15 13 | | 90 18 15 | ns | 2.0 4.5 6.0 | Fig. 6 |
| t _W | clock pulse width HIGH or LOW | 80 16 14 | 19 7 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig. 6 |
| t _{SU} | set-up time D _n to CP | 60 12 10 | 14 5 4 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig. 8 |
| t _H | hold time D _n to CP | 5 5 5 | -6 -2 -2 | | 5 5 5 | | 5 5 5 | | ns | 2.0 4.5 6.0 | Fig. 8 |
| f _{max} | maximum clock pulse frequency | 6.0 30 35 | 23 70 83 | | 4.8 24 28 | | 4.0 20 24 | | MHz | 2.0 4.5 6.0 | Fig. 6 |

[查询"74HC374D-T"供应商](#)**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| \overline{OE} | 1.25 |
| CP | 0.90 |
| D _n | 0.35 |

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|--|--|-----------------------|------|------|------------|------|-------------|------|----------------------|-----------|--------|
| | | 74HCT | | | | | | | V _{CC} V | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay CP to Q _n | | 16 | 32 | | 40 | | 48 | ns | 4.5 | Fig. 6 |
| t _{PZH} / t _{PZL} | 3-state output enable time \overline{OE} to Q _n | | 16 | 30 | | 38 | | 45 | ns | 4.5 | Fig. 7 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time \overline{OE} to Q _n | | 18 | 28 | | 35 | | 42 | ns | 4.5 | Fig. 7 |
| t _{THL} / t _{TLH} | output transition time | | 5 | 12 | | 15 | | 18 | ns | 4.5 | Fig. 6 |
| t _W | clock pulse width HIGH or LOW | 19 | 11 | | 24 | | 29 | | ns | 4.5 | Fig. 6 |
| t _{su} | set-up time D _n to CP | 12 | 7 | | 15 | | 18 | | ns | 4.5 | Fig. 8 |
| t _h | hold time D _n to CP | 5 | -3 | | 5 | | 5 | | ns | 4.5 | Fig. 8 |
| f _{max} | maximum clock pulse frequency | 26 | 44 | | 21 | | 17 | | MHz | 4.5 | Fig. 6 |

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AC WAVEFORMS

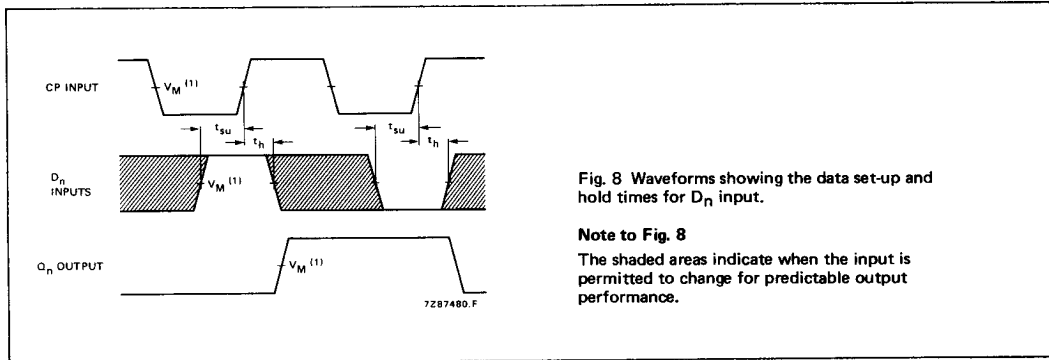
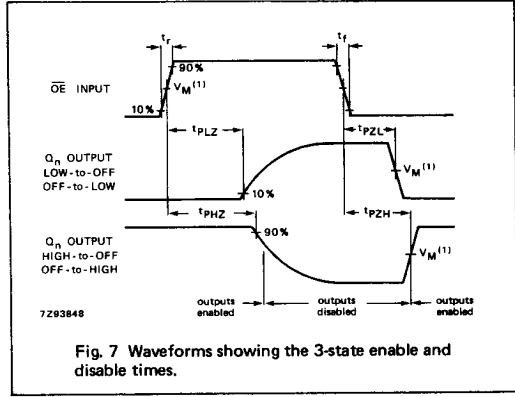
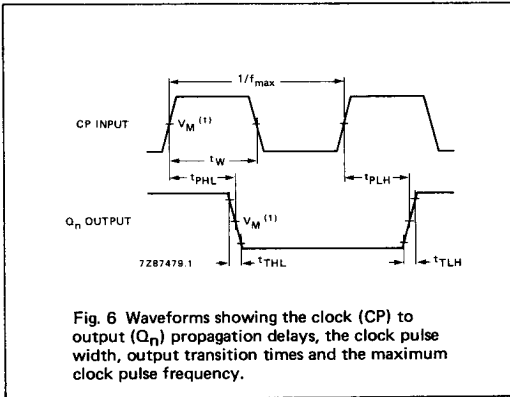


Fig. 8 Waveforms showing the data set-up and hold times for D_n input.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
- HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.