

MC10E212, MC100E212

5V ECL 3-Bit Scannable Registered Address Driver

The MC10E/100E212 is a scannable registered ECL driver typically used as a fan-out memory address driver for ECL cache driving. In a VLSI array based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

The 100 Series contains temperature compensation.

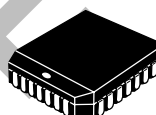
- Scannable Version E112 Driver
- 1025 ps Max. CLK to Output
- Dual Differential Outputs
- Master Reset
- PECL Mode Operating Range: $V_{CC} = 4.2\text{ V}$ to 5.7 V with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -4.2\text{ V}$ to -5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: $> 1\text{ KV HBM}$, $> 75\text{ V MM}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 259 devices



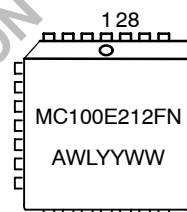
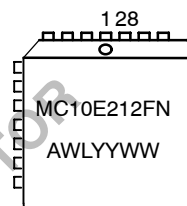
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MARKING DIAGRAMS



PLCC-28
FN SUFFIX
CASE 776



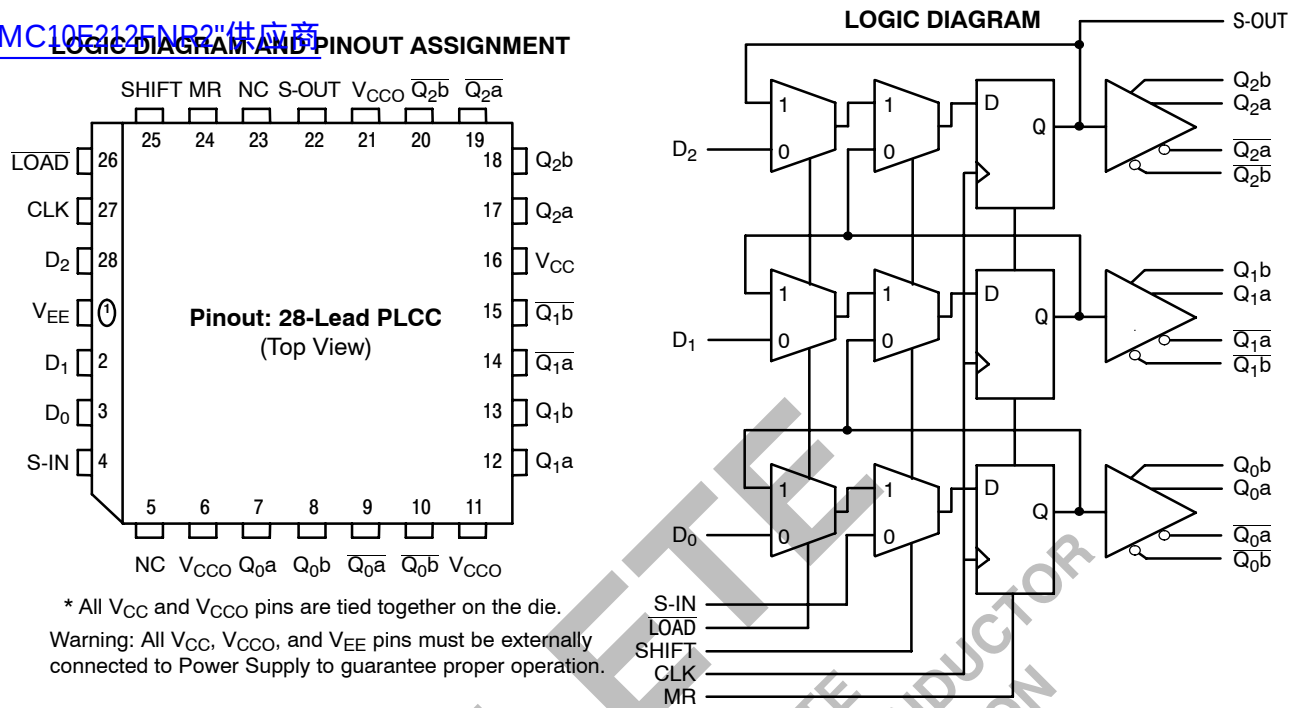
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E212FN	PLCC-28	37 Units/Rail
MC10E212FNR2	PLCC-28	500 Units/Reel
MC100E212FN	PLCC-28	37 Units/Rail
MC100E212FNR2	PLCC-28	500 Units/Reel

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PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_2$	ECL Data Inputs
S-IN	ECL Scan Input
LOAD	ECL LOAD/HOLD Control
SHIFT	ECL Scan Control
CLK	ECL Clock
MR	ECL Reset
S-OUT	ECL Scan Output
$Q[0:2]a$, $Q[0:2]b$	ECL True Outputs
$\overline{Q}[0:2]a$, $\overline{Q}[0:2]b$	ECL Inverting Outputs
V_{CC} , V_{CC0}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

LOAD	SHIFT	MR	MODE
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

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MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-8	V
V _I	PECL Mode Input Voltage	V _{EE} = 0 V	V _I ≤ V _{CC}	6	V
	NECL Mode Input Voltage	V _{CC} = 0 V	V _I ≥ V _{EE}	-6	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			0 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V _{EE}	PECL Operating Range			4.2 to 5.7	V
	NECL Operating Range			-5.7 to -4.2	V
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		80	96		80	96		80	96	mA
V _{OH}	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V _{OL}	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V _{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V _{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / -0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = -5.0 V (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		80	96		80	96		80	96	mA
V _{OH}	Output HIGH Voltage (Note 2)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
V _{OL}	Output LOW Voltage (Note 2)	-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
V _{IH}	Input HIGH Voltage	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
V _{IL}	Input LOW Voltage	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / -0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.

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100E SERIES PECL DC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		80	96		80	96		92	110	mA
V_{OH}	Output HIGH Voltage (Note 2)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.46 V / -0.8 V.

2. Outputs are terminated through a 50 ohm resistor to V_{CC} -2 volts.

100E SERIES NECL DC CHARACTERISTICS $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		80	96		80	96		92	110	mA
V_{OH}	Output HIGH Voltage (Note 2)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
V_{OL}	Output LOW Voltage (Note 2)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
V_{IH}	Input HIGH Voltage	-1165	-950	-880	-1165	-880	-880	-1165	-880	-880	mV
V_{IL}	Input LOW Voltage	-1810	-1700	-1475	-1810	-1475	-1475	-1810	-1475	-1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.46 V / -0.8 V.

2. Outputs are terminated through a 50 ohm resistor to V_{CC} -2 volts.

AC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK MR CLK to S-OUT	575 575 575	800 800 800	1025 1025 1025	575 575 575	800 800 800	1025 1025 1025	575 575 575	800 800 800	1025 1025 1025	ps
t_s	Setup Time D SHIFT LOAD S-IN	175 150 225 150	25 - 50 50 - 50		175 150 225 150	25 - 50 50 - 50		175 150 225 150	25 - 50 50 - 50		ps
t_h	Hold Time D SHIFT LOAD S-IN	250 300 225 300	25 100 0 100		250 300 225 300	25 100 0 100		250 300 225 300	25 100 0 100		ps
t_{RR}	Reset Recovery	600	350		600	350		600	350		ps
t_{SKEW}	Within-Device Skew (Note 1.)		100			100			100		ps
t_{SKEW}	Within-Gate Skew (Note 2.)		50			50			50		ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times (20 - 80%)	275	425	650	275	425	650	275	425	650	ps

1. 10 Series: V_{EE} can vary +0.46 V / -0.06 V.

100 Series: V_{EE} can vary +0.46 V / -0.8 V.

1. Within-device skew is defined as identical transitions on similar paths through a device.

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2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

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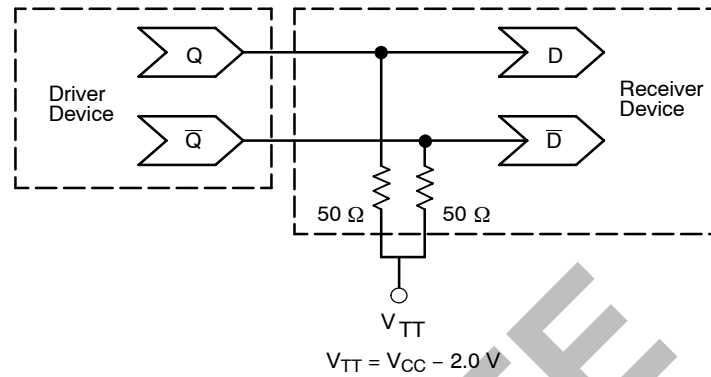


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

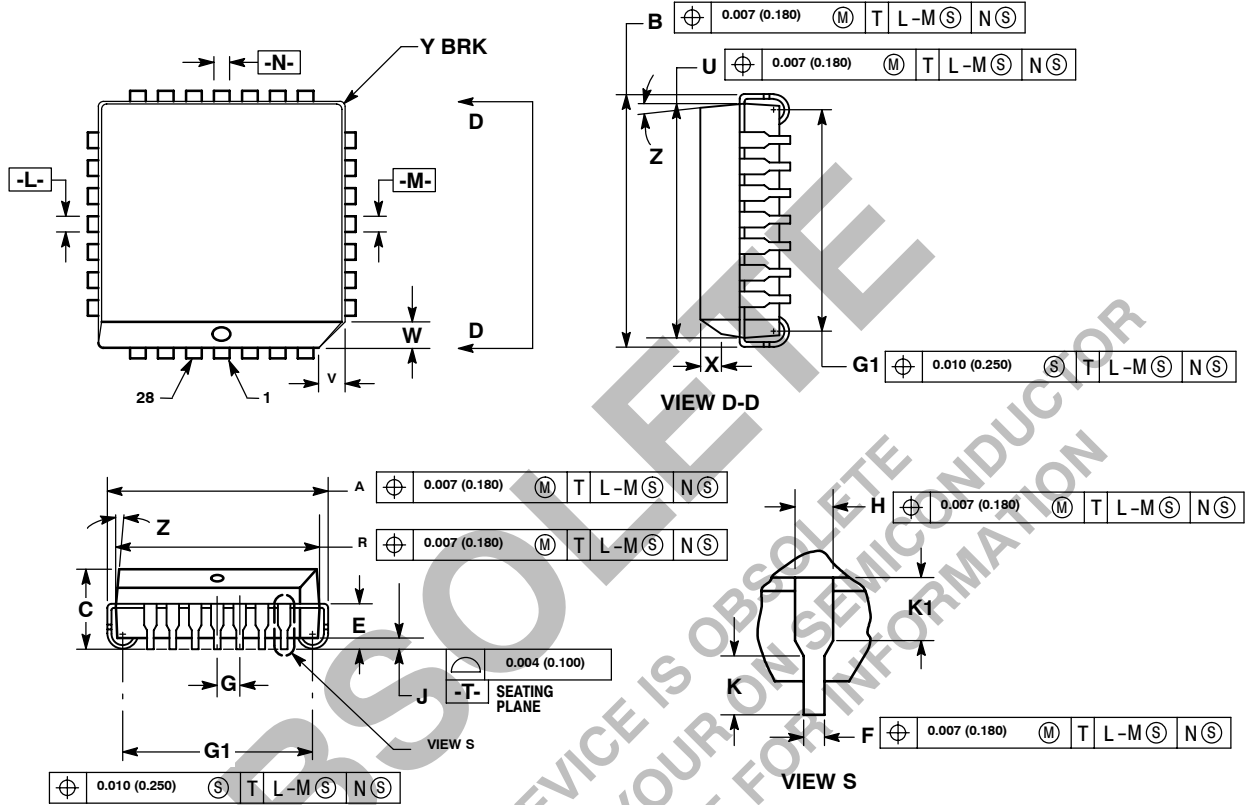
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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