OKI Semiconductor

This version: Jan. 1998
Previous version: Dec. 1996

MSM5416125A

131,072-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The OKI MSM5416125A is a 128K-word × 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM5416125A achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM5416125A has conventional two $\overline{CAS}$ type 256K × 16 DRAM compatible pinout. The MSM5416125A is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP.

FEATURES

- Fast Page Mode Operation
- Byte wide control: 2 $\overline{CAS}$ control
- 131,072-word × 16-bit organization
- Pin compatible with 2 $\overline{CAS}$ type 256K × 16 DRAM
- Single 5 V power supply, ±10% tolerance
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- Refresh: 512 cycles/8 ms
- Package options:

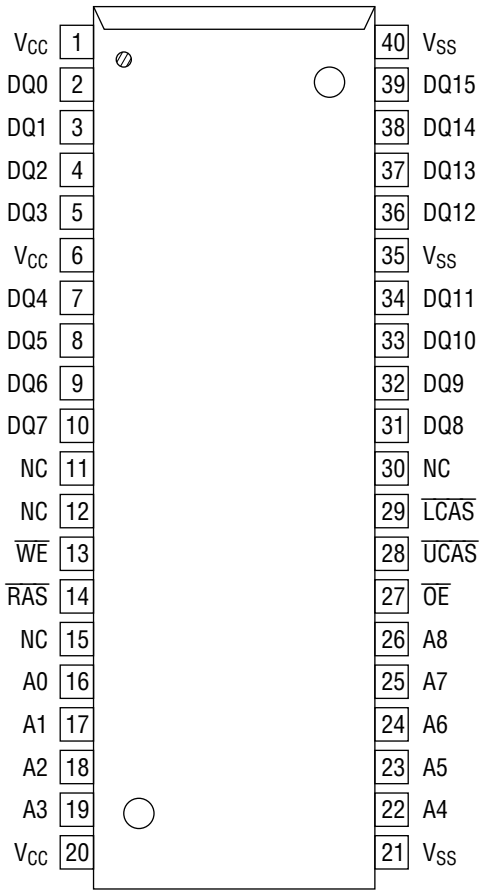
40-pin 400 mil plastic SOJ	(SOJ40-P-400-1.27)	(Product : MSM5416125A-xxJS)
44/40-pin 400 mil plastic TSOP (Type II)	(TSOPII44/40-P-400-0.80-K)	(Product : MSM5416125A-xxTS-K)

xx indicates speed rank.

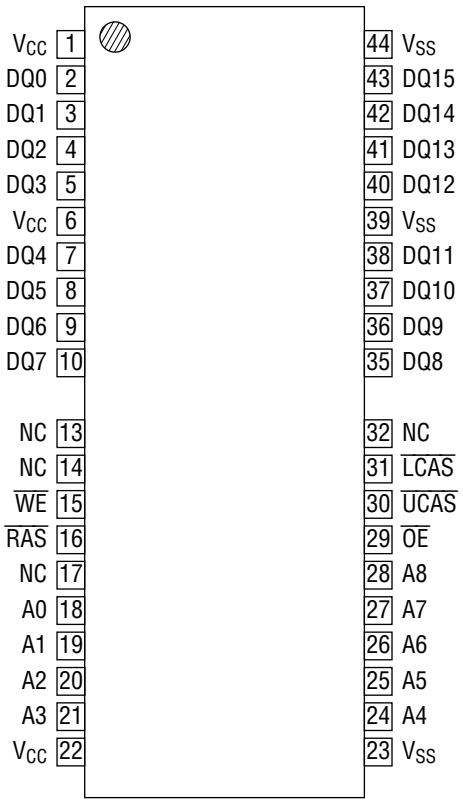
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}	t_{RC}	Operating (Max.)	Standby (Max.)
MSM5416125A-40	40 ns	22 ns	14 ns	14 ns	80 ns	770 mW	11 mW
MSM5416125A-45	45 ns	24 ns	14 ns	14 ns	90 ns	715 mW	
MSM5416125A-50	50 ns	26 ns	14 ns	14 ns	100 ns	660 mW	
MSM5416125A-60	60 ns	30 ns	15 ns	15 ns	120 ns	605mW	

PIN CONFIGURATION (TOP VIEW)



40-Pin Plastic SOJ

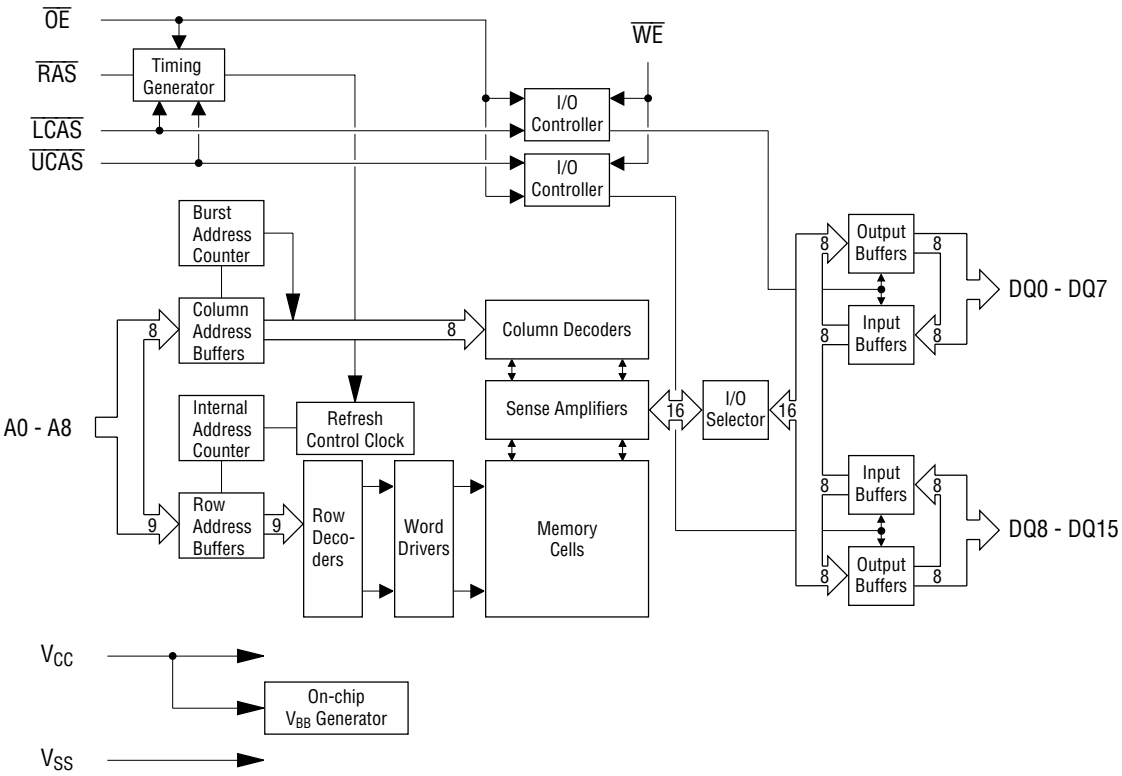


44/40-Pin Plastic TSOP (II)
(K Type)

Pin Name	Function
A0 - A8	Address Input Row Address : A0 - A8 Column Address : A0 - A7
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$	Lower Byte Column Address Strobe
$\overline{UCAS}$	Upper Byte Column Address Strobe
DQ0 - DQ15	Data - Input / Data - Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (5 V)
V_{SS}	Ground (0 V)
NC	No Connection

Note: The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ0 - DQ7	DQ8 - DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

* : "H" or "L"

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	Ta = 25°C	–1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	–55 to 150	°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ0 - DQ15)	$C_{I/O}$	—	10	pF

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM5416125A -40		MSM5416125A -45		MSM5416125A -50		MSM5416125A -60		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –1.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 1.0 mA	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ 6.5 V ; All other pins not under test = 0 V	–10	10	–10	10	–10	10	–10	10	µA	
Output Leakage Current	I_{LO}	DQi Disable 0 V ≤ V_O ≤ 5.5 V	–10	10	–10	10	–10	10	–10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = Min.	—	140	—	130	—	120	—	110	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	—	2	—	2	—	2	mA	1
Average Power Supply Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ = Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	140	—	130	—	120	—	110	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	—	5	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ = Cycling, $\overline{CAS}$ before $\overline{RAS}$	—	140	—	130	—	120	—	110	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = Min.	—	130	—	130	—	120	—	110	mA	1, 3

Notes : 1. Specified values are obtained with output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5416125A -40		MSM5416125A -45		MSM5416125A -50		MSM5416125A -60		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	80	—	90	—	100	—	120	—	ns	
Read Modify Write Cycle Time	t_{RWC}	115	—	130	—	145	—	165	—	ns	
Fast Page Mode Cycle Time	t_{PC}	28	—	30	—	31	—	33	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	60	—	60	—	65	—	80	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	40	—	45	—	50	—	60	ns	4, 9, 10
Access Time from $\overline{CAS}$	t_{CAC}	—	14	—	14	—	14	—	15	ns	4, 9
Access Time from Column Address	t_{AA}	—	22	—	24	—	26	—	30	ns	4, 10
Access Time from $\overline{OE}$	t_{OEA}	—	14	—	14	—	14	—	15	ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	27	—	27	—	29	—	34	ns	4, 9, 10
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	0	—	ns	
Output Buffer Turn-off Delay Time	t_{OFF}	3	8	3	8	3	8	3	10	ns	5
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	3	8	3	8	3	8	3	10	ns	5
Transition Time	t_T	2	35	2	35	2	35	2	35	ns	
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	30	—	35	—	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	40	10,000	45	10,000	50	10,000	60	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	40	100,000	45	100,000	50	100,000	60	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	14	—	14	—	14	—	15	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	8	—	8	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	6	—	6	—	7	—	8	—	ns	14
$\overline{CAS}$ Pulse Width	t_{CAS}	14	10,000	14	10,000	14	10,000	15	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	—	45	—	50	—	60	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	5	—	ns	12
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	18	26	18	31	20	36	20	45	ns	9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	13	18	13	21	15	24	15	30	ns	10
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	8	—	8	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	11
Column Address Hold Time	t_{CAH}	6	—	6	—	8	—	10	—	ns	11
Column Address Hold Time from $\overline{RAS}$	t_{AR}	30	—	30	—	35	—	45	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	22	—	24	—	26	—	30	—	ns	

AC Characteristics (2/2)

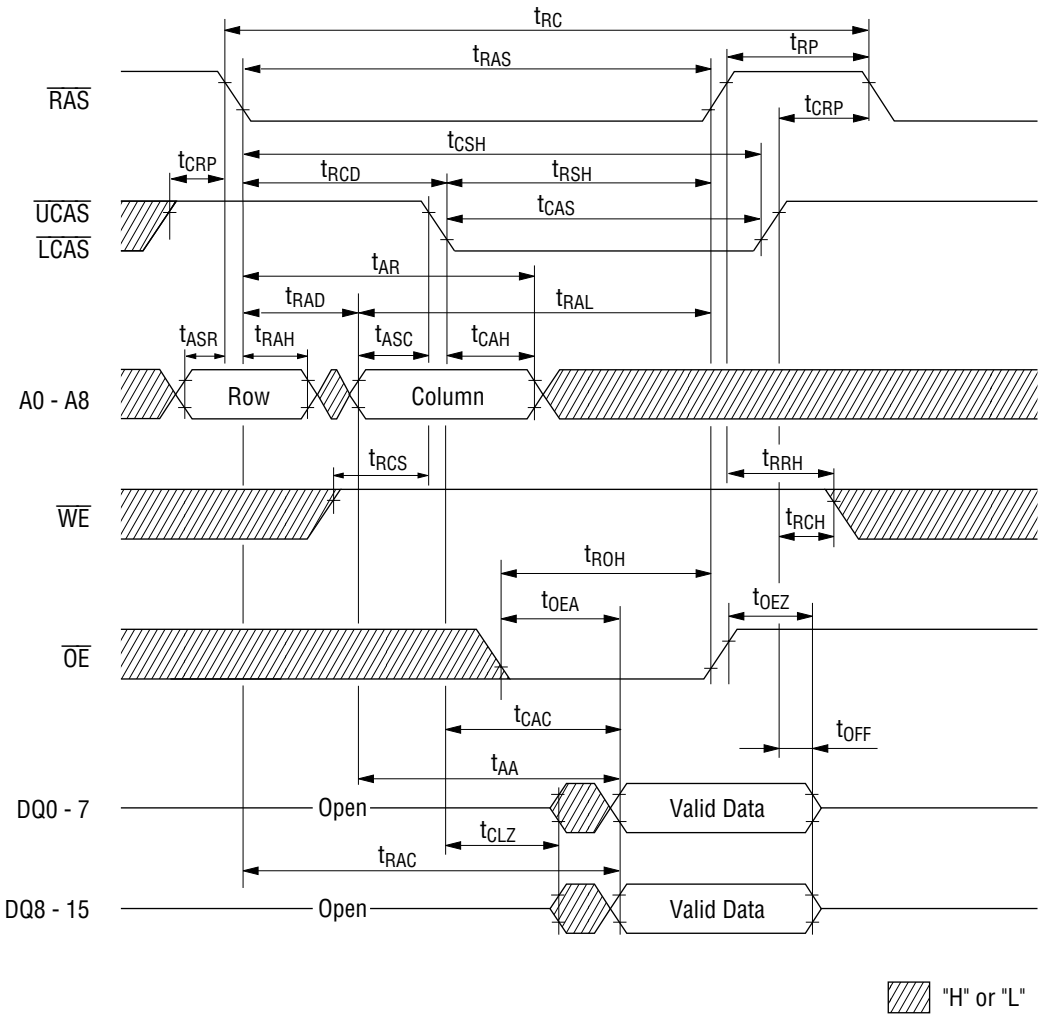
(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5416125A -40		MSM5416125A -45		MSM5416125A -50		MSM5416125A -60		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	11
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	6, 11
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	6
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	8, 11
Write Command Hold Time	t_{WCH}	8	—	8	—	9	—	10	—	ns	11
Write Command Pulse Width	t_{WP}	7	—	8	—	9	—	10	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	30	—	30	—	35	—	45	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	8	—	8	—	9	—	10	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	7	—	8	—	9	—	12	—	ns	13
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	14	—	14	—	14	—	15	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	0	—	ns	7, 11
Data-in Hold Time	t_{DH}	7	—	8	—	9	—	10	—	ns	7, 11
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	30	—	30	—	35	—	45	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	8	—	8	—	8	—	10	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	28	—	30	—	32	—	35	—	ns	8
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	38	—	40	—	44	—	50	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	—	65	—	70	—	80	—	ns	8
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	0	—	0	—	0	—	0	—	ns	11
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	10	—	ns	11
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	10	—	10	—	10	—	ns	12

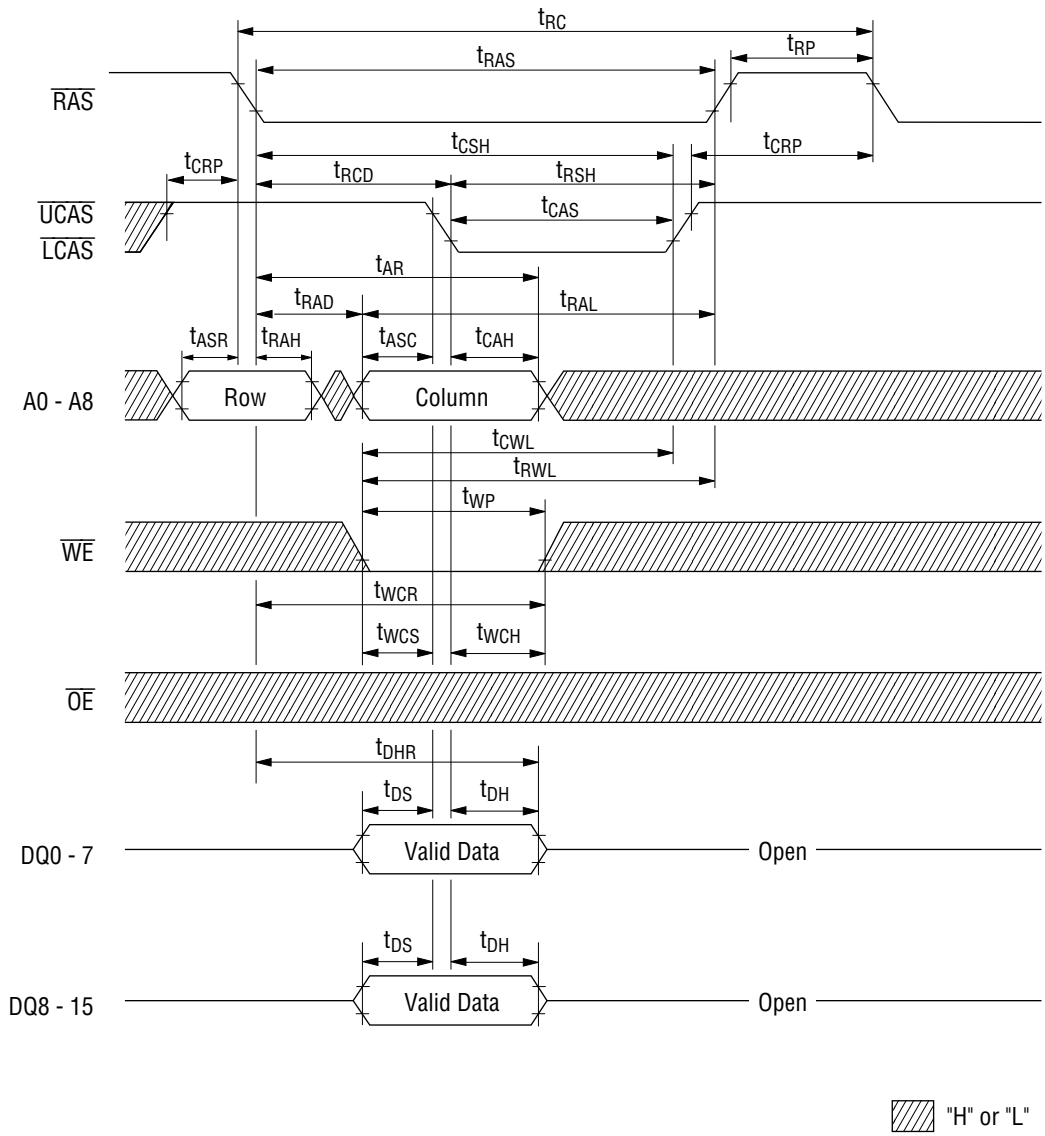
Notes:
1. An initial pause of 200 µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles. (Example : $\overline{RAS}$-only-refresh) before proper device operation is achieved.
2. The AC characteristics assume t_T = 5 ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. This parameter is measured with a load circuit equivalent to 1 TTL load and 50 pF. Output timing reference levels are V_{OH} = 2.0 V and V_{OL} = 0.8 V.
5. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
6. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{UCAS}$, $\overline{LCAS}$, leading edge in an early write cycle, and to $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle or a read modify write cycle.
8. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) , $t_{RWD} \geq t_{RWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.) , the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
11. These parameters are determined by the falling edge of $\overline{UCAS}$ or $\overline{LCAS}$, whichever is earlier.
12. These parameters are determined by the rising edge of $\overline{UCAS}$ or $\overline{LCAS}$, whichever is later.
13. t_{CWL} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
14. t_{CP} is determined by the time both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
15. Input levels at the AC testing are 3.0 V/0.5 V.

TIMING WAVEFORM

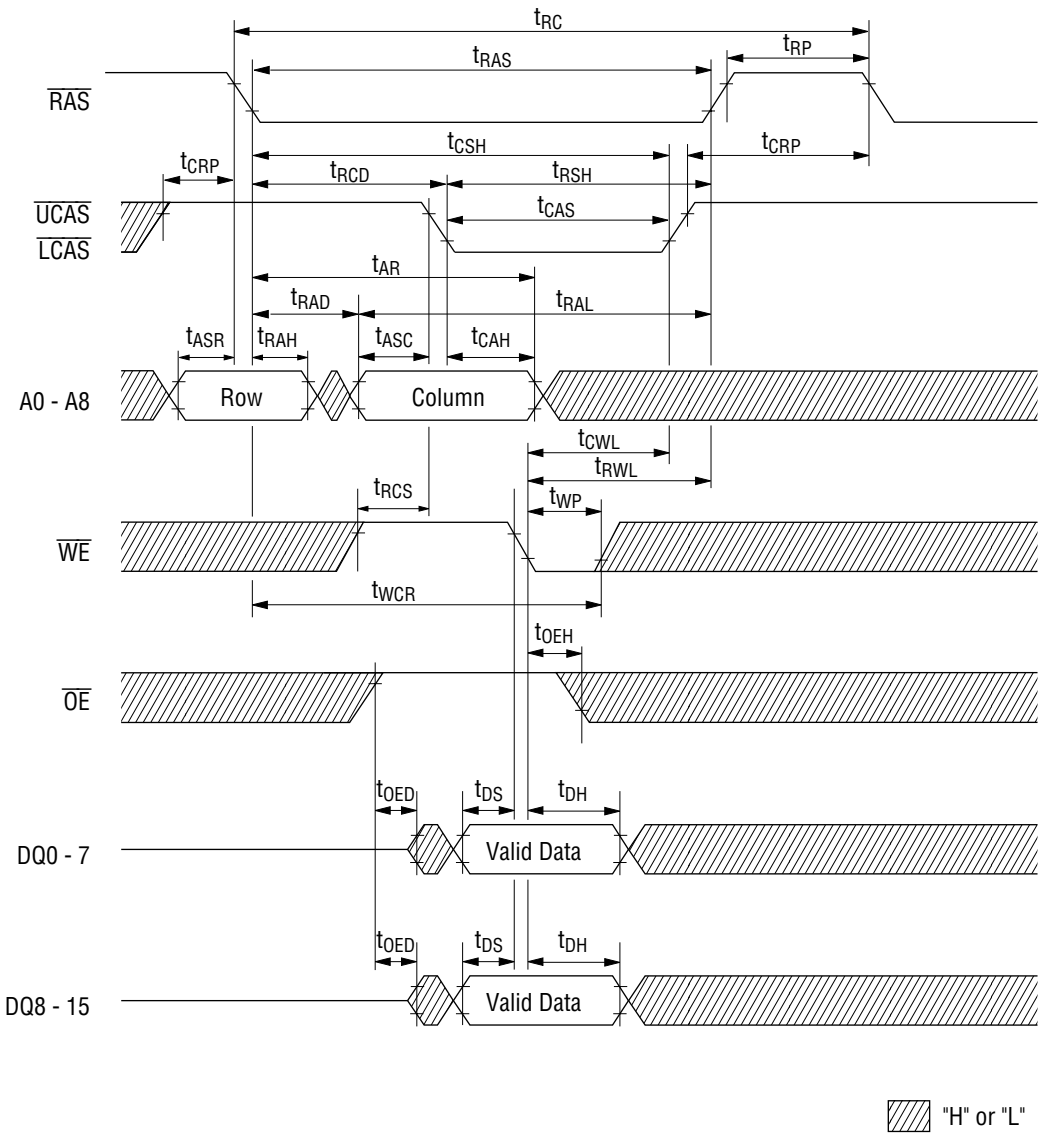
Read Cycle



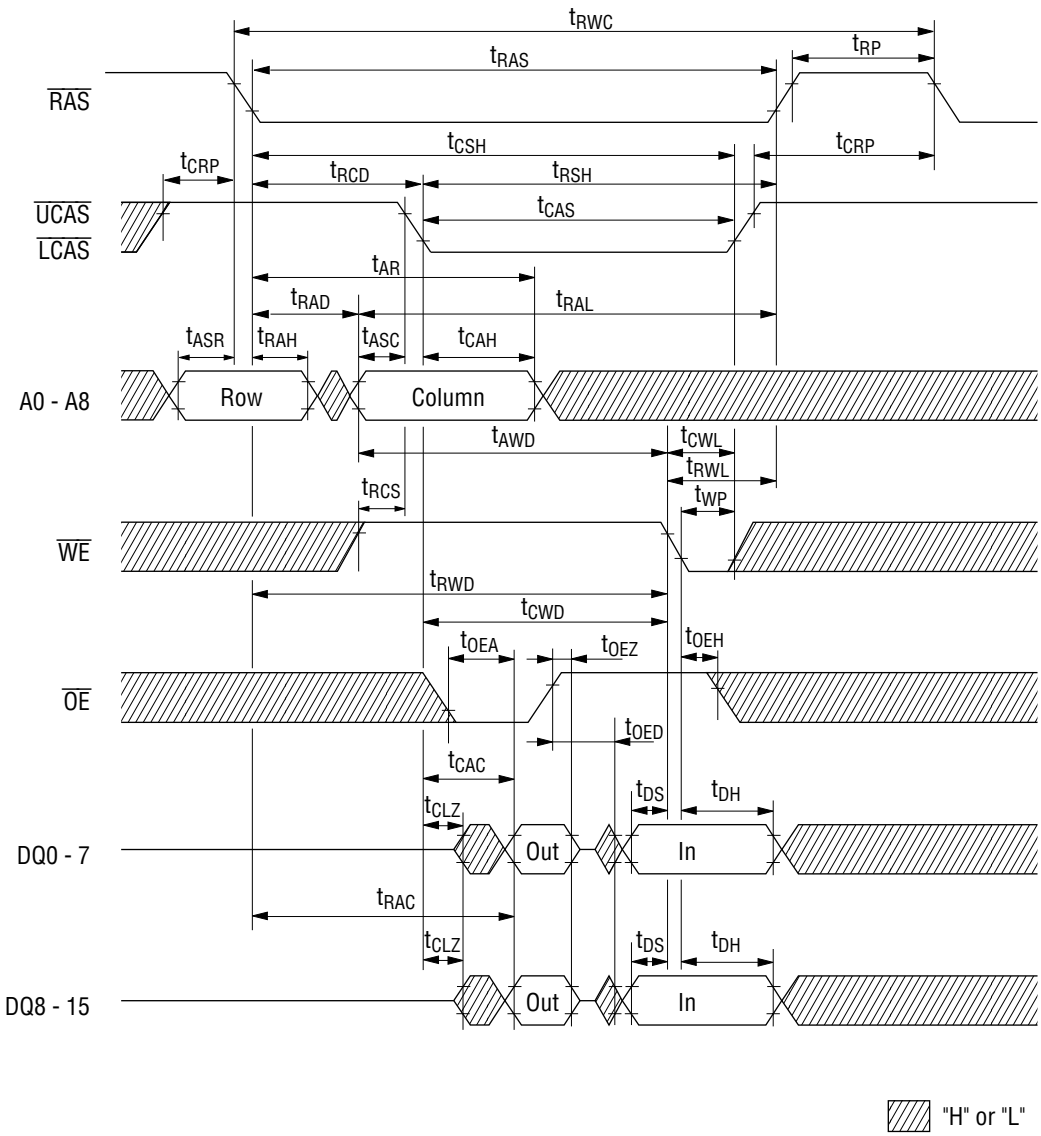
Early Write Cycle ($\overline{LCAS}$ and $\overline{UCAS}$ Active)



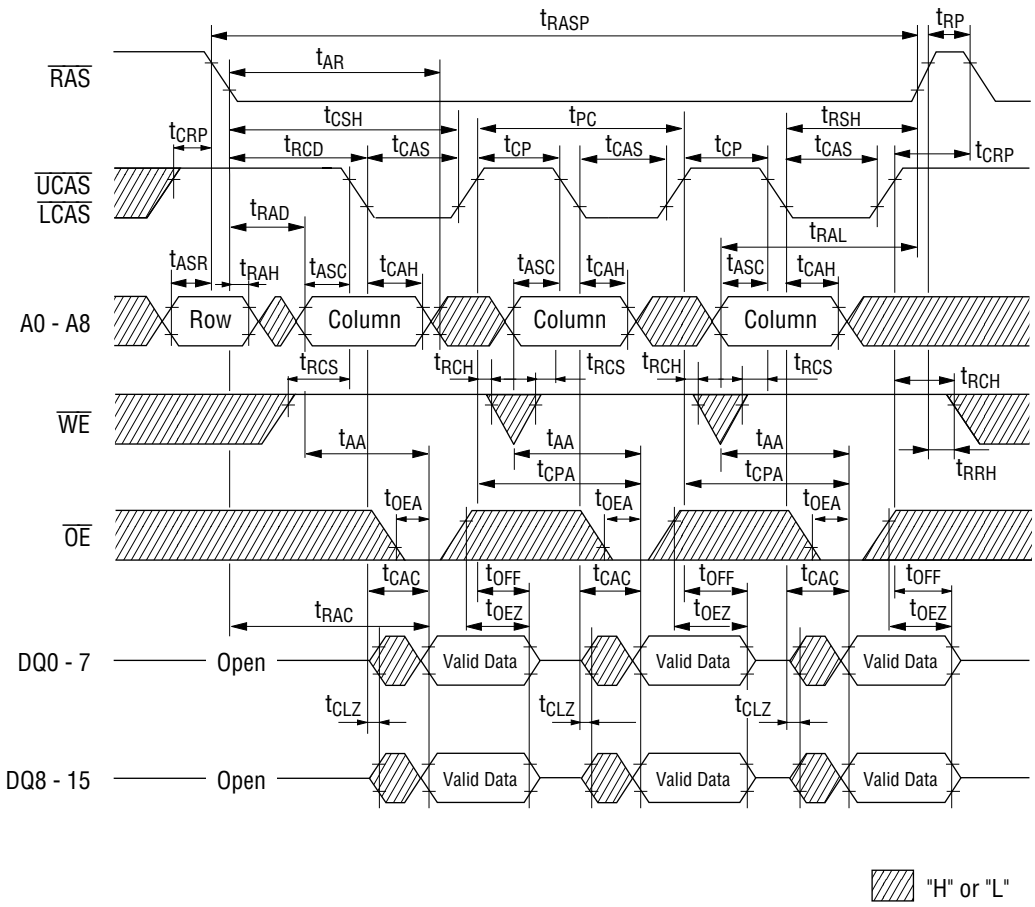
Late Write Cycle ($\overline{LCAS}$ and $\overline{UCAS}$ Active)



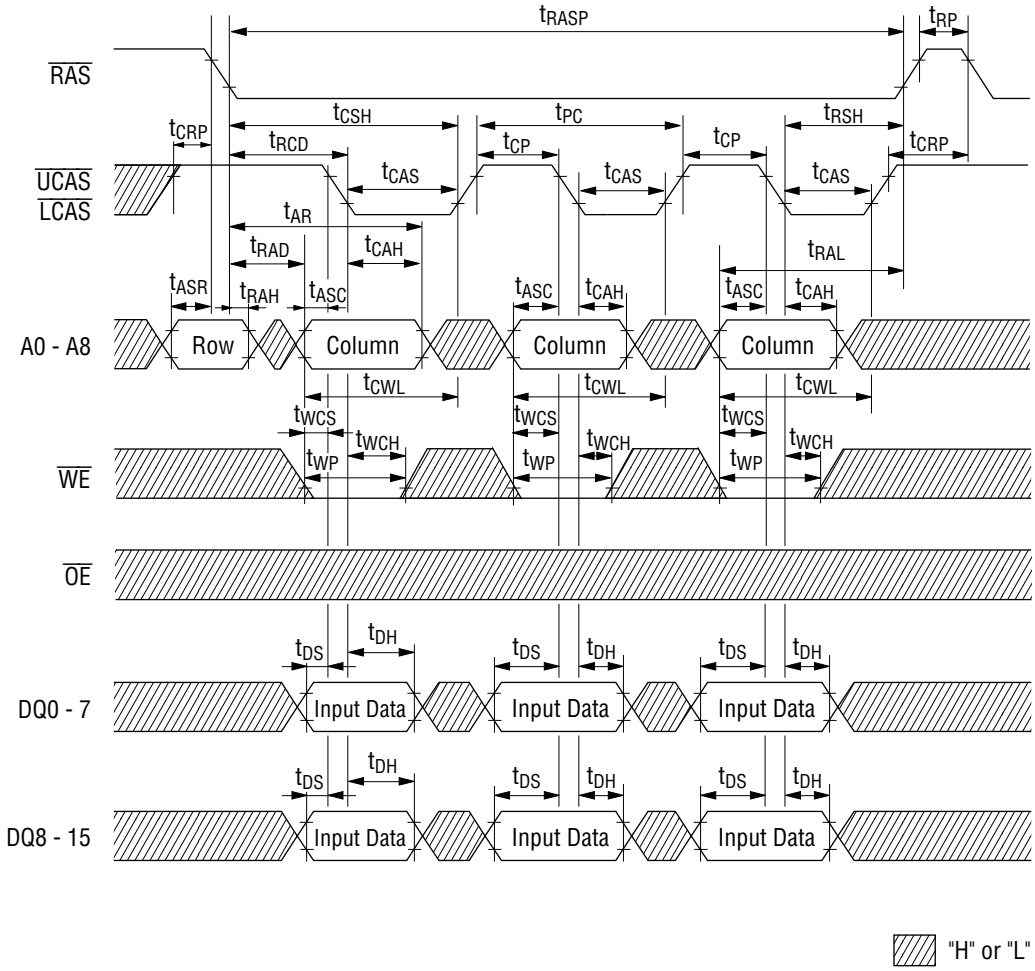
Read Modify Write Cycle ($\overline{LCAS}$ and $\overline{UCAS}$ Active)



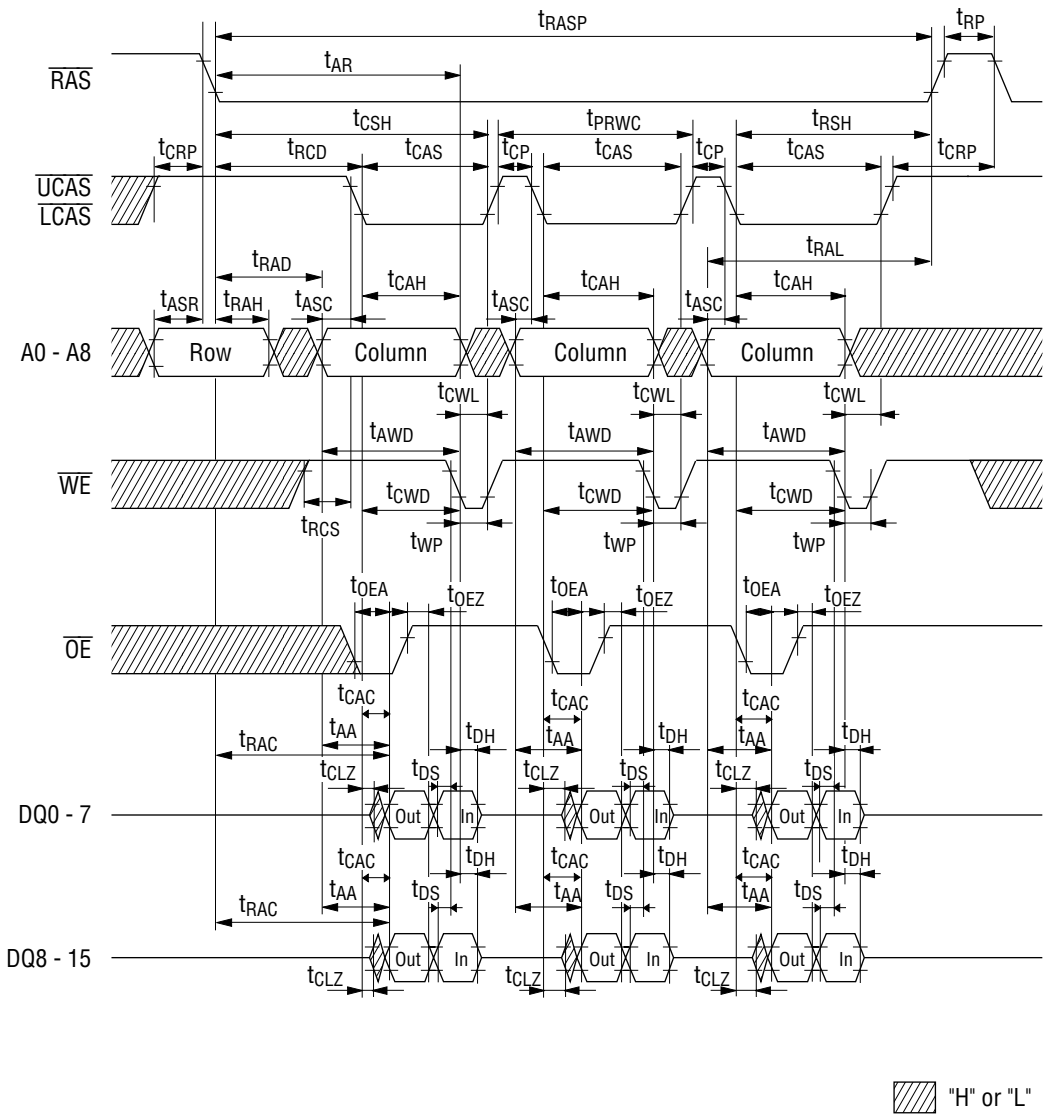
Fast Page Mode Read Cycle



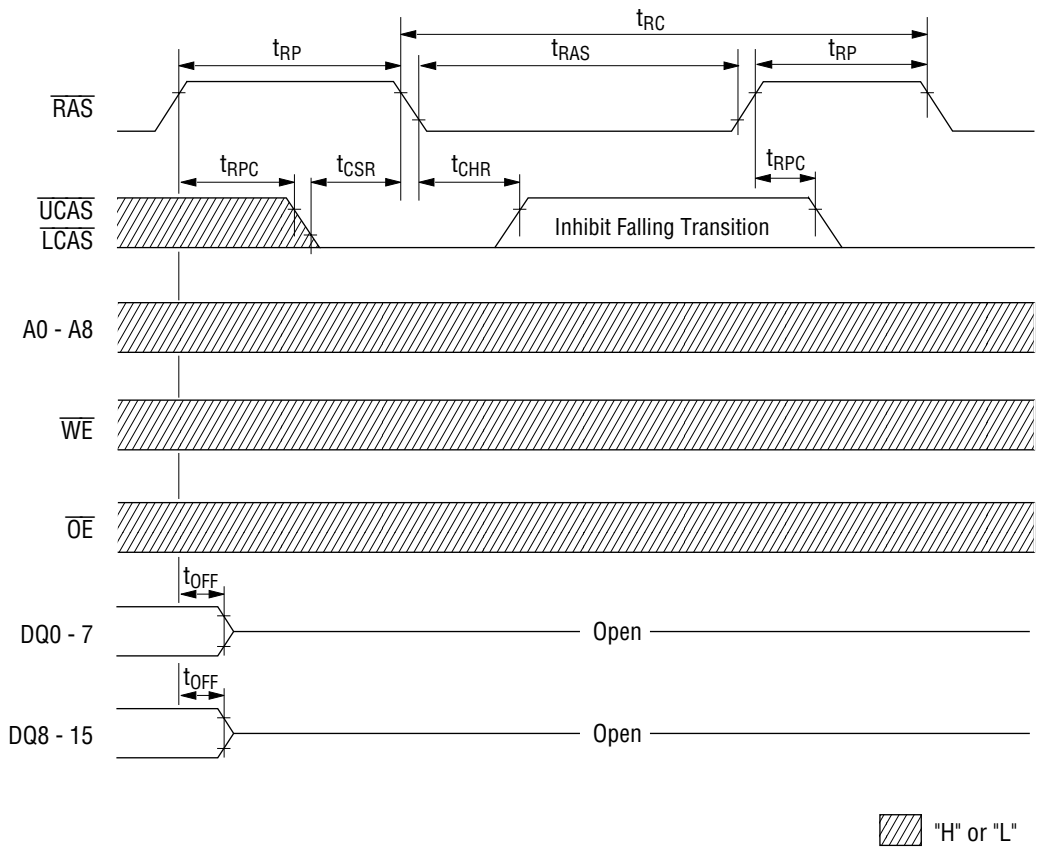
Fast Page Mode Early Write Cycle



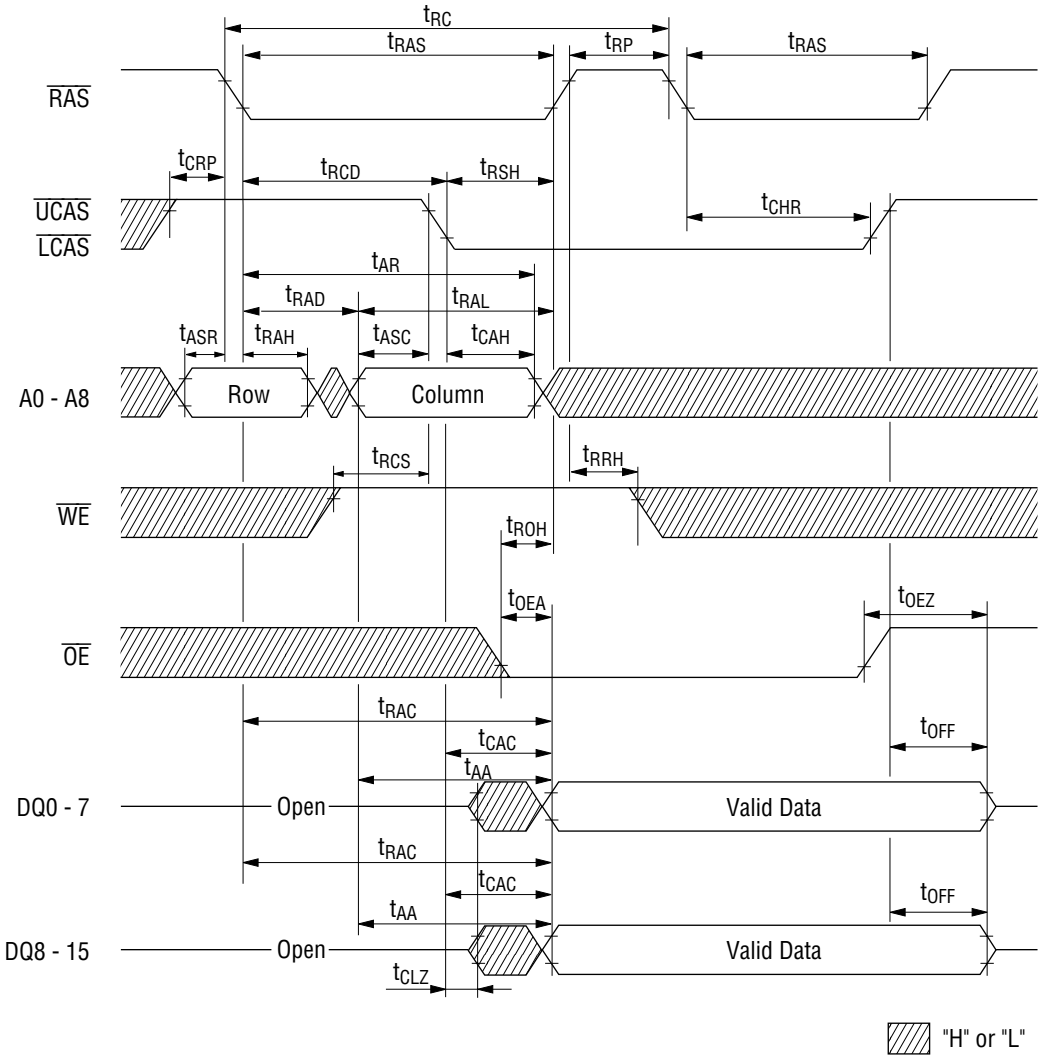
Fast Page Mode Read Modify Write Cycle



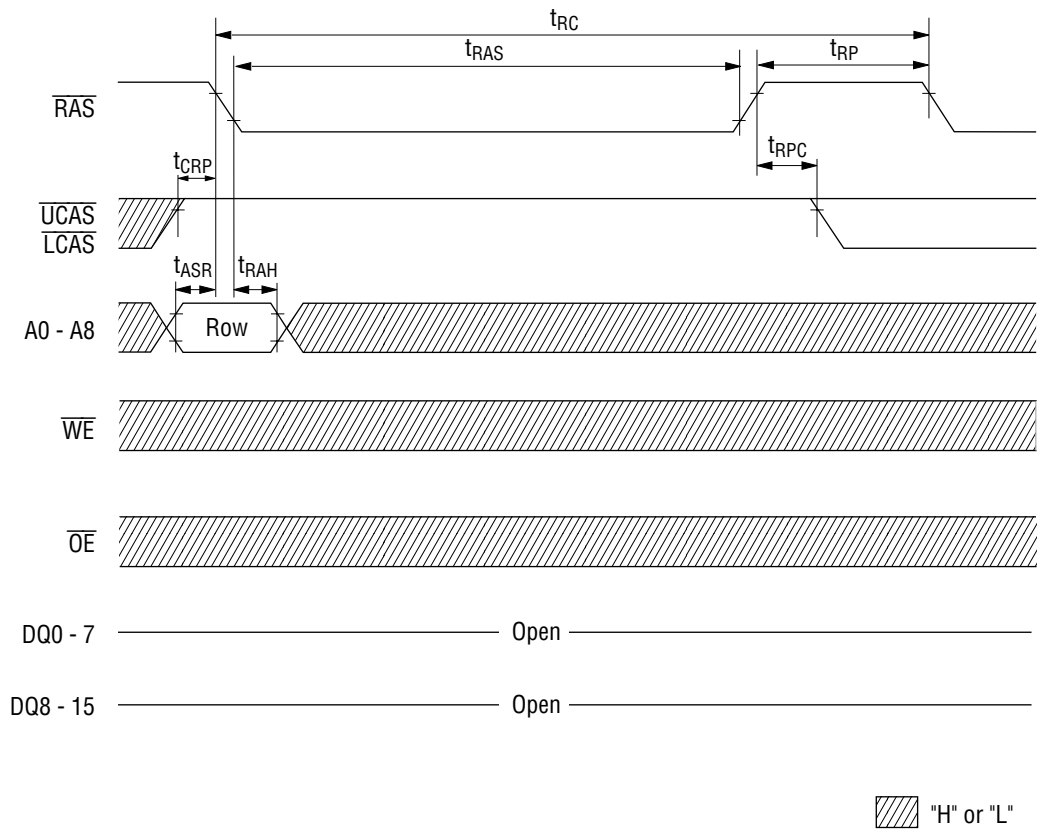
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Hidden Refresh Cycle



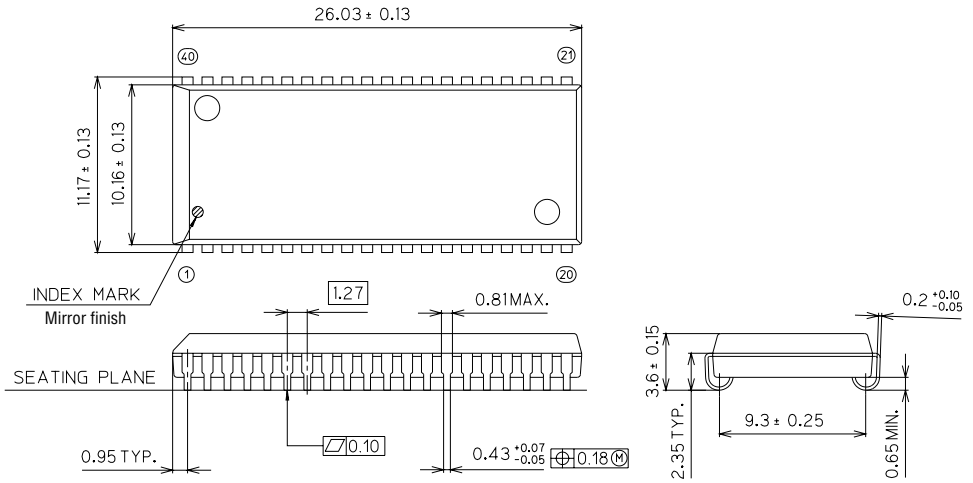
$\overline{\text{RAS}}$ Only Refresh Cycle



PACKAGE DIMENSIONS

(Unit : mm)

SOJ40-P-400-1.27



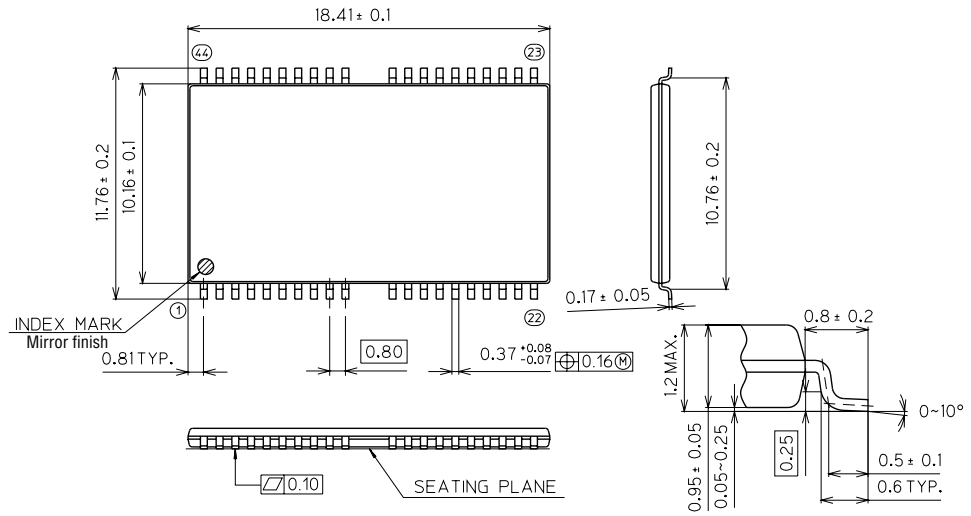
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.70 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TSOPII44/40-P-400-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.49 TYP.

Notes for Mounting the Surface Mount Type Package

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