# Five/Ten Output Clock Generator/Buffer

## FEATURES

- Universal Input Buffers That Accept LVPECL, LVDS, or LVCMOS Level Signaling
- Fully Configurable Outputs Including Frequency, Output Format, and Output Skew
- Output Multiplexer That Serves as a Clock Switch Between the Three Reference Inputs and the Outputs
- Clock Generation Via AT-Cut Crystal
- Integrated EEPROM Determines Device Configuration at Power-up
- Low Additive Jitter Performance
- Universal Output Blocks Support up to 5 Differential, 10 Single-ended, or Combinations of Differential or Single-ended:
  - Low Additive Jitter
  - Output Frequency up to 1.5 GHz
  - LVPECL, LVDS, LVCMOS, and Special High Output Swing Modes
  - Independent Output Dividers Support Divide Ratios from 1–80
  - Independent limited Coarse Skew Control on all Outputs
- Flexible Inputs:
  - Two Universal Differential Inputs Accept Frequencies up to 1500 MHz (LVPECL), 800 MHz (LVDS), or 250 MHz (LVCMOS).
  - One Auxiliary Input Accepts Single Ended Clock Source or Crystal. Auxiliary Input Accepts Crystals in the Range of 2 MHz–42 MHz or an LVCMOS Input up to 75 MHz.
  - Clock Generator Mode Using Crystal Input.
- Typical Power Consumption 1.0W at 3.3V (see Table 27)
- Integrated EEPROM Stores Default Settings; Therefore, The Device Powers up in a Known, Predefined State.
- Offered in QFN-48 Package
- ESD Protection Exceeds 2kV HBM
- Industrial Temperature Range –40°C to 85°C

## APPLICATIONS

- Data Converter and Data Aggregation Clocking
- Wireless Infrastructure
- Switches and Routers
- Medical Electronics
- Military and Aerospace
- Industrial
- Clock Fan-out

## DESCRIPTION

The CDCE18005 is a high performance clock generator and distributor featuring a high degree of configurability via a SPI interface, and programmable start up modes determined by on-board EEPROM. Specifically tailored for buffering clocks for data converters and high-speed digital signals, the CDCE18005 achieves low additive jitter in the 50 fs RMS(1) range. The clock distribution block includes five individually programmable outputs that can be configured to provide different combinations of output formats (LVPECL, LVDS, LVCMOS). Each output can also be programmed to a unique output frequency (up to 1.5 GHz(2) ) and skew relationship via a programmable delay block. If all outputs are configured in single-ended mode (e.g. LVCMOS), the CDCE18005 supports up to ten outputs. Each output can select one of three clock input sources. The input block includes two universal differential inputs which support frequencies up to 1500 MHz and an auxiliary single ended input that can be connected to a CMOS level clock or configured to connect to an external crystal via an on board oscillator block.

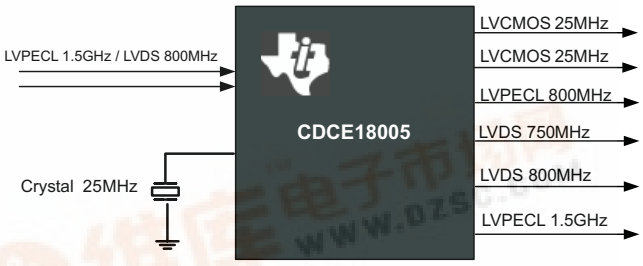



**Figure 1. CDCE18005 Application Example**

(1) 12 kHz to 20 MHz integration bandwidth.
(2) Maximum output frequency depends on the output format selected

## DEVICE INFORMATION

### PACKAGE

The CDCE18005 is packaged in a 48-Pin Plastic Quad Flatpack Package with enhanced bottom thermal pad for heat dissipation. The Texas Instruments Package Designator is: **RGZ (S-PQFP-N48)**

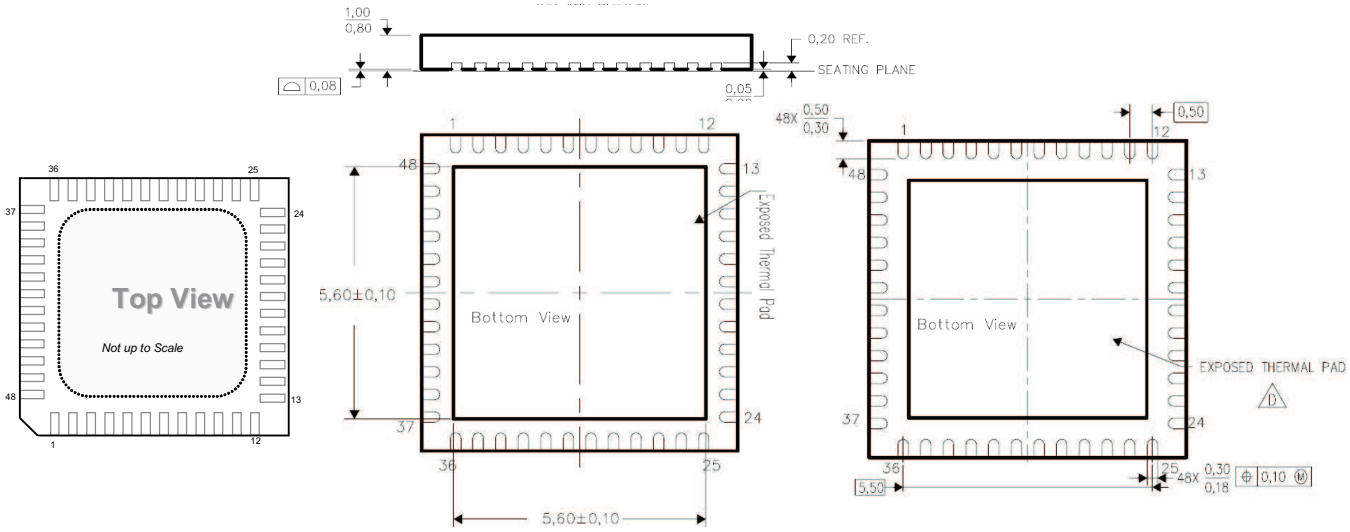



**Figure 2. 48-Pin QFN Package Outline**

## PIN FUNCTIONS

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | QFN | | |
| VCC_OUT | 8, 11, 15, 18, 21, 26, 29, 32 | Power | 3.3V Supply for the Output Buffers |
| VCC_CORE | 5, 39, 42, 34, 35 | Power | 3.3V Core Voltage Circuitry |
| VCC_IN_PRI | 47 | A. Power | 3.3V References Input Buffer and Circuitry Supply Voltage. |
| VCC_IN_SEC | 1 | A. Power | 3.3V References Input Buffer and Circuitry Supply Voltage. |
| VCC_IN_AUX | 44 | A. Power | 3.3V Crystal Oscillator Input Circuitry. |
| GND | 36 | Ground | Ground (All internal Ground Pins are connected to the PAD) |
| GND | PAD | Ground | Ground is on Thermal PAD. See Layout recommendation |
| SPI_MISO | 22 | OD | In SPI Mode it is an Open Drain Output and it functions as a Master In Slave Out as a serial Control Data Output to CDCE18005 . |
| SPI_LE | 25 | I | LVCMOS input, control Latch Enable for Serial Programmable Interface (SPI), with Hysteresis in SPI Mode. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1". |
| SPI_CLK | 24 | I | LVCMOS input, serial Control Clock Input for the SPI bus interface, with Hysteresis. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1". |
| SPI_MOSI | 23 | I | LVCMOS input, Master Out Slave In as a serial Control Data Input to **CDCE18005** for the SPI bus interface. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1". |
| TEST_MODE | 33 | I | Pull High or leave unconnected |
| TEST_MODE2 | 31 | I | Pull High or leave unconnected |
| $\overline{\text{Power\_Down}}$ | 12 | I | Active Low. Power down mode can be activated via this pin. See Table 13 for more details. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1". SPI_LE has to be HIGH in order for the rising edge of $\overline{\text{Power\_Down}}$ signal to load the EEPROM. |
| $\overline{\text{SYNC}}$ | 14 | I | Active Low. Sync mode can be activated via this pin. See Table 13 for more details. The input has an internal 150-kΩ, pull-up resistor if left unconnected it will default to logic level “1”. |
| AUX IN | 43 | I | Auxiliary Input is a single ended input including an on-board oscillator circuit so that a crystal may be connected. |
| AUX OUT | 13 | O | Auxiliary Output LVCMOS level that can be programmed via SPI interface to be driven by Output 2 or Output 3. |
| PRI REF+ | 45 | I | Universal Input Buffer (LVPECL, LVDS, LVCMOS) positive input for the Primary Reference Clock, |
| PRI REF– | 46 | I | Universal Input Buffer (LVPECL, LVDS) negative input for the Primary Reference Clock. In case of LVCMOS signaling Ground this pin. |
| SEC REF+ | 3 | I | Universal Input Buffer (LVPECL, LVDS, LVCMOS) positive input for the Secondary Reference Clock, |
| SEC REF– | 2 | I | Universal Input Buffer (LVPECL, LVDS,) negative input for the Secondary Reference Clock. In case of LVCMOS signaling Ground this pin. |
| TESTOUTA | 30 | Analog | Analog Test Point for Use for TI Internal Testing. Pull Down to GND Via a 1kΩ Resistor. |
| NC | 4 | | This Pin is not used |
| NC | 38 | | This Pin is not used |
| VBB | 48 | Analog | Capacitor for the internal termination Voltage. Connect to a 1µF Capacitor (Y5V) |
| NC | 40 | | This Pin is not used |
| NC | 41 | | This Pin is not used |
| NC | 37 | | This Pin is not used |
| U0P:U0N<br>U1P:U1N:<br>U2P:U2N<br>U3P:U3N<br>U4P:U4N | 27, 28<br>19, 20<br>16,17<br>9, 10<br>6, 7 | O | The Main outputs of **CDCE18005** are user definable and can be any combination of up to 5 LVPECL outputs, 5 LVDS outputs or up to 10 LVCMOS outputs. The outputs are selectable via SPI interface. The power-up setting is EEPROM configurable. |

## FUNCTIONAL DESCRIPTION

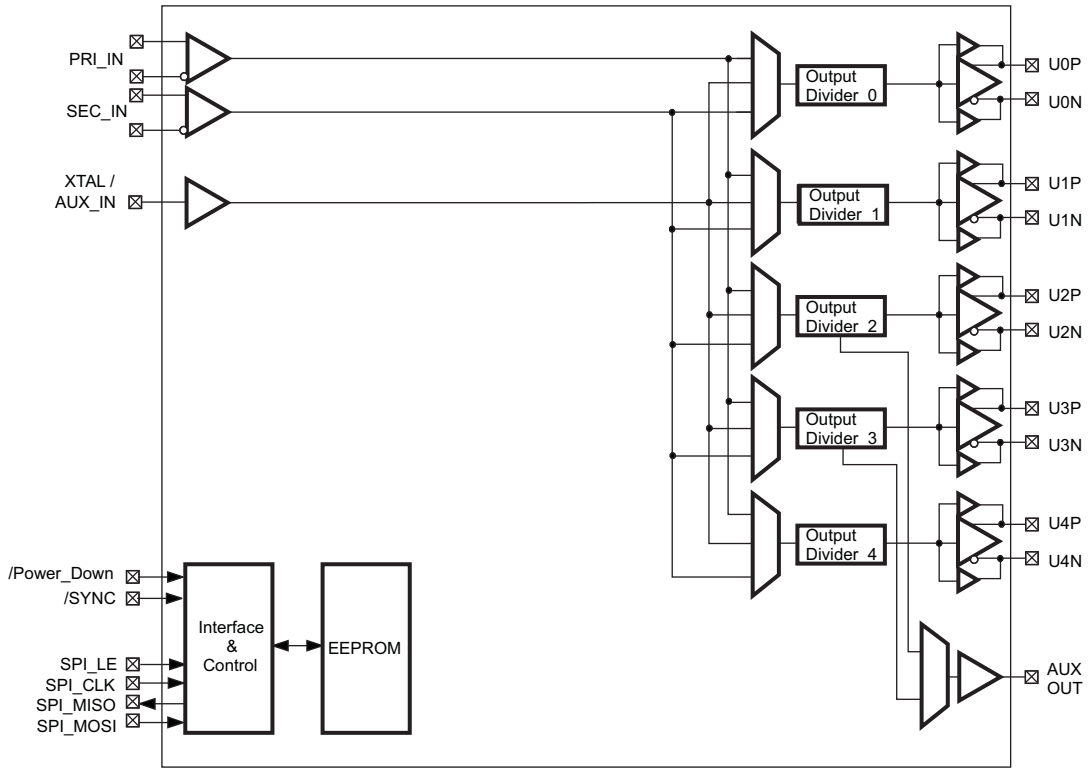



**Figure 3. CDCE18005 Block Diagram**

The CDCE18005 comprises three primary blocks: the interface and control block, the input block and the output block. In order to determine which settings are appropriate for any specific combination of input/output frequencies, a basic understanding of these blocks is required. The interface and control block determines the state of the CDCE18005 at power-up based on the contents of the

on-board EEPROM. In addition to the EEPROM, the SPI port is available to configure the CDCE18005 by writing directly to the device registers after power-up. The input block buffers three clock signals, converts them to differential signals, and drives them onto an internal clock distribution bus. The output block provides five separate clock channels that are fully programmable and configurable to select and condition one of four internal clock sources

**NOTE:**

This Section of the data sheet provides a high-level description of the features of the CDCE18005 for purpose of understanding its capabilities. For a complete description of device registers and I/O, please refer to the Device Configuration Section.

## Interface and Control Block

The CDCE18005 is a highly flexible and configurable architecture and as such contains a number of registers so that the user may specify device operation. The contents of nine 28-bit wide registers implemented in static RAM determine device configuration at all times. The CDCE18005 implements the SPI Interface Mode. SPI Interface Mode is used to access the device RAM and EEPROM either during normal operation (if the host system provides a native SPI interface) or during device configuration (i.e. device programming). During power up the EEPROM content gets copied into the registers after the detection of a valid device power-up. The EEPROM can be locked enabling the designer to implement a fault tolerant design.

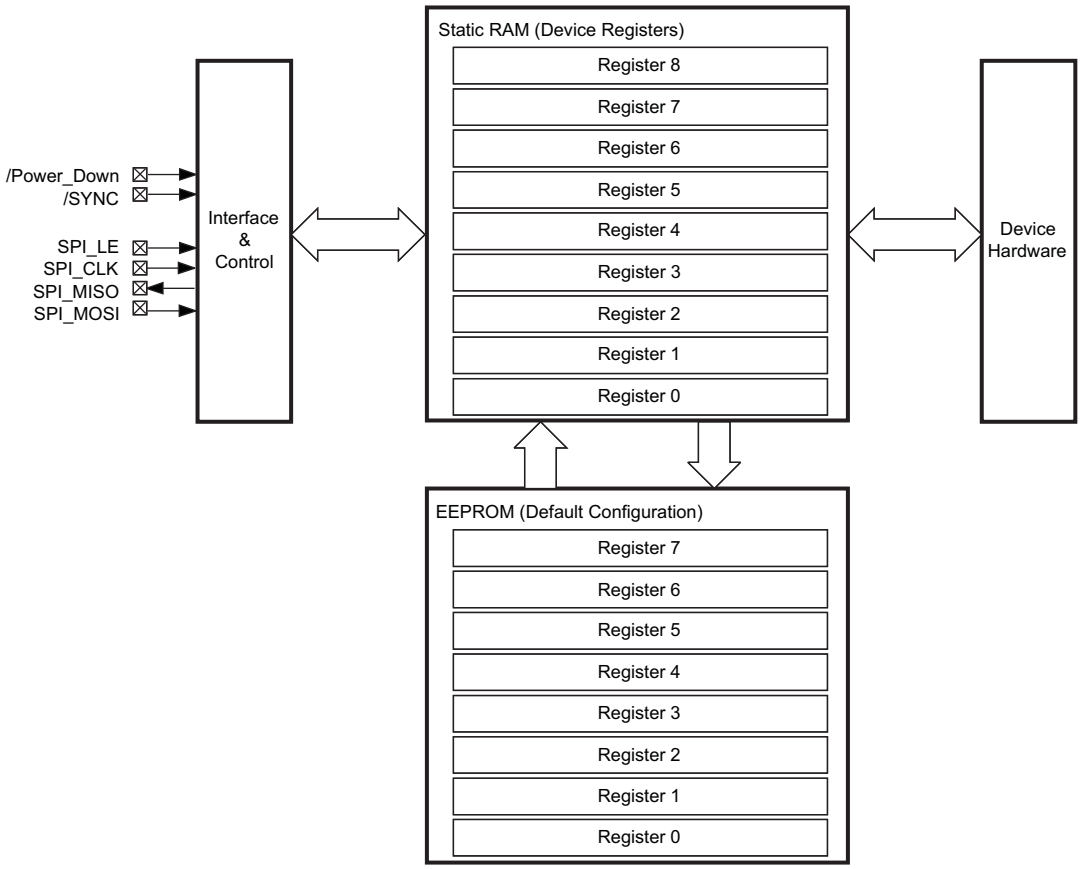



**Figure 4. CDCE18005 Interface and Control Block**

## Input Block

The Input Block includes a pair of Universal Input Buffers and an Auxiliary Input. The Input Block buffers the incoming signals and facilitates signal routing to the Internal Clock Distribution bus. The Internal Clock Distribution Bus connects to all output blocks discussed in the next section. Therefore, a clock signal present on the Internal Clock Distribution bus can appear on any or all of the device outputs.

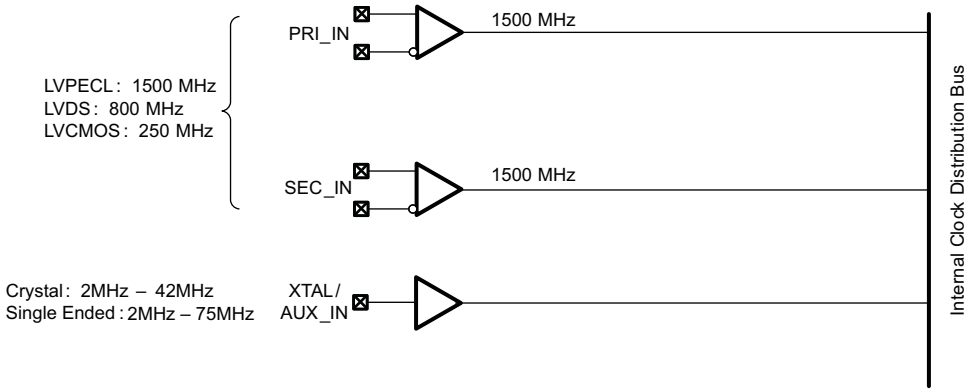



**Figure 5. CDCE18005 Input Block**

## Output Block

Each of the five identical output blocks incorporates an output multiplexer, a clock divider module, and a universal output array as shown.

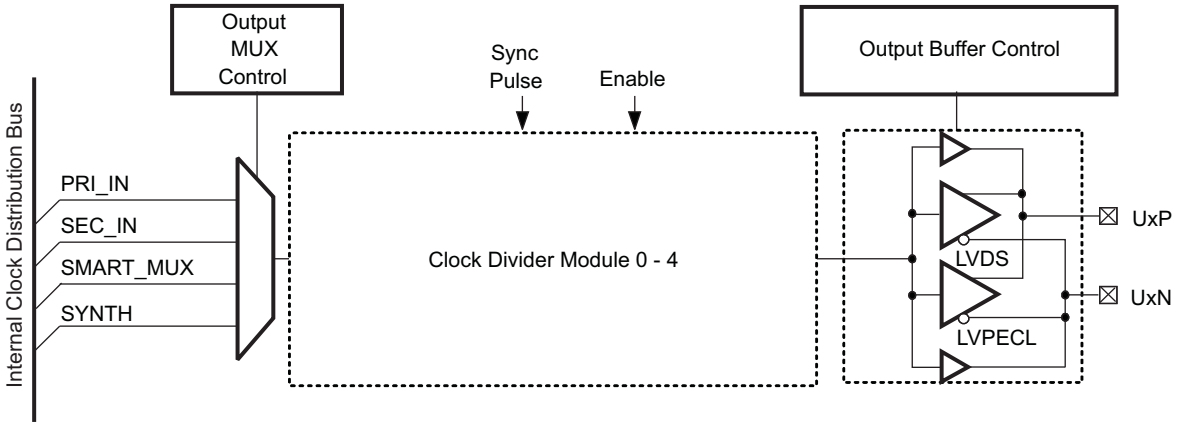



**Figure 6. CDCE18005 Output Block (1 of 5)**

### *Clock Divider Module 0–4*

The following shows a simplified version of a Clock Divider Module (CDM). If an individual clock output channel is not used, then the user should disable the CDM and Output Buffer for the unused channel to save device power. Each channel includes two 7-bit registers to control the divide ratio used and the clock phase for each output.

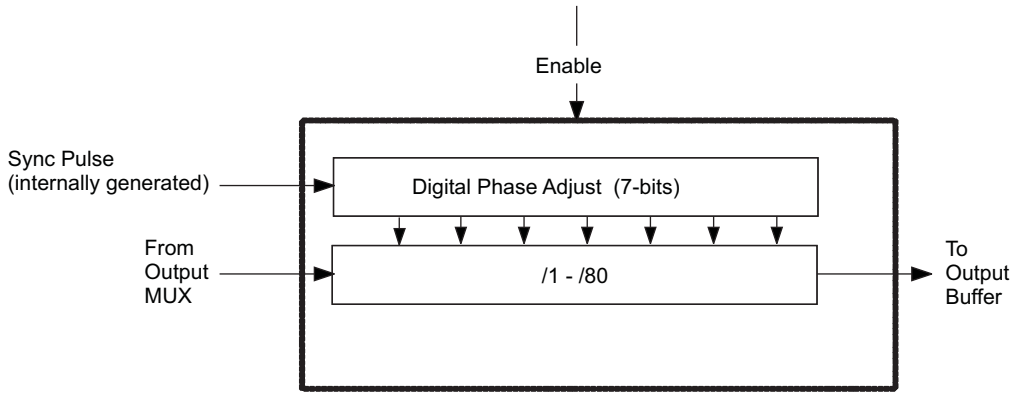



**Figure 7. CDCE18005 Output Divider Module (1 of 5)**

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage range(2) | -0.5 to 4.6 | V |
| $V_I$ | Input voltage range(3) | –0.5 to VCC + 0.5 | V |
| $V_O$ | Output voltage range(3) | –0.5 to VCC + 0.5 | V |
| | Input Current ($V_I$ < 0, $V_I$ > $V_{CC}$) | ±20 | mA |
| | Output current for LVPECL/LVCMOS Outputs (0 < $V_O$ < $V_{CC}$) | ±50 | mA |
| $T_J$ | Maximum junction temperature | 125 | °C |
| $T_{stg}$ | Storage temperature range | –65 to 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated *under recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All supply voltages have to be supplied simultaneously.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp–current ratings are observed.

## THERMAL CHARACTERISTICS

Package Thermal Resistance for QFN (RGZ) Package (1) (2)

| AIRFLOW (LFM) | | $\theta_{JP}$ (°C/W)(3) | $\theta_{JA}$ (°C/W) |
|---|---|---|---|
| 0 | JEDEC Compliant Board (6X6 VIAs on PAD) | 2 | 28.9 |
| 100 | JEDEC Compliant Board (6X6 VIAs on PAD) | 2 | 20.4 |
| 0 | Recommended Layout (7X7 VIAs on PAD) | 2 | 27.3 |
| 100 | Recommended Layout (7X7 VIAs on PAD) | 2 | 20.3 |

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) Connected to GND with 36 thermal vias (0,3 mm diameter).
(3) $\theta_{JP}$ (Junction – Pad) is used for the QFN Package, because the main heat flow is from the Junction to the GND-Pad of the QFN.

## ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS

recommended operating conditions for the **CDCE18005** device for under the specified Industrial temperature range of –40°C to 85°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{CC}$ | Supply voltage | | 3 | 3.3 | 3.6 | V |
| $V_{CC\_IN}$ & $V_{Core}$ | Analog supply voltage | | 3 | 3.3 | 3.6 | |
| $P_{LVPECL}$ | REF at 491.52 MHz, Outputs are LVPECL | Output 1 = 491.52 MHz (LVCMOS = 245 MHz)<br>Output 2 = 245.76 MHz<br>Output 3 = 122.88 MHz<br>Output 4 = 61.44 MHz<br>Output 5 = 30.72 MHz | | 1.6 | | W |
| $P_{LVDS}$ | REF at 491.52 MHz, Outputs are LVDS | | | 1.3 | | W |
| $P_{LVCMOS}$ | REF at 491.52 MHz, Outputs are LVCMOS | | | 1.5 | | W |
| $P_{OFF}$ | REF at 491.52 MHz | Dividers are disabled.<br>Outputs are disabled. | | 0.45 | | W |
| $P_{PD}$ | | Device is powered down | | 20 | | mW |
| **DIFFERENTIAL INPUT MODE (PRI_IN, SEC_IN)** | | | | | | |
| $V_{INPP}$ | Input amplitude ($V_{IN} – V_{\overline{IN}}$) | | 0.1 | | 1.3 | V |
| $V_{IC}$ | Common-mode input voltage | | 1.0 | | $V_{CC}$–0.3 | V |
| $I_{IH}$ | Differential input current high (no internal termination) | $V_I = V_{CC}$, $V_{CC}$ = 3.6 V | | | 20 | µA |
| $I_{IL}$ | Differential input current low (no internal termination) | $V_I$ = 0 V, $V_{CC}$ = 3.6 V | –20 | | 20 | µA |
| | Input Capacitance on PRI_IN, SEC_IN | | | 3 | | pF |
| **LVCMOS INPUT MODE (AUX_IN)** | | | | | | |
| $V_{IL}$ | Low-level input voltage LVCMOS | | 0 | | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage LVCMOS | | 0.7 $V_{CC}$ | | $V_{CC}$ | V |
| | VIK LVCMOS input clamp voltage | $V_{CC}$ = 3 V, $I_I$ = –18 mA | | | –1.2 | V |
| $I_{IH}$ | LVCMOS input current | $V_I = V_{CC}$, $V_{CC}$ = 3.6 V | | 300 | | µA |
| $I_{IL}$ | LVCMOS input | $V_I$ = 0 V, $V_{CC}$ = 3.6 V | –10 | | 10 | µA |
| $C_I$ | Input capacitance (LVCMOS signals) | $V_I$ = 0 V or $V_{CC}$ | | 8 | | pF |
| **CRYSTAL INPUT SPECIFICATIONS** | | | | | | |
| | Crystal shunt capacitance | | | | 20 | pF |
| | Equivalent series resistance (ESR) | | | | 50 | Ω |
| **LVCMOS INPUT MODE (SPI_CLK,SPI_MOSI,SPI_LE,PD,SYNC,REF_SEL, PRI_IN, SEC_IN )** | | | | | | |
| | Low-level input voltage LVCMOS, | | 0 | | 0.3 $V_{CC}$ | V |
| | High-level input voltage LVCMOS | | 0.7 $V_{CC}$ | | $V_{CC}$ | V |
| $V_{IK}$ | LVCMOS input clamp voltage | $V_{CC}$ = 3 V, $I_I$ = –18 mA | | | –1.2 | V |
| $I_{IH}$ | LVCMOS input current | $V_I = V_{CC}$, $V_{CC}$ = 3.6 V | | | | µA |
| $I_{IL}$ | LVCMOS input (Except PRI_IN and SEC_IN) | $V_I$ = 0 V, $V_{CC}$ = 3.6 V | –10 | | –40 | µA |
| $I_{IL}$ | LVCMOS input (PRI_IN and SEC_IN) | $V_I$ = 0 V, $V_{CC}$ = 3.6 V | –10 | | 10 | µA |
| $C_I$ | Input capacitance (LVCMOS signals) | $V_I$ = 0 V or $V_{CC}$ | | 3 | | pF |

## ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)

recommended operating conditions for the **CDCE18005** device for under the specified Industrial temperature range of –40°C to 85°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SPI OUTPUT (MISO)** | | | | | | | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3.3 V, | $V_O$ = 1.65 V | | –30 | | mA |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3.3 V, | $V_O$ = 1.65 V | | 33 | | mA |
| $V_{OH}$ | High-level output voltage for LVCMOS outputs | $V_{CC}$ = 3 V, | $I_{OH}$ = −100 µA | $V_{CC}$–0.5 | | | V |
| $V_{OL}$ | Low-level output voltage for LVCMOS outputs | $V_{CC}$ = 3 V, | $I_{OL}$ = 100 µA | | | 0.3 | V |
| $C_O$ | Output capacitance on MISO | VCC = 3.3 V; VO = 0 V or VCC | | | 3 | | pF |
| $I_{OZH}$ | 3-state output current | $V_O$ = $V_{CC}$ , $V_O$ = 0 V | | | 5 | | µA |
| $I_{OZL}$ | | | | | –5 | | |
| **VBB** | | | | | | | |
| VBB | Termination voltage for reference inputs. | $I_{BB}$ = –0.2 mA, Depending on the setting. | | 0.9 | | 1.9 | V |
| **INPUT BUFFERS INTERNAL TERMINATION RESISTORS (PRI_IN and SEC_IN)** | | | | | | | |
| | Termination resistance | Single ended | | | 50 | | Ω |

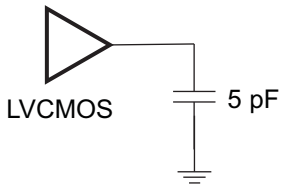
(1) All typical values are at $V_{CC}$ = 3.3 V, temperature = 25 °C

## ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)

recommended operating conditions for the **CDCE18005** device for under the specified Industrial temperature range of –40°C to 85°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **LVCMOS OUTPUT OR AUXILIARY OUTPUT** | | | | | | | |
| $f_{clk}$ | Output frequency, see Figure Below | Load = 5 pF to GND | | | | 250 | MHz |
| $V_{OH}$ | High-level output voltage for LVCMOS outputs | $V_{CC}$ = min to max | $I_{OH}$ = –100 µA | $V_{CC}$ –0.5 | | | |
| $V_{OL}$ | Low-level output voltage for LVCMOS outputs | $V_{CC}$ = min to max | $I_{OL}$ =100 A | | | 0.3 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3.3 V | $V_O$ = 1.65 V | | –30 | | mA |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3.3 V | $V_O$ = 1.65 V | | 33 | | mA |
| $t_{pd(LH)}$/ $t_{pd(HL)}$ | Propagation delay from PRI_IN or SEC_IN to Outputs (LVCMOS to LVCMOS) | $V_{CC}$/2 to $V_{CC}$/2 | | | 4 | | ns |
| $t_{sk(o)}$ | Skew, output to output For Y0 to Y4 | All Outputs set at 200 MHz, Reference = 200 MHz | | | 75 | | ps |
| $C_O$ | Output capacitance on Y0 to Y4 | $V_{CC}$ = 3.3 V; $V_O$ = 0 V or $V_{CC}$ | | | 5 | | pF |
| $I_{OZH}$ | 3-State LVCMOS output current | $V_O$ = $V_{CC}$ | | | 5 | | µA |
| $I_{OZL}$ | | $V_O$ = 0 V | | | –5 | | µA |
| $I_{OPDH}$ | Power Down output current | $V_O$ = $V_{CC}$ | | | | 25 | µA |
| $I_{OPDL}$ | | $V_O$ = 0 V | | | | 5 | µA |
| | Duty cycle LVCMOS | 50% to 50% | | 45% | | 55% | |
| $t_{slew-rate}$ | Output rise/fall slew rate | | | 3.6 | 5.2 | | V/ns |

(1) All typical values are at $V_{CC}$ = 3.3 V, temperature = 25°C



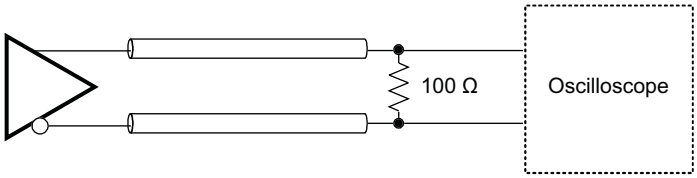
## ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)(1)(2)(3)(4)

recommended operating conditions for the **CDCE18005** device for under the specified Industrial temperature range of –40°C to 85°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP(5) | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LVDS OUTPUT** | | | | | | |
| $f_{clk}$ | Output frequency | Configuration Load (100 Ω) | 0 | | 800 | MHz |
| $\|V_{OD}\|$ | Differential output voltage | $R_L$ = 100 Ω | 270 | | 550 | mV |
| $\Delta V_{OD}$ | LVDS VOD magnitude change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | –40°C to 85°C | | 1.24 | | V |
| $\Delta V_{OS}$ | VOS magnitude change | | | 40 | | mV |
| | Short circuit Vout+ to ground | VOUT = 0 | | | 27 | mA |
| | Short circuit Vout– to ground | VOUT = 0 | | | 27 | mA |
| $t_{pd(LH)}/t_{pd(HL)}$ | Propagation delay from PRI_IN or SEC_IN to outputs (LVDS to LVDS) | Crosspoint to Crosspoint | | 3.1 | | ns |
| $t_{sk(o)}$(6) | Skew, output to output For Y0 to Y4 | All Outputs set at 200 MHz<br>Reference = 200 MHz | | 25 | | ps |
| $C_O$ | Output capacitance on Y0 to Y4 | $V_{CC}$ = 3.3 V; $V_O$ = 0 V or $V_{CC}$ | | 5 | | pF |
| $I_{OPDH}$ | Power down output current | $V_O = V_{CC}$ | | | 25 | µA |
| $I_{OPDL}$ | Power down output current | $V_O$ = 0 V | | | 5 | µA |
| | Duty cycle | 50% input | 45% | | 55% | |
| $t_r$ / $t_f$ | Rise and fall time | 20% to 80% of $V_{OUT(PP)}$ | 110 | 160 | 190 | ps |
| **LVCMOS-TO-LVDS** | | | | | | |
| $t_{skP\_c}$ | Output skew between LVCMOS and LVDS outputs(7) | Crosspoint to VCC/2 | 0.9 | 1.4 | 1.9 | ns |

(1) This is valid only for same REF_IN clock and Y output clock frequency
(2) VINPP minimum and maximum is required to maintain ac specifications; the actual device function tolerates at a minimum VINPP of 100mV.
(3) Lock output has a 80 kΩ pull-down resistor.
(4) The phase of LVCMOS is lagging in reference to the phase of LVDS.
(5) All typical values are at $V_{CC}$ = 3.3 V, temperature = 25°C
(6) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
(7) Operating the LVCMOS or LVDS output above the maximum frequency will not cause a malfunction to the device, but the output signal swing might no longer meet the output specification

LVDS DC Termination Test



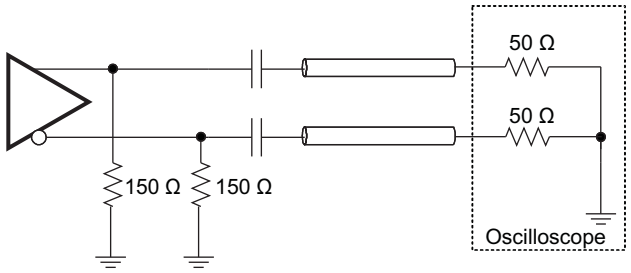
## ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)

recommended operating conditions for the **CDCE18005** device for under the specified Industrial temperature range of –40°C to 85°C

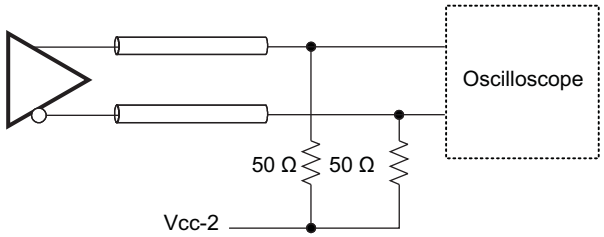
| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LVPECL OUTPUT** | | | | | | |
| $f_{clk}$ | Output frequency | Configuration load (Figures below) | 0 | | 1500 | MHz |
| $V_{OH}$ | LVPECL high-level output voltage load | | $V_{CC}$ –1.06 | | $V_{CC}$ –0.88 | V |
| $V_{OL}$ | LVPECL low-level output voltage load | | $V_{CC}$ –2.02 | | $V_{CC}$ –1.58 | V |
| $\|V_{OD}\|$ | Differential output voltage | | 610 | | 970 | mV |
| $t_{pd(LH)}$/ $t_{pd(HL)}$ | Propagation delay from PRI_IN or SEC_IN to outputs (LVPECL to LVPECL) | Crosspoint to Crosspoint | | 3.4 | | ns |
| $t_{sk(o)}$ | Skew, output to output For Y0 to Y4 | All Outputs set at 200 MHz Reference = 200MHz | | 25 | | ps |
| $C_O$ | Output capacitance on Y0 to Y4 | $V_{CC}$ = 3.3 V; $V_O$ = 0 V or $V_{CC}$ | | 5 | | pF |
| $I_{OPDH}$ | Power Down output current | $V_O$ = $V_{CC}$ | | | 25 | µA |
| $I_{OPDL}$ | | $V_O$ = 0 V | | | 5 | µA |
| | Duty Cycle | 50% input | 45% | | 55% | |
| $t_r$ / $t_f$ | Rise and fall time | 20% to 80% of Voutpp | 55 | 75 | 135 | ps |
| **LVDS-TO-LVPECL** | | | | | | |
| $t_{skP\_C}$ | Output skew between LVDS and LVPECL outputs | Crosspoint to Crosspoint | 0.9 | 1.1 | 1.3 | ns |
| **LVCMOS-TO-LVPECL** | | | | | | |
| $t_{skP\_C}$ | Output skew between LVCMOS and LVPECL outputs | $V_{CC}$/2 to crosspoint | –150 | 260 | 700 | ps |
| **LVPECL HI-PERFORMANCE OUTPUT** | | | | | | |
| $V_{OH}$ | LVPECL high-level output voltage load | | $V_{CC}$ –1.11 | | $V_{CC}$ –0.87 | V |
| $V_{OL}$ | LVPECL low-level output voltage load | | $V_{CC}$ –2.06 | | $V_{CC}$ –1.73 | V |
| $\|V_{OD}\|$ | Differential output voltage | | 760 | | 1160 | mV |
| $t_r$ / $t_f$ | Rise and fall time | 20% to 80% of Voutpp | 55 | 75 | 135 | ps |

(1) All typical values are at $V_{CC}$ = 3.3 V, temperature = 25°C

LVPECL AC Termination Test




LVPECL DC Termination Test



**LVPECL OUTPUT SWING vs FREQUENCY**

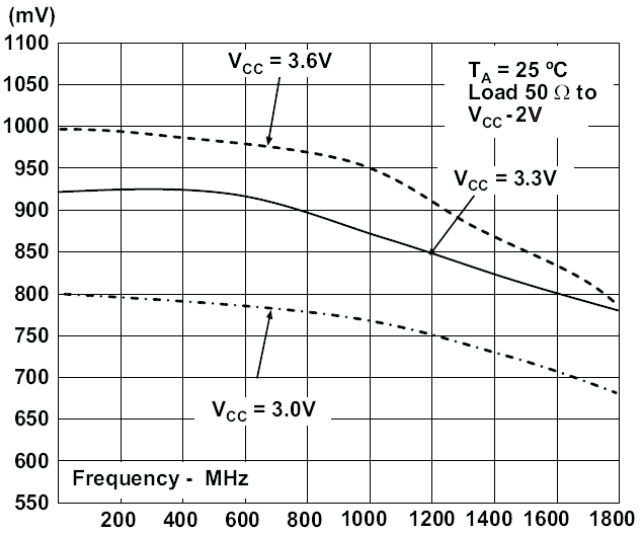



**Figure 8.**

**HI SWING LVPECL OUTPUT SWING vs FREQUENCY**

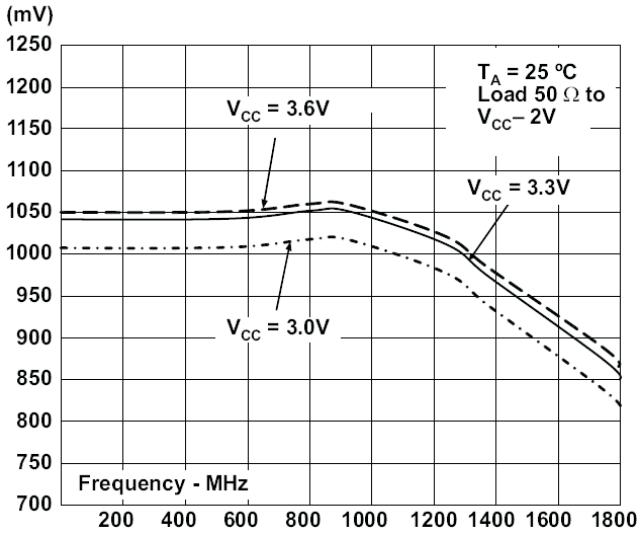



**Figure 9.**

**LVDS OUTPUT SWING vs FREQUENCY**

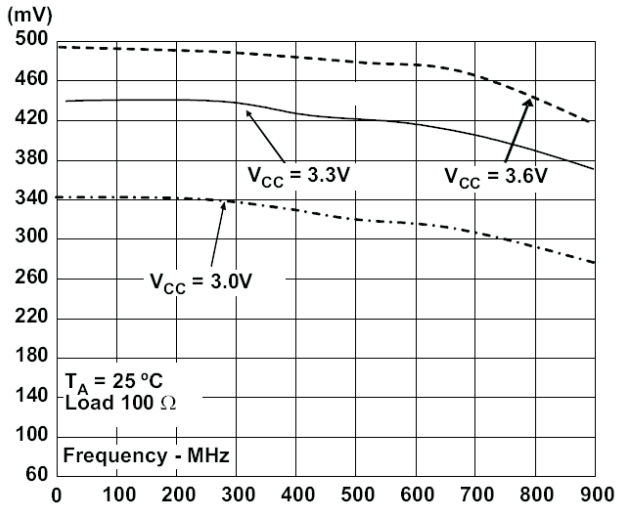



**Figure 10.**

**LVCMOS OUTPUT SWING vs FREQUENCY**

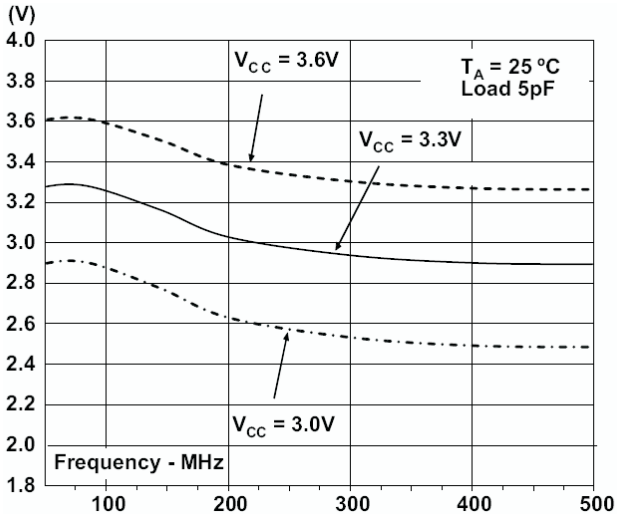



**Figure 11.**

## TIMING REQUIREMENTS

over recommended ranges of supply voltage, load and operating free air temperature (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **PRI_IN/SEC_IN_IN REQUIREMENTS** | | | | | |
| $f_{max}$ | For Single ended Inputs ( LVCMOS) on PRI_IN and SEC_IN | | | 250 | MHz |
| | For Differential Inputs on PRI_IN & SEC_IN | | | 1500 | MHz |
| | Single ended clock duty cycle of PRI_IN or SEC_IN at $V_{CC}$ / 2 | 40% | | 60% | |
| | Differential clock duty cycle of PRI_IN or SEC_IN at $V_{CC}$ / 2 | 40% | | 60% | |
| **AUXILARY_IN REQUIREMENTS** | | | | | |
| $f_{REF}$ | Single ended Inputs (LVCMOS) on AUX_IN | 2 | | 75 | MHz |
| $f_{REF}$ | Crystal single ended Inputs (AT-Cut Crystal Input) | 2 | | 42 | MHz |
| **$\overline{\text{Power\_Down}}$, $\overline{\text{SYNC}}$, REF_SEL REQUIREMENTS** | | | | | |
| $t_r$/ $t_f$ | Rise and fall time of the $\overline{\text{PD}}$, $\overline{\text{SYNC}}$, REF_SEL signal from 20% to 80% of $V_{CC}$ | | | 4 | ns |

## PHASE NOISE ANALYSIS

**Table 1. Output Phase Noise for a 491.52 MHz External Reference**

| Phase Noise Specifications under following configuration: REF = 491.52 MHz Diff, LVPECL | | | | | |
|---|---|---|---|---|---|
| **Phase Noise** | **Reference 491.52 MHz** | **LVPECL 491.52 MHz** | **LVDS 245.52 MHz** | **LVCMOS 122.88 MHz** | **Unit** |
| 10 Hz | -86 | -84 | -90 | -96 | dBc/Hz |
| 100 Hz | -100 | -100 | -105 | -111 | dBc/Hz |
| 1 kHz | -108 | -109 | -115 | -121 | dBc/Hz |
| 10 kHz | -130 | -130 | -136 | -140 | dBc/Hz |
| 100 kHz | -135 | -135 | -140 | -145 | dBc/Hz |
| 1 MHz | -138 | -142 | -143 | -148 | dBc/Hz |
| 10 MHz | -150 | -148 | -150 | -153 | dBc/Hz |
| 20 MHz | -150 | -148 | -150 | -152 | dBc/Hz |
| Jitter(RMS) 10k~20Mhz | 84 | 93 | 150 | 206 | fs |

**Table 2. Output Phase Noise for a 25 MHz Crystal Reference**

| Phase Noise Specifications under following configuration: REF = 25 MHz, SE:LVCMOS | | | | | |
|---|---|---|---|---|---|
| **Phase Noise** | **Reference 25.00 MHz** | **LVPECL 25 MHz** | **LVDS 25 MHz** | **LVCMOS 25 MHz** | **Unit** |
| 10 Hz | - | -83 | -82 | -82 | dBc/Hz |
| 100 Hz | - | -115 | -116 | -115 | dBc/Hz |
| 1 kHz | - | -142 | -142 | -141 | dBc/Hz |
| 10 kHz | - | -152 | -149 | -151 | dBc/Hz |
| 100 kHz | - | -155 | -151 | -155 | dBc/Hz |
| 1 MHz | - | -157 | -151 | -158 | dBc/Hz |
| 5 MHz | - | -157 | -151 | -158 | dBc/Hz |
| Jitter(RMS) 10k~20 MHz | - | 275 | 345 | 249 | fs |

## SPI CONTROL INTERFACE TIMING

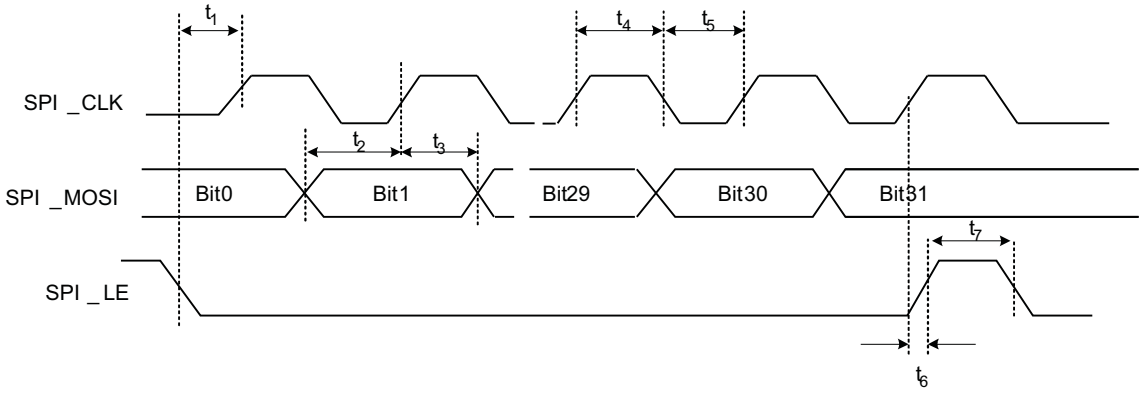



**Figure 12. Timing Diagram for SPI Write Command**

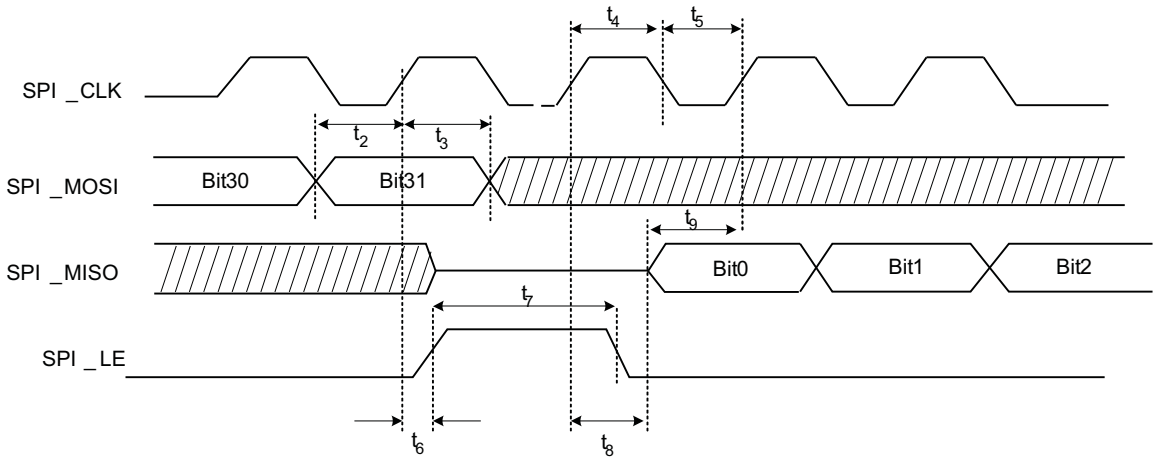



**Figure 13. Timing Diagram for SPI Read Command**

**SPI Bus Timing Characteristics**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{Clock}$ | Clock Frequency for the SPI_CLK | | | 20 | MHz |
| $t_1$ | SPI_LE to SPI_CLK setup time | 10 | | | ns |
| $t_2$ | SPI_MOSI to SPI_CLK setup time | 10 | | | ns |
| $t_3$ | SPI_MOSI to SPI_CLK hold time | 10 | | | ns |
| $t_4$ | SPI_CLK high duration | 25 | | | ns |
| $t_5$ | SPI_CLK low duration | 25 | | | ns |
| $t_6$ | SPI_CLK to SPI_LE Setup time | 10 | | | ns |
| $t_7$ | SPI_LE Pulse Width | 20 | | | ns |
| $t_8$ | SPI_MISO to SPI_CLK Data Valid (First Valid Bit after LE) | 10 | | | ns |

## DEVICE CONFIGURATION

The Functional Description Section described three different functional blocks contained within the CDCE18005. Figure 14 depicts these blocks along with a high-level functional block diagram of the circuit elements comprising each block. The balance of this section focuses on a detailed discussion of each functional block from the perspective of how to configure them.

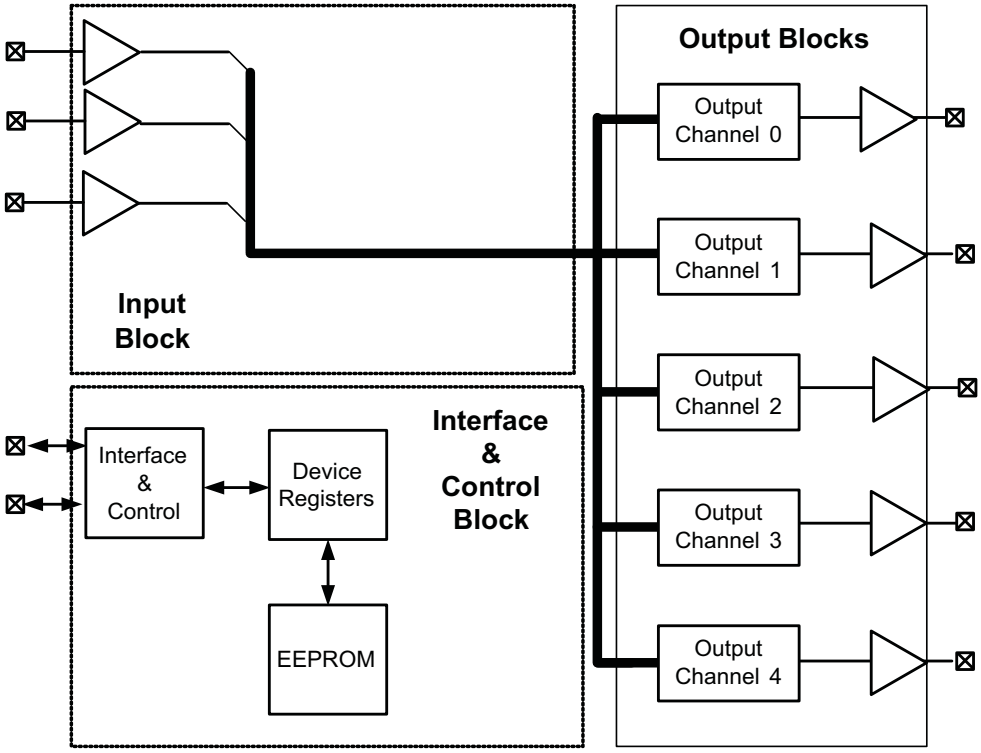



**Figure 14. CDCE18005 Circuit Blocks**

Throughout this section, references to Device Register memory locations follow the following convention:

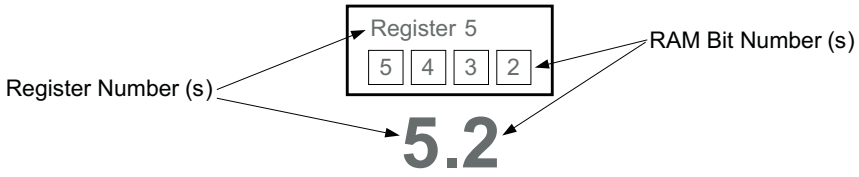



**Figure 15. Device Register Reference Convention**

## INTERFACE AND CONTROL BLOCK

The Interface & Control Block includes a SPI interface, four control pins, a non-volatile memory array in which the device stores default configuration data, and an array of device registers implemented in Static RAM. This RAM, also called the device registers, configures all hardware within the CDCE18005.

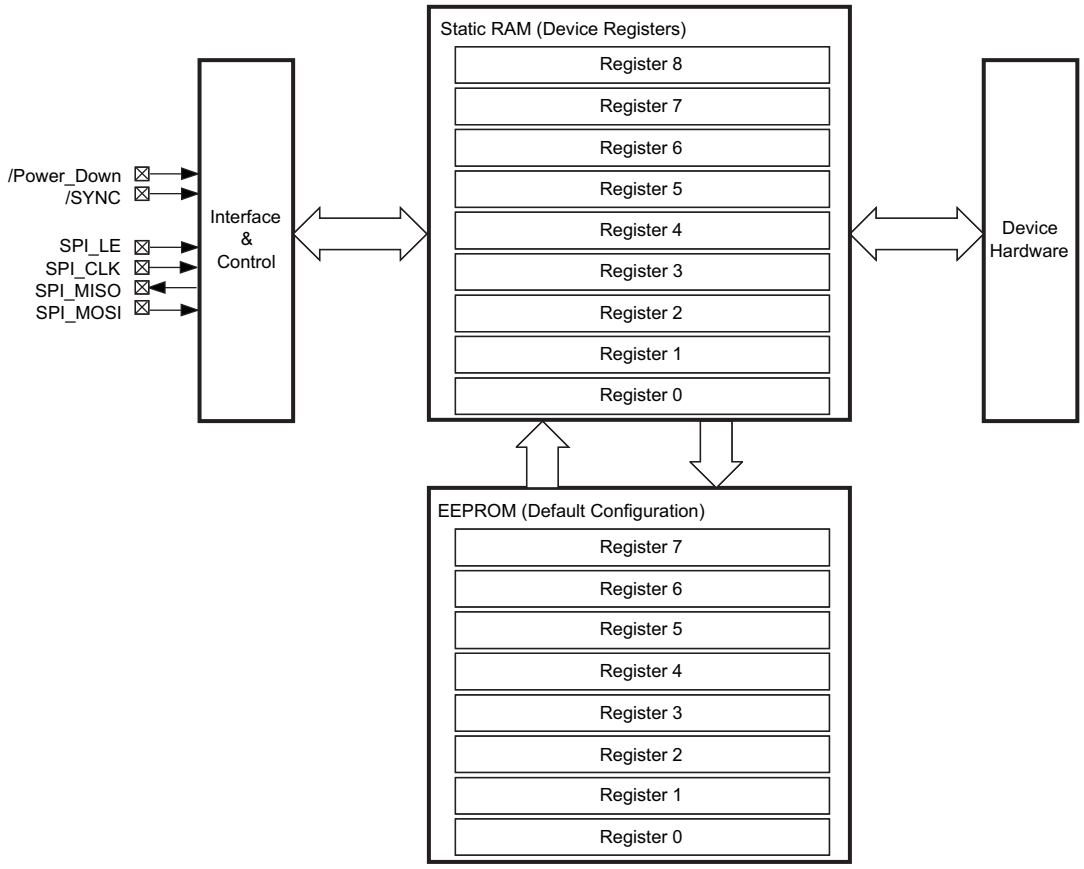



**Figure 16. CDCE18005 Interface and Control Block**

### SPI (Serial Peripheral Interface)

The serial interface of CDCE18005 is a simple bidirectional SPI interface for writing and reading to and from the device registers. It implements a low speed serial communications link in a master/slave topology in which the CDCE18005 is a slave. The SPI consists of four signals:

- **SPI_CLK:** Serial Clock (Output from Master) – the CDCE18005 clocks data in and out on the rising edge of SPI_CLK. Data transitions therefore occur on the falling edge of the clock.
- **SPI_MOSI:** Master Output Slave Input (Output from Master).
- **SPI_MISO:** Master Input Slave Output (Output from Slave).
- **SPI_LE:** Latch Enable (Output from Master). The falling edge of SPI_LE initiates a transfer. If SPI_LE is high, no data transfer can take place.

The CDCE18005 implements data fields that are 28-bits wide. In addition, it contains 9 registers, each comprising a 28 bit data field. Therefore, accessing the CDCE18005 requires that the host program append a 4-bit address field to the front of the data field as follows:

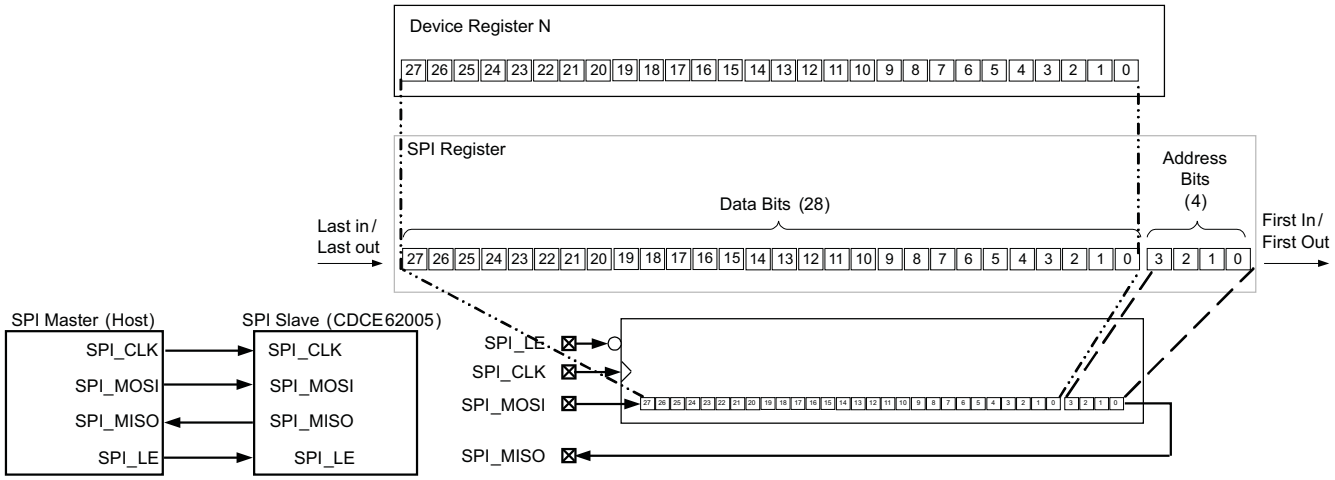



**Figure 17. CDCE18005 SPI Communications Format**

### CDCE18005 SPI Command Structure

The CDCE18005 supports four commands issued by the Master via the SPI:

- Write to RAM
- Read Command
- Copy RAM to EEPROM – unlock
- Copy RAM to EEPROM – lock

Table 3 provides a summary of the CDCE18005 SPI command structure. The host (master) constructs a Write to RAM command by specifying the appropriate register address in the address field and appends this value to the beginning of the data field. Therefore, a valid command stream must include 32 bits, transmitted LSB first. The host must issue a Read Command to initiate a data transfer from the CDCE18005 back to the host. This command specifies the address of the register of interest in the data field.

**Table 3. CDCE18005 SPI Command Structure**

| | | | Data Field (28 Bits) | | | | | | | | | | | | | | | | | | | | | | | | | | Addr Field (4 Bits) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register | Operation | NVM | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 |
| 0 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 |
| 1 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 1 |
| 2 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 1 | 0 |
| 3 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 1 | 1 |
| 4 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 | 0 | 0 |
| 5 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 | 0 | 1 |
| 6 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 | 1 | 0 |
| 7 | Write to RAM | Yes | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 | 1 | 1 |
| 8 | Status/Control | No | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 | 0 | 0 | 0 |
| Instruction | Read Command | No | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | A | A | A | 1 | 1 | 1 | 0 |
| Instruction | RAM EEPROM | Unlock(1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| Instruction | RAM EEPROM | Lock | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

(1) **CAUTION:** After execution of this command, the EEPROM is permanently locked. After locking the EEPROM, device configuration can only be changed via Write to RAM after power-up; however, the EEPROM can no longer be changed

The CDCE18005 on-board EEPROM has been factory preset to the default settings listed in the table below.

| REGISTER | DEFAULT SETTING |
|---|---|
| REG0000 | 8140000 |
| REG0001 | 8140000 |
| REG0002 | 8140000 |
| REG0003 | 8140000 |
| REG0004 | 8140000 |
| REG0005 | 0000096 |
| REG0006 | 0000000 |
| REG0007 | 9400000 |
| REG0008 (RAM) | 8000580 |

The default configurations programmed in the device is set to: PRI_REF (set to LVPECL) feeding all outputs. Output dividers are set to DIVIDE by 1. All output dividers are set to LVPECL

### Writing to the CDCE18005

Figure 18 illustrates a Write to RAM operation. Notice that the latching of the first data bit in the data stream (Bit 0) occurs on the first rising edge of SPI_CLK after SPI_LE transitions from a high to a low. For the CDCE18005, data transitions occur on the falling edge of SPI_CLK. A rising edge on SPI_LE signals to the CDCE18005 that the transmission of the last bit in the stream (Bit 31) has occurred.

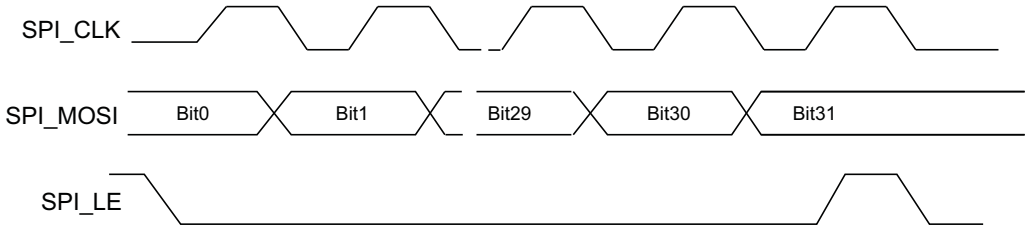



**Figure 18. CDCE18005 SPI Write Operation**

### Reading from the CDCE18005

Figure 19 shows how the CDCE18005 executes a Read Command. The SPI master first issues a Read Command to initiate a data transfer from the CDCE18005 back to the host (see Table 6). This command specifies the address of the register of interest. By transitioning SPI_LE from a low to a high, the CDCE18005 resolves the address specified in the appropriate bits of the data field. The host drives SPI_LE low and the CDCE18005 presents the data present in the register specified in the Read Command on SPI_MISO.

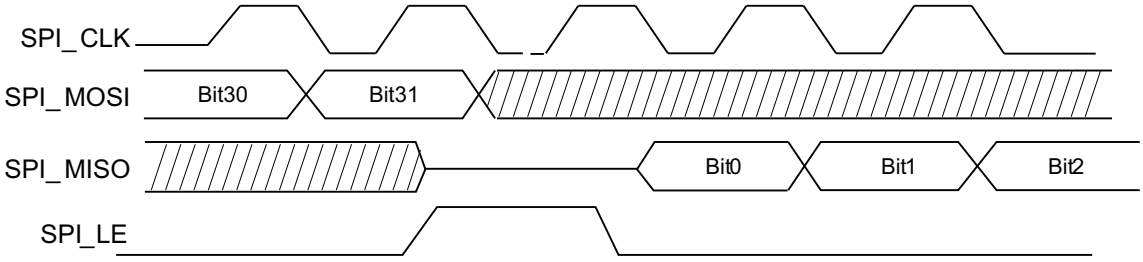



**Figure 19. CDCE18005 Read Operation**

### Writing to EEPROM

After the CDCE18005 detects a power-up and completes a reset cycle, it copies the contents of the on-board EEPROM into the Device Registers. Therefore, the CDCE18005 initializes into a known state pre-defined by the user. The host issues one of two special commands shown in Table 6 to copy the contents of Device Registers 0 through 7 (a total of 184 bits) into EERPOM. They include:

- Copy RAM to EEPROM – Unlock, Execution of this command can happen many times.
- Copy RAM to EEPROM – Lock: Execution of this command can happen only once; after which the EEPROM is **permanently locked**.

After either command is initiated, power must remain stable and the host must not access the CDCE18005 for at least 50 ms to allow the EEPROM to complete the write cycle and to avoid the possibility of EEPROM corruption.

## Device Registers: Register 0

**Table 4. CDCE18005 Register 0 Bit Definitions**

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION/FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 0 |
| 1 | | A1 | | Address 1 | 0 |
| 2 | | A2 | | Address 2 | 0 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | RESERVED | | Always Set to "0" for Proper Operation | EEPROM |
| 5 | 1 | RESERVED | | | EEPROM |
| 6 | 2 | RESERVED | | | EEPROM |
| 7 | 3 | RESERVED | | | EEPROM |
| 8 | 4 | OUTMUX0SELX | Output 0 | OUTPUT MUX “0” Select. Selects the Signal driving Output Divider ”0”<br>(X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:Reserved | EEPROM |
| 9 | 5 | OUTMUX0SELY | Output 0 | | EEPROM |
| 10 | 6 | PH0ADJC0 | Output 0 | Coarse phase adjust select for output divider “0” | EEPROM |
| 11 | 7 | PH0ADJC1 | Output 0 | | EEPROM |
| 12 | 8 | PH0ADJC2 | Output 0 | | EEPROM |
| 13 | 9 | PH0ADJC3 | Output 0 | | EEPROM |
| 14 | 10 | PH0ADJC4 | Output 0 | | EEPROM |
| 15 | 11 | PH0ADJC5 | Output 0 | | EEPROM |
| 16 | 12 | PH0ADJC6 | Output 0 | | EEPROM |
| 17 | 13 | OUT0DIVRSEL0 | Output 0 | OUTPUT DIVIDER “0” Ratio Select | EEPROM |
| 18 | 14 | OUT0DIVRSEL1 | Output 0 | | EEPROM |
| 19 | 15 | OUT0DIVRSEL2 | Output 0 | | EEPROM |
| 20 | 16 | OUT0DIVRSEL3 | Output 0 | | EEPROM |
| 21 | 17 | OUT0DIVRSEL4 | Output 0 | | EEPROM |
| 22 | 18 | OUT0DIVRSEL5 | Output 0 | | EEPROM |
| 23 | 19 | OUT0DIVRSEL6 | Output 0 | | EEPROM |
| 24 | 20 | OUT0DIVSEL | Output 0 | When set to “0”, the divider is disabled<br>When set to “1”, the divider is enabled | EEPROM |
| 25 | 21 | HiSWINGLVPECL0 | Output 0 | High Swing LVPECL When set to “1” and Normal Swing when set to “0”<br>– If LVCMOS or LVDS is selected the Output swing will stay at the same level.<br>– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”. | EEPROM |
| 26 | 22 | CMOSMODE0PX | Output 0 | LVCMOS mode select for OUTPUT “0” Positive Pin.<br>(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 27 | 23 | CMOSMODE0PY | Output 0 | | EEPROM |
| 28 | 24 | CMOSMODE0NX | Output 0 | LVCMOS mode select for OUTPUT “0” Negative Pin.<br>(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 29 | 25 | CMOSMODE0NY | Output 0 | | EEPROM |
| 30 | 26 | OUTBUFSEL0X | Output 0 | | EEPROM |
| 31 | 27 | OUTBUFSEL0Y | Output 0 | | EEPROM |

| OUTPUT TYPE | RAM BITS | | | | | |
|---|---|---|---|---|---|---|
| | 22 | 23 | 24 | 25 | 26 | 27 |
| LVPECL | 0 | 0 | 0 | 0 | 0 | 1 |
| LVDS | 0 | 1 | 0 | 1 | 1 | 1 |
| LVCMOS | *See Settings Above** | | | | 0 | 0 |
| Output Disabled | 0 | 1 | 0 | 1 | 1 | 0 |

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

## Device Registers: Register 1

**Table 5. CDCE18005 Register 1 Bit Definitions**

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION/FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 1 |
| 1 | | A1 | | Address 1 | 0 |
| 2 | | A2 | | Address 2 | 0 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | RESERVED | | Always St "0" for Proper Operation | EEPROM |
| 5 | 1 | RESERVED | | | EEPROM |
| 6 | 2 | RESERVED | | | EEPROM |
| 7 | 3 | RESERVED | | | EEPROM |
| 8 | 4 | OUTMUX1SELX | Output 1 | OUTPUT MUX “1” Select. Selects the Signal driving Output Divider ”1” (X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:Reserved | EEPROM |
| 9 | 5 | OUTMUX1SELY | Output 1 | | EEPROM |
| 10 | 6 | PH1ADJC0 | Output 1 | Coarse phase adjust select for output divider “1” | EEPROM |
| 11 | 7 | PH1ADJC1 | Output 1 | | EEPROM |
| 12 | 8 | PH1ADJC2 | Output 1 | | EEPROM |
| 13 | 9 | PH1ADJC3 | Output 1 | | EEPROM |
| 14 | 10 | PH1ADJC4 | Output 1 | | EEPROM |
| 15 | 11 | PH1ADJC5 | Output 1 | | EEPROM |
| 16 | 12 | PH1ADJC6 | Output 1 | | EEPROM |
| 17 | 13 | OUT1DIVRSEL0 | Output 1 | OUTPUT DIVIDER “1” Ratio Select | EEPROM |
| 18 | 14 | OUT1DIVRSEL1 | Output 1 | | EEPROM |
| 19 | 15 | OUT1DIVRSEL2 | Output 1 | | EEPROM |
| 20 | 16 | OUT1DIVRSEL3 | Output 1 | | EEPROM |
| 21 | 17 | OUT1DIVRSEL4 | Output 1 | | EEPROM |
| 22 | 18 | OUT1DIVRSEL5 | Output 1 | | EEPROM |
| 23 | 19 | OUT1DIVRSEL6 | Output 1 | | EEPROM |
| 24 | 20 | OUT1DIVSEL | Output 1 | When set to “0”, the divider is disabled<br>When set to “1”, the divider is enabled | EEPROM |
| 25 | 21 | HiSWINGLVPECL1 | Output 1 | High Swing LVPECL When set to “1” and Normal Swing when set to “0”<br>– If LVCMOS or LVDS is selected the Output swing will stay at the same level.<br>– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”. | EEPROM |
| 26 | 22 | CMOSMODE1PX | Output 1 | LVCMOS mode select for OUTPUT “1” Positive Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 27 | 23 | CMOSMODE1PY | Output 1 | | EEPROM |
| 28 | 24 | CMOSMODE1NX | Output 1 | LVCMOS mode select for OUTPUT “1” Negative Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 29 | 25 | CMOSMODE1NY | Output 1 | | EEPROM |
| 30 | 26 | OUTBUFSEL1X | Output 1 | | EEPROM |
| 31 | 27 | OUTBUFSEL1Y | Output 1 | | EEPROM |

| OUTPUT TYPE | RAM BITS | | | | | |
|---|---|---|---|---|---|---|
| | 22 | 23 | 24 | 25 | 26 | 27 |
| LVPECL | 0 | 0 | 0 | 0 | 0 | 1 |
| LVDS | 0 | 1 | 0 | 1 | 1 | 1 |
| LVCMOS | *See Settings Above** | | | | 0 | 0 |
| Output Disabled | 0 | 1 | 0 | 1 | 1 | 0 |

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

## Device Registers: Register 2

### Table 6. CDCE18005 Register 2 Bit Definitions

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION/FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 0 |
| 1 | | A1 | | Address 1 | 1 |
| 2 | | A2 | | Address 2 | 0 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | RESERVED | | Always Set to "0" for Proper Operation | EEPROM |
| 5 | 1 | RESERVED | | | EEPROM |
| 6 | 2 | RESERVED | | | EEPROM |
| 7 | 3 | RESERVED | | | EEPROM |
| 8 | 4 | OUTMUX2SELX | Output 2 | OUTPUT MUX “2” Select. Selects the Signal driving Output Divider ”2”<br>(X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:Reserved | EEPROM |
| 9 | 5 | OUTMUX2SELY | Output 2 | | EEPROM |
| 10 | 6 | PH2ADJC0 | Output 2 | Coarse phase adjust select for output divider “2” | EEPROM |
| 11 | 7 | PH2ADJC1 | Output 2 | | EEPROM |
| 12 | 8 | PH2ADJC2 | Output 2 | | EEPROM |
| 13 | 9 | PH2ADJC3 | Output 2 | | EEPROM |
| 14 | 10 | PH2ADJC4 | Output 2 | | EEPROM |
| 15 | 11 | PH2ADJC5 | Output 2 | | EEPROM |
| 16 | 12 | PH2ADJC6 | Output 2 | | EEPROM |
| 17 | 13 | OUT2DIVRSEL0 | Output 2 | OUTPUT DIVIDER “2” Ratio Select | EEPROM |
| 18 | 14 | OUT2DIVRSEL1 | Output 2 | | EEPROM |
| 19 | 15 | OUT2DIVRSEL2 | Output 2 | | EEPROM |
| 20 | 16 | OUT2DIVRSEL3 | Output 2 | | EEPROM |
| 21 | 17 | OUT2DIVRSEL4 | Output 2 | | EEPROM |
| 22 | 18 | OUT2DIVRSEL5 | Output 2 | | EEPROM |
| 23 | 19 | OUT2DIVRSEL6 | Output 2 | | EEPROM |
| 24 | 20 | OUT2DIVSEL | Output 2 | When set to “0”, the divider is disabled<br>When set to “1”, the divider is enabled | EEPROM |
| 25 | 21 | HiSWINGLVPEC2 | Output 2 | High Swing LVPECL When set to “1” and Normal Swing when set to “0”<br>– If LVCMOS or LVDS is selected the Output swing will stay at the same level.<br>– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”. | EEPROM |
| 26 | 22 | CMOSMODE2PX | Output 2 | LVCMOS mode select for OUTPUT “2” Positive Pin.<br>(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 27 | 23 | CMOSMODE2PY | Output 2 | | EEPROM |
| 28 | 24 | CMOSMODE2NX | Output 2 | LVCMOS mode select for OUTPUT “2” Negative Pin.<br>(X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 29 | 25 | CMOSMODE2NY | Output 2 | | EEPROM |
| 30 | 26 | OUTBUFSEL2X | Output 2 | | EEPROM |
| 31 | 27 | OUTBUFSEL2Y | Output 2 | | EEPROM |

| OUTPUT TYPE | RAM BITS | | | | | |
|---|---|---|---|---|---|---|
| | 22 | 23 | 24 | 25 | 26 | 27 |
| LVPECL | 0 | 0 | 0 | 0 | 0 | 1 |
| LVDS | 0 | 1 | 0 | 1 | 1 | 1 |
| LVCMOS | *See Settings Above** | | | | 0 | 0 |
| Output Disabled | 0 | 1 | 0 | 1 | 1 | 0 |

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

## Device Registers: Register 3

**Table 7. CDCE18005 Register 3 Bit Definitions**

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION/FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 1 |
| 1 | | A1 | | Address 1 | 1 |
| 2 | | A2 | | Address 2 | 0 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | RESERVED | | Always Set to "0" for Proper Operation | EEPROM |
| 5 | 1 | RESERVED | | | EEPROM |
| 6 | 2 | RESERVED | | | EEPROM |
| 7 | 3 | RESERVED | | | EEPROM |
| 8 | 4 | OUTMUX3SELX | Output 3 | OUTPUT MUX “3” Select. Selects the Signal driving Output Divider ”3” (X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:Reserved | EEPROM |
| 9 | 5 | OUTMUX3SELY | Output 3 | | EEPROM |
| 10 | 6 | PH3ADJC0 | Output 3 | Coarse phase adjust select for output divider “3” | EEPROM |
| 11 | 7 | PH3ADJC1 | Output 3 | | EEPROM |
| 12 | 8 | PH3ADJC2 | Output 3 | | EEPROM |
| 13 | 9 | PH3ADJC3 | Output 3 | | EEPROM |
| 14 | 10 | PH3ADJC4 | Output 3 | | EEPROM |
| 15 | 11 | PH3ADJC5 | Output 3 | | EEPROM |
| 16 | 12 | PH3ADJC6 | Output 3 | | EEPROM |
| 17 | 13 | OUT3DIVRSEL0 | Output 3 | OUTPUT DIVIDER “3” Ratio Select | EEPROM |
| 18 | 14 | OUT3DIVRSEL1 | Output 3 | | EEPROM |
| 19 | 15 | OUT3DIVRSEL2 | Output 3 | | EEPROM |
| 20 | 16 | OUT3DIVRSEL3 | Output 3 | | EEPROM |
| 21 | 17 | OUT3DIVRSEL4 | Output 3 | | EEPROM |
| 22 | 18 | OUT3DIVRSEL5 | Output 3 | | EEPROM |
| 23 | 19 | OUT3DIVRSEL6 | Output 3 | | EEPROM |
| 24 | 20 | OUT3DIVSEL | Output 3 | When set to “0”, the divider is disabled<br>When set to “1”, the divider is enabled | EEPROM |
| 25 | 21 | HiSWINGLVPEC3 | Output 3 | High Swing LVPECL When set to “1” and Normal Swing when set to “0”<br>– If LVCMOS or LVDS is selected the Output swing will stay at the same level.<br>– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”. | EEPROM |
| 26 | 22 | CMOSMODE3PX | Output 3 | LVCMOS mode select for OUTPUT “3” Positive Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 27 | 23 | CMOSMODE3PY | Output 3 | | EEPROM |
| 28 | 24 | CMOSMODE3NX | Output 3 | LVCMOS mode select for OUTPUT “3” Negative Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 29 | 25 | CMOSMODE3NY | Output 3 | | EEPROM |
| 30 | 26 | OUTBUFSEL3X | Output 3 | | EEPROM |
| 31 | 27 | OUTBUFSEL3Y | Output 3 | | EEPROM |

| OUTPUT TYPE | RAM BITS | | | | | |
|---|---|---|---|---|---|---|
| | 22 | 23 | 24 | 25 | 26 | 27 |
| LVPECL | 0 | 0 | 0 | 0 | 0 | 1 |
| LVDS | 0 | 1 | 0 | 1 | 1 | 1 |
| LVCMOS | *See Settings Above** | | | | 0 | 0 |
| Output Disabled | 0 | 1 | 0 | 1 | 1 | 0 |

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

## Device Registers: Register 4

### Table 8. CDCE18005 Register 4 Bit Definitions

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION/FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 0 |
| 1 | | A1 | | Address 1 | 0 |
| 2 | | A2 | | Address 2 | 1 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | RESERVED | | Must be set to "0" for proper operation | EEPROM |
| 5 | 1 | RESERVED | | | EEPROM |
| 6 | 2 | RESERVED | | | EEPROM |
| 7 | 3 | RESERVED | | | EEPROM |
| 8 | 4 | OUTMUX4SELX | Output 4 | OUTPUT MUX “4” Select. Selects the Signal driving Output Divider ”4” (X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:Reserved | EEPROM |
| 9 | 5 | OUTMUX4SELY | Output 4 | | EEPROM |
| 10 | 6 | PH4ADJC0 | Output 4 | Coarse phase adjust select for output divider “4” | EEPROM |
| 11 | 7 | PH4ADJC1 | Output 4 | | EEPROM |
| 12 | 8 | PH4ADJC2 | Output 4 | | EEPROM |
| 13 | 9 | PH4ADJC3 | Output 4 | | EEPROM |
| 14 | 10 | PH4ADJC4 | Output 4 | | EEPROM |
| 15 | 11 | PH4ADJC5 | Output 4 | | EEPROM |
| 16 | 12 | PH4ADJC6 | Output 4 | | EEPROM |
| 17 | 13 | OUT4DIVRSEL0 | Output 4 | OUTPUT DIVIDER “4” Ratio Select | EEPROM |
| 18 | 14 | OUT4DIVRSEL1 | Output 4 | | EEPROM |
| 19 | 15 | OUT4DIVRSEL2 | Output 4 | | EEPROM |
| 20 | 16 | OUT4DIVRSEL3 | Output 4 | | EEPROM |
| 21 | 17 | OUT4DIVRSEL4 | Output 4 | | EEPROM |
| 22 | 18 | OUT4DIVRSEL5 | Output 4 | | EEPROM |
| 23 | 19 | OUT4DIVRSEL6 | Output 4 | | EEPROM |
| 24 | 20 | OUT4DIVSEL | Output 4 | When set to “0”, the divider is disabled<br>When set to “1”, the divider is enabled | EEPROM |
| 25 | 21 | HiSWINGLVPEC4 | Output 4 | High Swing LVPECL When set to “1” and Normal Swing when set to “0”<br>– If LVCMOS or LVDS is selected the Output swing will stay at the same level.<br>– If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”. | EEPROM |
| 26 | 22 | CMOSMODE4PX | Output 4 | LVCMOS mode select for OUTPUT “4” Positive Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 27 | 23 | CMOSMODE4PY | Output 4 | | EEPROM |
| 28 | 24 | CMOSMODE4NX | Output 4 | LVCMOS mode select for OUTPUT “3” Negative Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State | EEPROM |
| 29 | 25 | CMOSMODE4NY | Output 4 | | EEPROM |
| 30 | 26 | OUTBUFSEL4X | Output 4 | | EEPROM |
| 31 | 27 | OUTBUFSEL4Y | Output 4 | | EEPROM |

| OUTPUT TYPE | RAM BITS | | | | | |
|---|---|---|---|---|---|---|
| | 22 | 23 | 24 | 25 | 26 | 27 |
| **LVPECL** | 0 | 0 | 0 | 0 | 0 | 1 |
| **LVDS** | 0 | 1 | 0 | 1 | 1 | 1 |
| **LVCMOS** | *See Settings Above** | | | | 0 | 0 |
| **Output Disabled** | 0 | 1 | 0 | 1 | 1 | 0 |

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

## Device Registers: Register 5

**Table 9. CDCE18005 Register 5 Bit Definitions**

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION/FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 1 |
| 1 | | A1 | | Address 1 | 0 |
| 2 | | A2 | | Address 2 | 1 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | INBUFSELX | INBUFSELX | Input Buffer Select (LVPECL,LVDS or LVCMOS)<br>XY(01 ) LVPECL, (11) LVDS, (00) LVCMOS- Input is Positive Pin | EEPROM |
| 5 | 1 | INBUFSELY | INBUFSELY | | EEPROM |
| 6 | 2 | SYNCSEL1 | Output Divider Synchronization | SYNCSEL(1,2)= 10 :Output divider sync to Primary input<br>SYNCSEL(1,2)= 01 :Output divider sync to Secondary input<br>SYNCSEL(1,2)= 00 :Output divider sync to Auxiliary input | EEPROM |
| 7 | 3 | SYNCSEL2 | | | EEPROM |
| 8 | 4 | RESERVED | | Always Set to **"1"** for Proper Operation | EEPROM |
| 9 | 5 | RESERVED | | Always Set to **"0"** for Proper Operation | EEPROM |
| 10 | 6 | ACDCSEL | Input Buffers | If Set to “1” DC Termination, If set to “0” AC Termination | EEPROM |
| 11 | 7 | HYSTEN | Input Buffers | If Set to “1” Input Buffers Hysteresis Enabled. It is not recommended that Hysteresis be disabled. | EEPROM |
| 12 | 8 | PRI_TERMSEL | Input Buffers | If Set to “0” Primary Input Buffer Internal Termination Enabled<br>If set to “1” Primary Internal Termination circuitry Disabled | EEPROM |
| 13 | 9 | PRIINVBB | Input Buffers | If Set to “1” Primary Input Negative Pin Biased with Internal VBB Voltage. | EEPROM |
| 14 | 10 | SECINVBB | Input Buffers | If Set to “1” Secondary Input Negative Pin Biased with Internal VBB Voltage | EEPROM |
| 15 | 11 | FAILSAFE | Input Buffers | If Set to “1” Fail Safe is Enabled for all Input Buffers configured as LVDS, DC Coupling only. | EEPROM |
| 16 | 12 | RESERVED | - - - - | Must be set to "0" for proper operation | EEPROM |
| 17 | 13 | RESERVED | | | EEPROM |
| 18 | 14 | RESERVED | | | EEPROM |
| 19 | 15 | RESERVED | | | EEPROM |
| 20 | 16 | RESERVED | | | EEPROM |
| 21 | 17 | RESERVED | | | EEPROM |
| 22 | 18 | RESERVED | | | EEPROM |
| 23 | 19 | RESERVED | | | EEPROM |
| 24 | 20 | RESERVED | | | EEPROM |
| 25 | 21 | RESERVED | | | EEPROM |
| 26 | 22 | RESERVED | | | EEPROM |
| 27 | 23 | RESERVED | | | EEPROM |
| 28 | 24 | RESERVED | | | EEPROM |
| 29 | 25 | RESERVED | | | EEPROM |
| 30 | 26 | RESERVED | | | EEPROM |
| 31 | 27 | RESERVED | | | EEPROM |

## Device Registers: Register 6

**Table 10. CDCE18005 Register 6 Bit Definitions**

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION/FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 0 |
| 1 | | A1 | | Address 1 | 1 |
| 2 | | A2 | | Address 2 | 1 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | RESERVED | | Must be set to "0" | EEPROM |
| 5 | 1 | RESERVED | | | EEPROM |
| 6 | 2 | RESERVED | | | EEPROM |
| 7 | 3 | RESERVED | | | EEPROM |
| 8 | 4 | RESERVED | | | EEPROM |
| 9 | 5 | RESERVED | | | EEPROM |
| 10 | 6 | RESERVED | | | EEPROM |
| 11 | 7 | RESERVED | | | EEPROM |
| 12 | 8 | RESERVED | | | EEPROM |
| 13 | 9 | RESERVED | | | EEPROM |
| 14 | 10 | RESERVED | | | EEPROM |
| 15 | 11 | RESERVED | | | EEPROM |
| 16 | 12 | SEC_TERMSEL | Input Buffers | If Set to “0” Secondary Input Buffer Internal Termination Enabled<br>If set to “1” Secondary Internal Termination circuitry Disabled | EEPROM |
| 17 | 13 | RESERVED | | Must be set to "0" | EEPROM |
| 18 | 14 | RESERVED | | | EEPROM |
| 19 | 15 | RESERVED | | | EEPROM |
| 20 | 16 | RESERVED | | | EEPROM |
| 21 | 17 | RESERVED | | | EEPROM |
| 22 | 18 | RESERVED | | | EEPROM |
| 23 | 19 | RESERVED | | | EEPROM |
| 24 | 20 | RESERVED | | | EEPROM |
| 25 | 21 | RESERVED | | | EEPROM |
| 26 | 22 | RESERVED | | | EEPROM |
| 27 | 23 | RESERVED | | | EEPROM |
| 28 | 24 | AUXOUTEN | Output AUX | Enable Auxiliary Output when set to “1” | EEPROM |
| 29 | 25 | AUXFEEDSEL | Output AUX | Select the Output that will driving the AUX Output;<br>Low for Selecting Output Divider “2” and High for Selecting Output Divider “3” | EEPROM |
| 30 | 26 | RESERVED | | Must be set to "0" | EEPROM |
| 31 | 27 | RESERVED | | Must be set to "0" | EEPROM |

## Device Registers: Register 7

**Table 11. CDCE18005 Register 7 Bit Definitions**

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION/FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 1 |
| 1 | | A1 | | Address 1 | 1 |
| 2 | | A2 | | Address 2 | 1 |
| 3 | | A3 | | Address 3 | 0 |
| 4 | 0 | RESERVED | | | EEPROM |
| 5 | 1 | RESERVED | | | EEPROM |
| 6 | 2 | RESERVED | | | EEPROM |
| 7 | 3 | RESERVED | | | EEPROM |
| 8 | 4 | RESERVED | | | EEPROM |
| 9 | 5 | RESERVED | | | EEPROM |
| 10 | 6 | RESERVED | | | EEPROM |
| 11 | 7 | RESERVED | | | EEPROM |
| 12 | 8 | RESERVED | | | EEPROM |
| 13 | 9 | RESERVED | | | EEPROM |
| 14 | 10 | RESERVED | | | EEPROM |
| 15 | 11 | RESERVED | | Always Set to "0" for Proper Operation | EEPROM |
| 16 | 12 | RESERVED | | | EEPROM |
| 17 | 13 | RESERVED | | | EEPROM |
| 18 | 14 | RESERVED | | | EEPROM |
| 19 | 15 | RESERVED | | | EEPROM |
| 20 | 16 | RESERVED | | | EEPROM |
| 21 | 17 | RESERVED | | | EEPROM |
| 22 | 18 | RESERVED | | | EEPROM |
| 23 | 19 | RESERVED | | | EEPROM |
| 24 | 20 | RESERVED | | | EEPROM |
| 25 | 21 | RESERVED | | | EEPROM |
| 26 | 22 | TESTMUX1 | Diagnostics | Set to “1” | EEPROM |
| 27 | 23 | RESERVED | | Always Set to "0" for Proper Operation | EEPROM |
| 28 | 24 | TEXTMUX2 | Diagnostics | Set to “1” | EEPROM |
| 29 | 25 | RESERVED | | Always Set to "0" for Proper Operation | EEPROM |
| 30 | 26 | EPUNLOCK | Status | EEPROM Unlock | RAM |
| 31 | 27 | EPSTATUS | Status | EEPROM Status | RAM |

## Device Registers: Register 8

**Table 12. CDCE18005 Register 8 Bit Definitions**

| SPI BIT | RAM BIT | BIT NAME | RELATED BLOCK | DESCRIPTION/FUNCTION | |
|---|---|---|---|---|---|
| 0 | | A0 | | Address 0 | 0 |
| 1 | | A1 | | Address 1 | 0 |
| 2 | | A2 | | Address 2 | 0 |
| 3 | | A3 | | Address 3 | 1 |
| 4 | 0 | RESERVED | | | RAM |
| 5 | 1 | RESERVED | | | RAM |
| 6 | 2 | RESERVED | | | RAM |
| 7 | 3 | RESERVED | | *TI Test Registers. For TI Use Only* | RAM |
| 8 | 4 | RESERVED | | | RAM |
| 9 | 5 | RESERVED | | | RAM |
| 10 | 6 | RESERVED | | | RAM |
| 11 | 7 | $\overline{\text{SLEEP}}$ | Status | Set Device Sleep mode On when set to “0”, Normal Mode when set to “1” | RAM |
| 12 | 8 | $\overline{\text{SYNC}}$ | Status | If set to “0” this bit forces “/SYNC ; Set to “1” to exit the Synchronization State. | RAM |
| 13 | 9 | RESERVED | | | RAM |
| 14 | 10 | VERSION0 | Tie off | Silicon Revision | RAM |
| 15 | 11 | VERSION1 | Tie off | Silicon Revision | RAM |
| 16 | 12 | VERSION2 | Tie off | Silicon Revision | RAM |
| 17 | 13 | RESERVED | | | RAM |
| 18 | 14 | RESERVED | | | RAM |
| 19 | 15 | RESERVED | | | RAM |
| 20 | 16 | RESERVED | | | RAM |
| 21 | 17 | RESERVED | | | RAM |
| 22 | 18 | RESERVED | | | RAM |
| 23 | 19 | RESERVED | | | RAM |
| 24 | 20 | RESERVED | | *TI Test Registers. For TI Use Only* | RAM |
| 25 | 21 | RESERVED | | | RAM |
| 26 | 22 | RESERVED | | | RAM |
| 27 | 23 | RESERVED | | | RAM |
| 28 | 24 | RESERVED | | | RAM |
| 29 | 25 | RESERVED | | | RAM |
| 30 | 26 | RESERVED | | | RAM |
| 31 | 27 | RESERVED | | | RAM |

## Device Control

Figure 20 provides a conceptual explanation of the CDCE18005 Device operation. Table 13 defines how the device behaves in each of the operational states.

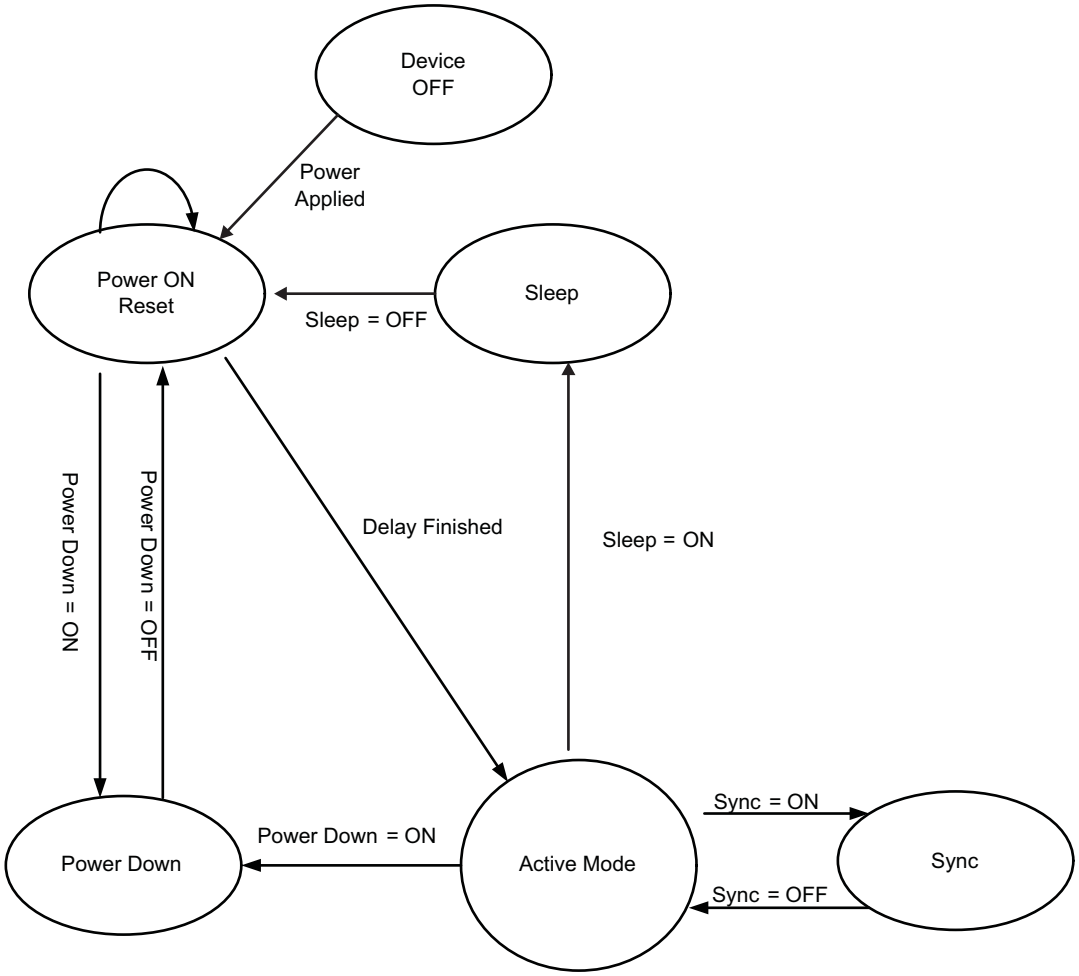



**Figure 20. CDCE18005 Device State Control Diagram**

**Table 13. CDCE18005 Device State Definitions**

| State | Device Behavior | Entered Via | Exited Via | Status | | |
|---|---|---|---|---|---|---|
| | | | | SPI Port | Output Divider | Output Buffer |
| Power-On Reset | After device power supply reaches approximately 2.35V, the contents of EEPROM are copied into the Device Registers, thereby initializing the device hardware . | Power applied to the device or upon exit from Power Down State via the Power_Down pin set HIGH. | Power On Reset and EEPROM loading delays are finished OR the Power_Down pin is set LOW. | OFF | Disabled | OFF |
| Active Mode | Normal Operation | Sync = OFF (from Sync State). | Sync, Power Down, Sleep, or Manual Recalibration activated. | ON | Disabled or Enabled | Disabled or Enabled |
| Power Down | Used to shut down all hardware and Resets the device after exiting the Power Down State. Therefore, the EEPROM contents will eventually be copied into RAM after the Power Down State is exited. | $\overline{\text{Power\_Down}}$ pin is pulled LOW. | $\overline{\text{Power\_Down}}$ pin is pulled HIGH. | ON | Disabled | Disabled |
| Sleep | Identical to the Power Down State except the EEPROM contents are not copied into RAM. | $\overline{\text{SLEEP}}$ bit in device register 8 bit 7 is set LOW. | $\overline{\text{SLEEP}}$ bit in device register 8 bit 7 is set HIGH. | ON | Disabled | Disabled |

**Table 13. CDCE18005 Device State Definitions (continued)**

| State | Device Behavior | Entered Via | Exited Via | Status | | |
|---|---|---|---|---|---|---|
| | | | | SPI Port | Output Divider | Output Buffer |
| Sync | Sync synchronizes all output dividers so that they begin counting at the same time. Note: this operation is performed automatically each time a divider register is accessed. | $\overline{\text{SYNC}}$ Bit in device register 8 bit 8 is set LOW or $\overline{\text{SYNC}}$ pin is pulled LOW | $\overline{\text{SYNC}}$ Bit in device register 8 bit 8 is set HIGH or $\overline{\text{SYNC}}$ pin is pulled HIGH | ON | Disabled | Disabled |

## External Control Pins

### $\overline{\text{Power\_Down}}$

The Power_Down pin places the CDCE18005 into the power down state. Additionally, the CDCE18005 loads the contents of the EEPROM into RAM after the Power_Down pin is de-asserted; therefore, it is used to initialize the device after power is applied. SPI_LE signal has to be HIGH in order for EEPROM to load correctly during the rising edge of Power_Down.

### $\overline{\text{SYNC}}$

The $\overline{\text{SYNC}}$ pin (Active LOW) has a complementary register location located in Device Register 8 bit 8. When enabled, Sync synchronizes all output dividers so that they begin counting simultaneously. Further, $\overline{\text{SYNC}}$ disables all outputs when in the active. State.

## INPUT BLOCK

The Input Block includes two Universal Input Buffers, an Auxiliary Input. The Input Block drives three different clock signals onto the Internal Clock Distribution Bus.

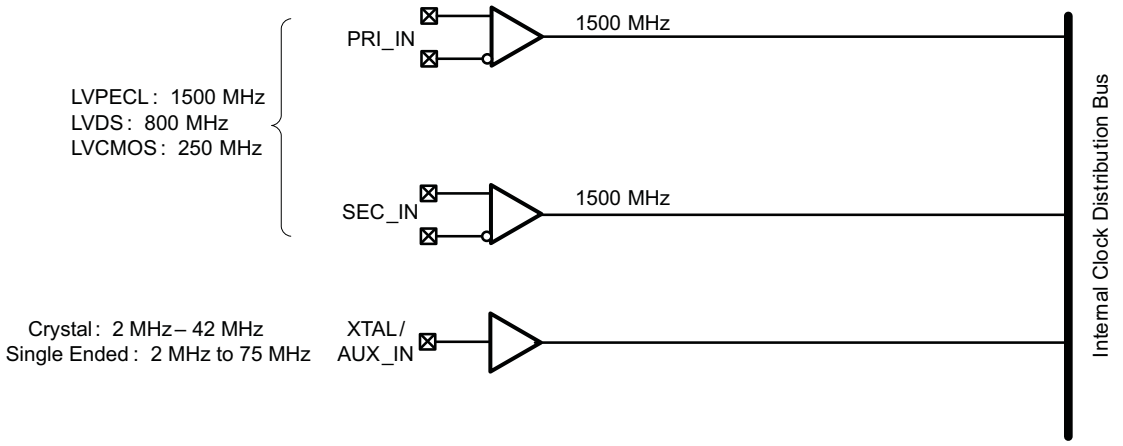
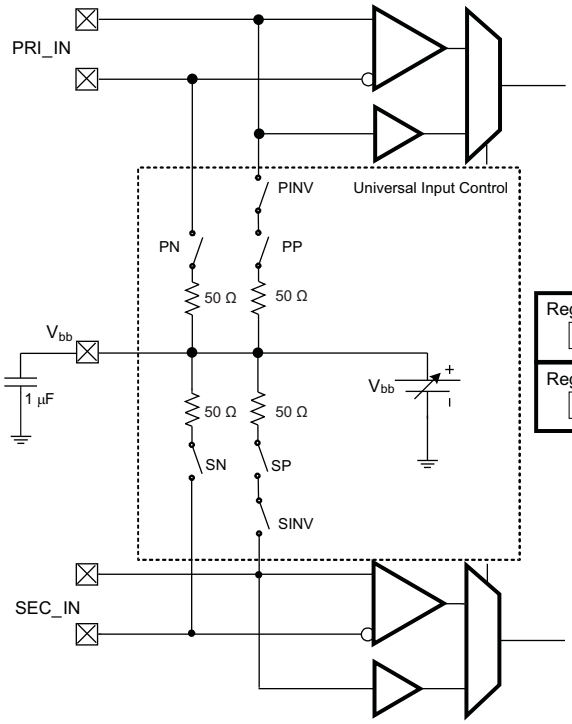



**Figure 21. CDCE18005 Input Block With References to Registers**

### Universal Input Buffers (UIB)

Figure 22 shows the key elements of a universal input buffer. A UIB supports multiple formats along with different termination and coupling schemes. The CDCE18005 implements the UIB by including on board switched termination, a programmable bias voltage generator, and an output multiplexer. The CDCE18005 provides a high degree of configurability on the UIB to facilitate most existing clock input formats.




| Settings | | | Nominal Vbb |
|---|---|---|---|
| 5.1 INBUFSELY | 5.0 INBUFSELX | 5.6 ACDCSEL | |
| 1 | 0 | 0 | 1.9V |
| 1 | 0 | 1 | 1.2V |
| 1 | 1 | 0 | 1.2V |
| 1 | 1 | 1 | 1.2V |

Register 6

| 12 |
|---|

Register 5

| 10 | 9 | 8 | 7 | 6 | 1 | 0 |
|---|---|---|---|---|---|---|

| Settings | | | | SWITCH Status | | |
|---|---|---|---|---|---|---|
| 5.0 INBUFSELX | 5.1 INBUFSELY | 5.8, 6.12 TERMSEL | 5.9,5.10 INVBB | P | N | INV |
| 0 | 0 | X | X | OFF | OFF | OFF |
| X | X | 1 | X | OFF | OFF | OFF |
| X | 1 | 0 | 0 | ON | ON | ON |
| X | 1 | 0 | 1 | ON | ON | OFF |

**Figure 22. CDCE18005 Universal Input Buffer**

Table 14 lists several settings for many possible clock input scenarios. Note that the two universal input buffers share the Vbb generator. Therefore, if both inputs use internal termination, they must use the same configuration mode (LVDS, LVPECL, or LVCMOS). If the application requires different modes (e.g. LVDS and LVPECL) then one of the two inputs must implement external termination.

**Table 14. CDCE18005 Universal Input Buffer Configuration Matrix**

| PRI_IN CONFIGURATION MATRIX | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | SETTINGS | | | | | | CONFIGURATION | | | | |
| Register.Bit → | 5.7 | 5.1 | 5.0 | 5.8 | 5.9 | 5.6 | | | | | |
| Bit Name → | HYSTEN | INBUFSELY | INBUFSELX | PRI_TERMSEL | PRIINVBB | ACDCSEL | Hysteresis | Mode | Coupling | Termination | Vbb |
| | 1 | 0 | 0 | X | X | X | ENABLED | LVCMOS | DC | N/A | — |
| | 1 | 1 | 0 | 0 | 0 | 0 | ENABLED | LVPECL | AC | Internal | 1.9V |
| | 1 | 1 | 0 | 0 | 0 | 1 | ENABLED | LVPECL | DC | Internal | 1.2V |
| | 1 | 1 | 0 | 1 | X | X | ENABLED | LVPECL | — | External | — |
| | 1 | 1 | 1 | 0 | 0 | 0 | ENABLED | LVDS | AC | Internal | 1.2V |
| | 1 | 1 | 1 | 0 | 0 | 1 | ENABLED | LVDS | DC | Internal | 1.2V |
| | 1 | 1 | 1 | 1 | X | X | ENABLED | LVDS | — | External | — |
| | 0 | X | X | X | X | X | OFF | — | — | — | — |
| | 1 | X | X | X | X | X | ENABLED | — | — | — | — |
| SEC_IN CONFIGURATION MATRIX | | | | | | | | | | | |
| | SETTINGS | | | | | | CONFIGURATION | | | | |
| Register.Bit → | 5.7 | 5.1 | 5.0 | 6.12 | 5.10 | 5.6 | | | | | |
| Bit Name → | HYSTEN | INBUFSELY | INBUFSELX | SEC_TERMSEL | SECINVBB | ACDCSEL | Hysteresis | Mode | Coupling | Termination | Vbb |
| | 1 | 0 | 0 | X | X | X | ENABLED | LVCMOS | DC | N/A | — |
| | 1 | 1 | 0 | 0 | 0 | 0 | ENABLED | LVPECL | AC | Internal | 1.9V |
| | 1 | 1 | 0 | 0 | 0 | 1 | ENABLED | LVPECL | DC | Internal | 1.2V |
| | 1 | 1 | 0 | 1 | X | X | ENABLED | LVPECL | — | External | — |
| | 1 | 1 | 1 | 0 | 0 | 0 | ENABLED | LVDS | AC | Internal | 1.2V |
| | 1 | 1 | 1 | 0 | 0 | 1 | ENABLED | LVDS | DC | Internal | 1.2V |
| | 1 | 1 | 1 | 1 | X | X | ENABLED | LVDS | — | External | — |
| | 0 | X | X | X | X | X | OFF | — | — | — | — |
| | 1 | X | X | X | X | X | ENABLED | — | — | — | — |

### LVDS Fail Safe Mode

Differential data line receivers can switch on noise in the absence of an input signal. This occurs when the bus driver is turned off or the interconnect is damaged or missing. Traditionally the solution to this problem involves incorporating an external resistor network on the receiver input. This network applies a steady-state bias voltage to the input pins. The additional cost of the external components notwithstanding, the use of such a network lowers input signal magnitude and thus reduces the differential noise margin. The CDCE18005 provides internal failsafe circuitry on all LVDS inputs if enabled as shown in Table 15 for DC termination only.

**Table 15. LVDS Failsafe Settings**

| Bit Name →<br>Register.Bit → | FAILSAFE<br>5.11 | LVDS Failsafe |
|---|---|---|
| | 0 | Disabled for all inputs |
| | 1 | Enabled for all inputs |

### Auxiliary Input Port

The auxiliary input on the CDCE18005 is designed to connect to an AT-Cut Crystal with a total load capacitance ($C_L$) of 0 to 10 pF. One side of the crystal connects to Ground while the other side connects to the Auxiliary input of the device. The circuit works optimally between 20 to 40 MHz but it can accept crystals from 2 to 42 MHz.

Since the Auxiliary input operates between 0 and 2 V with a crystal, it can accept single-ended signals (e.g. LVCMOS). Electrically, it is equivalent to an LVCMOS input buffer with 10 pF of input capacitance.

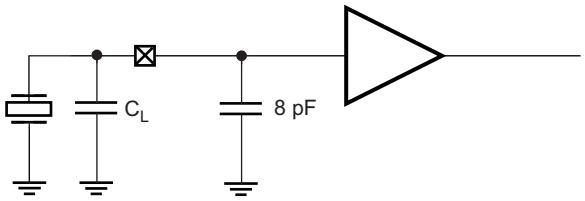



**Figure 23. CDCE18005 Auxiliary Input Port**

## OUTPUT BLOCK

The output block includes five identical output channels. Each output channel comprises an output multiplexer, a clock divider module, and a universal output buffer as shown in Figure 24.

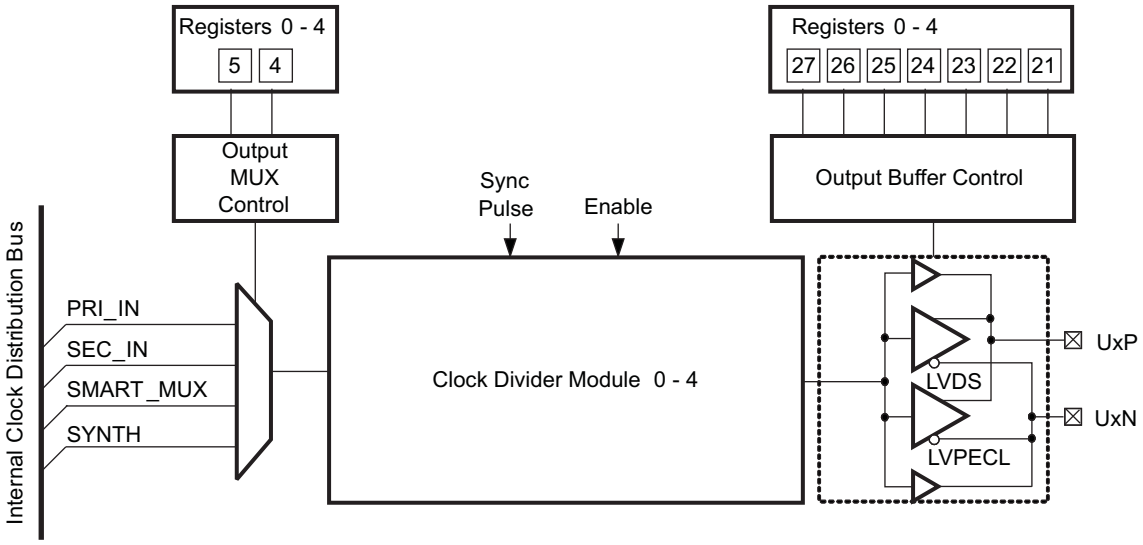



**Figure 24. CDCE18005 Output Channel**

### Output Multiplexer Control

The output multiplexer selects which of the four clock sources available on the Internal Clock Distribution Bus will be presented to the Clock Divider Module. For a description of these clock sources, see Figure 21.

**Table 16. CDCE18005 Output Multiplexer Control Settings**

| OUTPUT MULTIPLEXER CONTROL | | |
|---|---|---|
| Register n (n = 0,1,2,3,4) | | |
| OUTMUXnSELX n.4 | OUTMUXnSELY n.5 | CLOCK SOURCE SELECTED |
| 0 | 0 | PRI_IN |
| 0 | 1 | SEC_IN |
| 1 | 0 | AUX_IN |
| 1 | 1 | Reserved |

### Output Buffer Control

Each of the five output channels includes a programmable output buffer; supporting LVPECL, LVDS, and LVCMOS modes. Table 17 lists the settings required to configure the CDCE18005 for each output type. Registers 0 through 4 correspond to Output Channels 0 through 4 respectively.

**Table 17. CDCE18005 Output Buffer Control Settings**

| OUTPUT BUFFER CONTROL | | | | | | OUTPUT TYPE |
|---|---|---|---|---|---|---|
| Register n (n = 0,1,2,3,4) | | | | | | |
| CMOSMODEnPX | CMOSMODEnPY | CMOSMODEnNX | CMOSMODEnNY | OUTBUFSELnX | OUTBUFSELnY | |
| n.22 | n.23 | n.24 | n.25 | n.26 | n.27 | |
| 0 | 0 | 0 | 0 | 0 | 1 | LVPECL |
| 0 | 1 | 0 | 1 | 1 | 1 | LVDS |
| See LVCMOS Output Buffer Configuration Settings | | | | 0 | 0 | LVCMOS |
| 0 | 1 | 0 | 1 | 1 | 0 | OFF |

### Output Buffer Control – LVCMOS Configurations

A LVCMOS output configuration requires additional configuration data. In the single ended configuration, each Output Channel provides a pair of outputs. The CDCE18005 supports four modes of operation for single ended outputs as listed in Table 18.

**Table 18. LVCMOS Output Buffer Configuration Settings**

| OUTPUT BUFFER CONTROL – LVCMOS CONFIGURATION | | | | | | Output Type | Pin | Output Mode |
|---|---|---|---|---|---|---|---|---|
| Register n (n = 0,1,2,3,4) | | | | | | | | |
| CMOSMODEnPX | CMOSMODEnPY | CMOSMODEnNX | CMOSMODEnNY | OUTBUFSELnX | OUTBUFSELnY | | | |
| n.22 | n.23 | n.24 | n.25 | n.26 | n.27 | | | |
| X | X | 0 | 0 | 0 | 0 | LVCMOS | Negative | Active – Non-inverted |
| X | X | 0 | 1 | 0 | 0 | LVCMOS | Negative | Hi-Z |
| X | X | 1 | 0 | 0 | 0 | LVCMOS | Negative | Active – Non-inverted |
| X | X | 1 | 1 | 0 | 0 | LVCMOS | Negative | Low |
| 0 | 0 | X | X | 0 | 0 | LVCMOS | Positive | Active – Non-inverted |
| 0 | 1 | X | X | 0 | 0 | LVCMOS | Positive | Hi-Z |
| 1 | 0 | X | X | 0 | 0 | LVCMOS | Positive | Active – Non-inverted |
| 1 | 1 | X | X | 0 | 0 | LVCMOS | Positive | Low |

### Output Dividers

Figure 25 shows that each output channel provides a 7-bit divider and digital phase adjust block. Table 19 lists the divide ratios supported by the output divider for each output channel. The output divider's maximum input frequency is limited to 1.175GHz. If the divider is bypassed (divide ratio = 1) then the maximum frequency of the output channel is 1.5GHz.

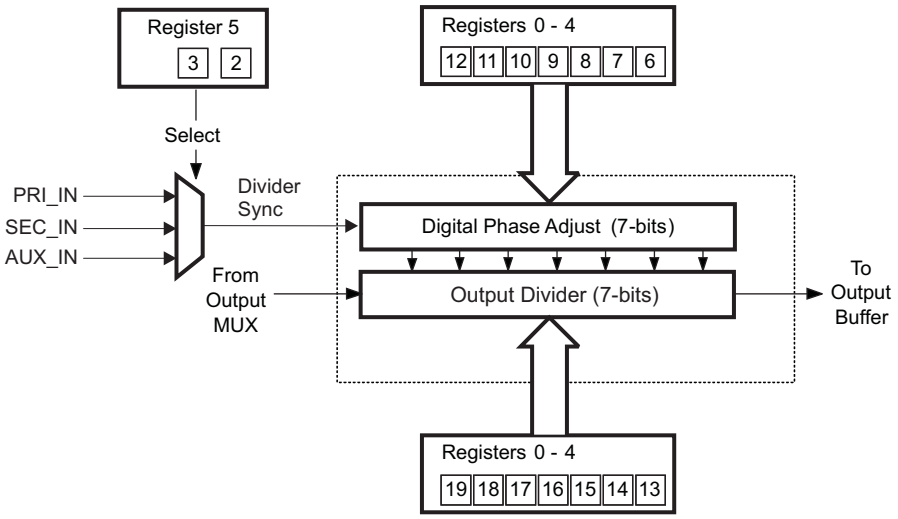



**Figure 25. CDCE18005 Output Divider and Phase Adjust**

## Table19. CDCE18005 Output Divider Settings

| OUTPUT DIVIDER n SETTINGSRegister n (n = 0,1,2,3,4) | | | | | | Output Phase* | | Output Divide Ratio | |
|---|---|---|---|---|---|---|---|---|---|
| Multiplexer | | Integer Divider | | | | | | | |
| OUTnDIVSEL6 | OUTnDIVSEL5 | OUTnDIVSEL4 | OUTnDIVSEL3 | OUTnDIVSEL2 | Integer Divider Setting | | | | |
| n.19 | n.18 | n.17 | n.16 | n.15 | | Cycles | Degree | Output Channels 0-4 | Auxiliary Output |
| X | X | X | X | X | | OFF | OFF | OFF | OFF |
| 0 | 1 | 0 | 0 | 0 | – | 0 | 0 | 1 | 4 |
| 1 | 0 | 0 | 0 | 0 | – | 0.5 | 180 | 2** | 4 |
| 1 | 0 | 0 | 0 | 0 | – | 0 | 0 | 3** | 6 |
| 1 | 0 | 0 | 0 | 0 | – | 0.5 | 180 | 4 | 8 |
| 1 | 0 | 0 | 0 | 0 | – | 0 | 0 | 5 | 10 |
| 0 | 0 | 0 | 0 | 0 | 2 | 21 | 7560 | 6 | 6 |
| 0 | 0 | 0 | 0 | 0 | 2 | 28.5 | 10260 | 8 | 8 |
| 0 | 0 | 0 | 0 | 0 | 2 | 35 | 12500 | 10 | 10 |
| 0 | 0 | 0 | 0 | 1 | 4 | 24 | 8640 | 12 | 12 |
| 0 | 0 | 0 | 0 | 1 | 4 | 32.5 | 11700 | 16 | 16 |
| 0 | 0 | 0 | 0 | 1 | 4 | 40 | 14400 | 20 | 20 |
| 0 | 0 | 0 | 1 | 0 | 6 | 27 | 9720 | 18 | 18 |
| 0 | 0 | 0 | 1 | 0 | 6 | 36.5 | 13140 | 24 | 24 |
| 0 | 0 | 0 | 1 | 0 | 6 | 45 | 16200 | 30 | 30 |
| 0 | 0 | 0 | 1 | 1 | 8 | 40.5 | 14580 | 32 | 32 |
| 0 | 0 | 0 | 1 | 1 | 8 | 50 | 18000 | 40 | 40 |
| 0 | 0 | 1 | 0 | 0 | 10 | 55 | 19800 | 50 | 50 |
| 0 | 0 | 1 | 0 | 1 | 12 | 36 | 12960 | 36 | 36 |
| 0 | 0 | 1 | 0 | 1 | 12 | 48.5 | 17460 | 48 | 48 |
| 0 | 0 | 1 | 0 | 1 | 12 | 60 | 21600 | 60 | 60 |
| 0 | 0 | 1 | 1 | 0 | 14 | 25.5 | 9540 | 28 | 28 |
| 0 | 0 | 1 | 1 | 0 | 14 | 39 | 14040 | 42 | 42 |

| OUTPUT DIVIDER n SETTINGSRegister n (n = 0,1,2,3,4) | | | | | | Output Phase* | | Output Divide Ratio | |
|---|---|---|---|---|---|---|---|---|---|
| Multiplexer | | Integer Divider | | | | | | | |
| OUTnDIVSEL6 | OUTnDIVSEL5 | OUTnDIVSEL4 | OUTnDIVSEL3 | OUTnDIVSEL2 | Integer Divider Setting | | | | |
| n.19 | n.18 | n.17 | n.16 | n.15 | | Cycles | Degree | Output Channels 0-4 | Auxiliary Output |
| 0 | 0 | 1 | 1 | 0 | 14 | 52.5 | 18900 | 56 | 56 |
| 0 | 0 | 1 | 1 | 0 | 14 | 65 | 23400 | 70 | 70 |
| 0 | 0 | 1 | 1 | 1 | 16 | 56.5 | 20340 | 64 | 64 |
| 0 | 0 | 1 | 1 | 1 | 16 | 70 | 25200 | 80 | 80 |

*These columns show that the output divider generates a unique phase lag in the output clock (relative to the clock from the output multiplexer) determined by the divide ratio used.

**Output channel 2 or 3 determine the auxiliary output divide ratio. For example, if the auxiliary output is programmed to drive via output 2 and output 2 divider is programmed to divide by 3, then the divide ratio for the auxiliary output will be 6.

### Digital Phase Adjust

Figure 26 provides an overview of the Digital Phase Adjust feature. The output divider includes a coarse phase adjust that shifts the divided clock signal that drives the output buffer. Essentially, the Digital Phase Adjust timer delays when the output divider starts dividing; thereby shifting the phase of the output clock. The phase adjust resolution is a function of the divide function. Coarse phase adjust parameters include:

- Number of Phase Delay Steps – the number of phase delay steps available is equal to the divide ratio selected. For example, if a Divide by 4 is selected, then the Digital Phase Adjust can be programmed to select when the output divider changes state based upon selecting one of the four counts on the input. Figure 26 shows an example of divide by 16 in which there are 16 rising edges of Clock IN at which the output divider changes state (this particular example shows the fourth edge shifting the output by one fourth of the period of the output).
- Phase Delay Step Size – the step size is determined by the number of phase delay steps according to the following equations:

$$\text{Stepsize(deg)} = \frac{360 \text{ degrees}}{\text{OutputDivideRatio}} \quad (1)$$

$$\text{Stepsize(sec)} = \frac{\frac{1}{f_{\text{ClockIN}}}}{\text{OutputDivideRatio}} \quad (2)$$

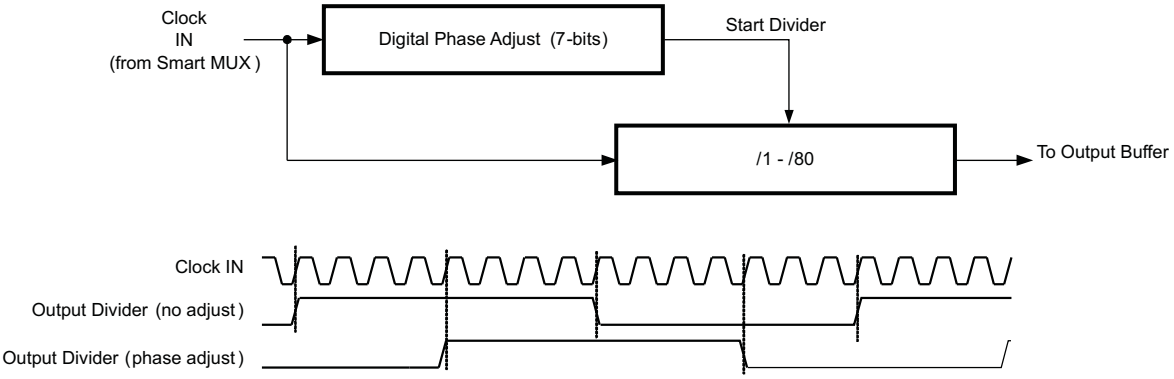



**Figure 26. CDCE18005 Phase Adjust**

### Phase Adjust example

**Given:**

Output Frequency: 30.72 MHz

Input Frequency: 491.52 MHz

Output Divider Setting: 16

$$\text{Stepsize(deg)} = \frac{360}{32} = 11.25^\circ / \text{Step} \quad (3)$$

The tables that follow provide a list of valid register settings for the digital phase adjust blocks.

## Table 20. CDCE18005 Output Coarse Phase Adjust Settings (1)

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/2) |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/3) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/3) |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/4) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/4) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/4) |
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/5) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/5) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/5) |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4(2π/5) |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/6) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/6) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 3(2π/6) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 4(2π/6) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 5(2π/6) |
| 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/8) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/8) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/8) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 4(2π/8) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 5(2π/8) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 6(2π/8) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 7(2π/8) |
| 10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/10) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/10) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/10) |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4(2π/10) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 5(2π/10) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 6(2π/10) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 7(2π/10) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 8(2π/10) |
| | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 9(2π/10) |
| 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/12) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/12) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 3(2π/12) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 4(2π/12) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 5(2π/12) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 6(2π/12) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 7(2π/12) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 8(2π/12) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 9(2π/12) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 10(2π/12) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 11(2π/12) |
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/16) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/16) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/16) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 4(2π/16) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 5(2π/16) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 6(2π/16) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 7(2π/16) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8(2π/16) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 9(2π/16) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 10(2π/16) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 11(2π/16) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 12(2π/16) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 13(2π/16) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 14(2π/16) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 15(2π/16) |

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/18) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/18) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 3(2π/18) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 4(2π/18) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 5(2π/18) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 6(2π/18) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 7(2π/18) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 8(2π/18) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 9(2π/18) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 10(2π/18) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 11(2π/18) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 12(2π/18) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 13(2π/18) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 14(2π/18) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 15(2π/18) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 16(2π/18) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 17(2π/18) |
| 20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/20) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/20) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/20) |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4(2π/20) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 5(2π/20) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 6(2π/20) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 7(2π/20) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8(2π/20) |
| | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 9(2π/20) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10(2π/20) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11(2π/20) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12(2π/20) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13(2π/20) |
| | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14(2π/20) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 15(2π/20) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 16(2π/20) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 17(2π/20) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 18(2π/20) |
| | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 19(2π/20) |
| 24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/24) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/24) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/24) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 4(2π/24) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 5(2π/24) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 6(2π/24) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 7(2π/24) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8(2π/24) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 9(2π/24) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 10(2π/24) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 11(2π/24) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 12(2π/24) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 13(2π/24) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 14(2π/24) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 15(2π/24) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 16(2π/24) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 17(2π/24) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 18(2π/24) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 19(2π/24) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 20(2π/24) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 21(2π/24) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 22(2π/24) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 23(2π/24) |

## Table 21. CDCE18005 Output Coarse Phase Adjust Settings (2)

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/28) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 2(2π/28) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 3(2π/28) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 4(2π/28) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 5(2π/28) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 6(2π/28) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 7(2π/28) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 8(2π/28) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 9(2π/28) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 10(2π/28) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 11(2π/28) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 12(2π/28) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 13(2π/28) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 14(2π/28) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 15(2π/28) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 16(2π/28) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 17(2π/28) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 18(2π/28) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 19(2π/28) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 20(2π/28) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 21(2π/28) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 22(2π/28) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 23(2π/28) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 24(2π/28) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 25(2π/28) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 26(2π/28) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 27(2π/28) |
| 30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/30) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/30) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/30) |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4(2π/30) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 5(2π/30) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 6(2π/30) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 7(2π/30) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8(2π/30) |
| | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 9(2π/30) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10(2π/30) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11(2π/30) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12(2π/30) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13(2π/30) |
| | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14(2π/30) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 15(2π/30) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 16(2π/30) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 17(2π/30) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 18(2π/30) |
| | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 19(2π/30) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20(2π/30) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21(2π/30) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22(2π/30) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23(2π/30) |
| | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24(2π/30) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 25(2π/30) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 26(2π/30) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 27(2π/30) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 28(2π/30) |
| | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 29(2π/30) |

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 32 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/32) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/32) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/32) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 4(2π/32) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 5(2π/32) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 6(2π/32) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 7(2π/32) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8(2π/32) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 9(2π/32) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 10(2π/32) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 11(2π/32) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 12(2π/32) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 13(2π/32) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 14(2π/32) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 15(2π/32) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 16(2π/32) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 17(2π/32) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 18(2π/32) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 19(2π/32) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 20(2π/32) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 21(2π/32) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 22(2π/32) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 23(2π/32) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 24(2π/32) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 25(2π/32) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 26(2π/32) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 27(2π/32) |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 28(2π/32) |
| | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 29(2π/32) |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 30(2π/32) |
| | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 31(2π/32) |
| 36 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/36) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/36) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 3(2π/36) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 4(2π/36) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 5(2π/36) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 6(2π/36) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 7(2π/36) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 8(2π/36) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 9(2π/36) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 10(2π/36) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 11(2π/36) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 12(2π/36) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 13(2π/36) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 14(2π/36) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 15(2π/36) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 16(2π/36) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 17(2π/36) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 18(2π/36) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 19(2π/36) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 20(2π/36) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 21(2π/36) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 22(2π/36) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 23(2π/36) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 24(2π/36) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 25(2π/36) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 26(2π/36) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 27(2π/36) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 28(2π/36) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 29(2π/36) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 30(2π/36) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 31(2π/36) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 32(2π/36) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 33(2π/36) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 34(2π/36) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 35(2π/36) |

## Table 22. CDCE18005 Output Coarse Phase Adjust Settings (3)

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 40 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/40) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/40) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/40) |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4(2π/40) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 5(2π/40) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 6(2π/40) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 7(2π/40) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8(2π/40) |
| | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 9(2π/40) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10(2π/40) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11(2π/40) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12(2π/40) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13(2π/40) |
| | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14(2π/40) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 15(2π/40) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 16(2π/40) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 17(2π/40) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 18(2π/40) |
| | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 19(2π/40) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20(2π/40) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21(2π/40) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22(2π/40) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23(2π/40) |
| | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24(2π/40) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 25(2π/40) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 26(2π/40) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 27(2π/40) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 28(2π/40) |
| | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 29(2π/40) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30(2π/40) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31(2π/40) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32(2π/40) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33(2π/40) |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34(2π/40) |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 35(2π/40) |
| | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 36(2π/40) |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 37(2π/40) |
| | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 38(2π/40) |
| | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 39(2π/40) |
| 42 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/42) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/42) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 3(2π/42) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 4(2π/42) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 5(2π/42) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 6(2π/42) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 7(2π/42) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 8(2π/42) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 9(2π/42) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 10(2π/42) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 11(2π/42) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 12(2π/42) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 13(2π/42) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 14(2π/42) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 15(2π/42) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 16(2π/42) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 17(2π/42) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 18(2π/42) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 19(2π/42) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 20(2π/42) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 21(2π/42) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 22(2π/42) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 23(2π/42) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 24(2π/42) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 25(2π/42) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 26(2π/42) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 27(2π/42) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 28(2π/42) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 29(2π/42) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 30(2π/42) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 31(2π/42) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 32(2π/42) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 33(2π/42) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 34(2π/42) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 35(2π/42) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 36(2π/42) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 37(2π/42) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 38(2π/42) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 39(2π/42) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 40(2π/42) |
| | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 41(2π/42) |

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 48 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/48) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/48) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/48) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 4(2π/48) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 5(2π/48) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 6(2π/48) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 7(2π/48) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8(2π/48) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 9(2π/48) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 10(2π/48) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 11(2π/48) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 12(2π/48) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 13(2π/48) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 14(2π/48) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 15(2π/48) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 16(2π/48) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 17(2π/48) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 18(2π/48) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 19(2π/48) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 20(2π/48) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 21(2π/48) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 22(2π/48) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 23(2π/48) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 24(2π/48) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 25(2π/48) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 26(2π/48) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 27(2π/48) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 28(2π/48) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 29(2π/48) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 30(2π/48) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 31(2π/48) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 32(2π/48) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 33(2π/48) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 34(2π/48) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 35(2π/48) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 36(2π/48) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 37(2π/48) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 38(2π/48) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 39(2π/48) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 40(2π/48) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 41(2π/48) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 42(2π/48) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 43(2π/48) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 44(2π/48) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 45(2π/48) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 46(2π/48) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 47(2π/48) |

## Table 23. CDCE18005 Output Coarse Phase Adjust Settings (4)

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 50 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/50) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/50) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/50) |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4(2π/50) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 5(2π/50) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 6(2π/50) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 7(2π/50) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8(2π/50) |
| | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 9(2π/50) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10(2π/50) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11(2π/50) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12(2π/50) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13(2π/50) |
| | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14(2π/50) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 15(2π/50) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 16(2π/50) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 17(2π/50) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 18(2π/50) |
| | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 19(2π/50) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20(2π/50) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21(2π/50) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22(2π/50) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23(2π/50) |
| | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24(2π/50) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 25(2π/50) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 26(2π/50) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 27(2π/50) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 28(2π/50) |
| | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 29(2π/50) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 30(2π/50) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 31(2π/50) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 32(2π/50) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 33(2π/50) |
| | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 34(2π/50) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 35(2π/50) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 36(2π/50) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 37(2π/50) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 38(2π/50) |
| | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 39(2π/50) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 40(2π/50) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 41(2π/50) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 42(2π/50) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 43(2π/50) |
| | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 44(2π/50) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 45(2π/50) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 46(2π/50) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 47(2π/50) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 48(2π/50) |
| | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 49(2π/50) |

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 56 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/56) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/56) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/56) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 4(2π/56) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 5(2π/56) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 6(2π/56) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 7(2π/56) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8(2π/56) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 9(2π/56) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 10(2π/56) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 11(2π/56) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 12(2π/56) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 13(2π/56) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 14(2π/56) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 15(2π/56) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 16(2π/56) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 17(2π/56) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 18(2π/56) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 19(2π/56) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 20(2π/56) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 21(2π/56) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 22(2π/56) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 23(2π/56) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 24(2π/56) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 25(2π/56) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 26(2π/56) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 27(2π/56) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 28(2π/56) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 29(2π/56) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 30(2π/56) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 31(2π/56) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 32(2π/56) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 33(2π/56) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 34(2π/56) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 35(2π/56) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 36(2π/56) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 37(2π/56) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 38(2π/56) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 39(2π/56) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 40(2π/56) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 41(2π/56) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 42(2π/56) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 43(2π/56) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 44(2π/56) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 45(2π/56) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 46(2π/56) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 47(2π/56) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 48(2π/56) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 49(2π/56) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 50(2π/56) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 51(2π/56) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 52(2π/56) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 53(2π/56) |
| | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 54(2π/56) |
| | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 55(2π/56) |

## Table 24. CDCE18005 Output Coarse Phase Adjust Settings (5)

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 60 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/60) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/60) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/60) |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4(2π/60) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 5(2π/60) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 6(2π/60) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 7(2π/60) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8(2π/60) |
| | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 9(2π/60) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10(2π/60) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11(2π/60) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12(2π/60) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13(2π/60) |
| | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14(2π/60) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 15(2π/60) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 16(2π/60) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 17(2π/60) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 18(2π/60) |
| | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 19(2π/60) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20(2π/60) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21(2π/60) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22(2π/60) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23(2π/60) |
| | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24(2π/60) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 25(2π/60) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 26(2π/60) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 27(2π/60) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 28(2π/60) |
| | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 29(2π/60) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 30(2π/60) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 31(2π/60) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 32(2π/60) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 33(2π/60) |
| | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 34(2π/60) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 35(2π/60) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 36(2π/60) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 37(2π/60) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 38(2π/60) |
| | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 39(2π/60) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 40(2π/60) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 41(2π/60) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 42(2π/60) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 43(2π/60) |
| | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 44(2π/60) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 45(2π/60) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 46(2π/60) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 47(2π/60) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 48(2π/60) |
| | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 49(2π/60) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 50(2π/60) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 51(2π/60) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 52(2π/60) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 53(2π/60) |
| | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 54(2π/60) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 55(2π/60) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 56(2π/60) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 57(2π/60) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 58(2π/60) |
| | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 59(2π/60) |

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 64 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/64) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/64) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/64) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 4(2π/64) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 5(2π/64) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 6(2π/64) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 7(2π/64) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8(2π/64) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 9(2π/64) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 10(2π/64) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 11(2π/64) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 12(2π/64) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 13(2π/64) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 14(2π/64) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 15(2π/64) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 16(2π/64) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 17(2π/64) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 18(2π/64) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 19(2π/64) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 20(2π/64) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 21(2π/64) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 22(2π/64) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 23(2π/64) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 24(2π/64) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 25(2π/64) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 26(2π/64) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 27(2π/64) |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 28(2π/64) |
| | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 29(2π/64) |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 30(2π/64) |
| | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 31(2π/64) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 32(2π/64) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 33(2π/64) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 34(2π/64) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 35(2π/64) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 36(2π/64) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 37(2π/64) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 38(2π/64) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 39(2π/64) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 40(2π/64) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 41(2π/64) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 42(2π/64) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 43(2π/64) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 44(2π/64) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 45(2π/64) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 46(2π/64) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 47(2π/64) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 48(2π/64) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 49(2π/64) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 50(2π/64) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 51(2π/64) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 52(2π/64) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 53(2π/64) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 54(2π/64) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 55(2π/64) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 56(2π/64) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 57(2π/64) |
| | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 58(2π/64) |
| | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 59(2π/64) |
| | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 60(2π/64) |
| | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 61(2π/64) |
| | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 62(2π/64) |
| | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 63(2π/64) |

## Table 25. CDCE18005 Output Coarse Phase Adjust Settings (6)

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 70 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/70) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/70) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/70) |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4(2π/70) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 5(2π/70) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 6(2π/70) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 7(2π/70) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8(2π/70) |
| | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 9(2π/70) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10(2π/70) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11(2π/70) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12(2π/70) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13(2π/70) |
| | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14(2π/70) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 15(2π/70) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 16(2π/70) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 17(2π/70) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 18(2π/70) |
| | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 19(2π/70) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20(2π/70) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21(2π/70) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22(2π/70) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23(2π/70) |
| | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24(2π/70) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 25(2π/70) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 26(2π/70) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 27(2π/70) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 28(2π/70) |
| | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 29(2π/70) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30(2π/70) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31(2π/70) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32(2π/70) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33(2π/70) |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34(2π/70) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 35(2π/70) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 36(2π/70) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 37(2π/70) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 38(2π/70) |
| | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 39(2π/70) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 40(2π/70) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 41(2π/70) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 42(2π/70) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 43(2π/70) |
| | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 44(2π/70) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 45(2π/70) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 46(2π/70) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 47(2π/70) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 48(2π/70) |
| | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 49(2π/70) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 50(2π/70) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 51(2π/70) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 52(2π/70) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 53(2π/70) |
| | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 54(2π/70) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 55(2π/70) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 56(2π/70) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 57(2π/70) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 58(2π/70) |
| | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 59(2π/70) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 60(2π/70) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 61(2π/70) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 62(2π/70) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 63(2π/70) |
| | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 64(2π/70) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 65(2π/70) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 66(2π/70) |
| | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 67(2π/70) |
| | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 68(2π/70) |
| | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 69(2π/70) |

| Divide Ratio | PHnADGC6 | PHnADGC5 | PHnADGC4 | PHnADGC3 | PHnADGC2 | PHnADGC1 | PHnADGC0 | Phase Delay |
|---|---|---|---|---|---|---|---|---|
| | n.12 | n.11 | n.10 | n.9 | n.8 | n.7 | n.6 | (radian) |
| 80 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (2π/80) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2(2π/80) |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3(2π/80) |
| | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4(2π/80) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 5(2π/80) |
| | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 6(2π/80) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 7(2π/80) |
| | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8(2π/80) |
| | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 9(2π/80) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10(2π/80) |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11(2π/80) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12(2π/80) |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13(2π/80) |
| | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14(2π/80) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 15(2π/80) |
| | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 16(2π/80) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 17(2π/80) |
| | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 18(2π/80) |
| | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 19(2π/80) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20(2π/80) |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21(2π/80) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22(2π/80) |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23(2π/80) |
| | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24(2π/80) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 25(2π/80) |
| | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 26(2π/80) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 27(2π/80) |
| | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 28(2π/80) |
| | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 29(2π/80) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30(2π/80) |
| | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31(2π/80) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32(2π/80) |
| | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33(2π/80) |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34(2π/80) |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 35(2π/80) |
| | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 36(2π/80) |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 37(2π/80) |
| | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 38(2π/80) |
| | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 39(2π/80) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40(2π/80) |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41(2π/80) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42(2π/80) |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 43(2π/80) |
| | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44(2π/80) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 45(2π/80) |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 46(2π/80) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 47(2π/80) |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 48(2π/80) |
| | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 49(2π/80) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50(2π/80) |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51(2π/80) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52(2π/80) |
| | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53(2π/80) |
| | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54(2π/80) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 55(2π/80) |
| | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 56(2π/80) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 57(2π/80) |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 58(2π/80) |
| | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 59(2π/80) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 60(2π/80) |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 61(2π/80) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 62(2π/80) |
| | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 63(2π/80) |
| | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 64(2π/80) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 65(2π/80) |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 66(2π/80) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 67(2π/80) |
| | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 68(2π/80) |
| | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 69(2π/80) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70(2π/80) |
| | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71(2π/80) |
| | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 72(2π/80) |
| | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 73(2π/80) |
| | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 74(2π/80) |
| | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 75(2π/80) |
| | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 76(2π/80) |
| | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 77(2π/80) |
| | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 78(2π/80) |
| | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 79(2π/80) |

### Auxiliary Output

Figure 27 shows the auxiliary output port. Table 26 lists how the auxiliary output port is controlled. The output buffer supports a maximum output frequency of 250 MHz and drives at LVCMOS levels. Refer to Table 19 for the list of divider settings that establishes the output frequency.

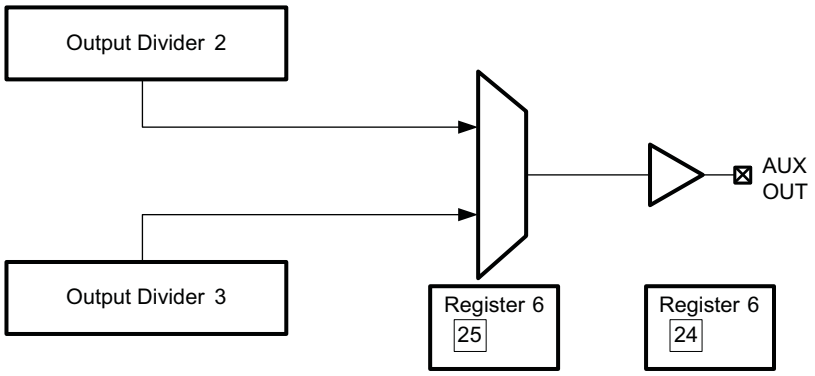



**Figure 27. CDCE18005 Auxiliary Output**

**Table 26. CDCE18005 Auxiliary Output Settings**

| Bit Name → | AUXFEEDSEL | AUXOUTEN | AUX OUTPUT SOURCE |
|---|---|---|---|
| Register.Bit → | 6.25 | 6.24 | |
| | X | 0 | OFF |
| | 0 | 1 | Divider 2 |
| | 1 | 1 | Divider 3 |

## DEVICE POWER CALCULATION AND THERMAL MANAGEMENT

The CDCE18005 is a high performance device, therefore careful attention must be paid to device configuration and printed circuit board layout with respect to power consumption. Table 27 provides the power consumption for the individual blocks within the CDCE18005. To estimate total power consumption, calculate the sum of the products of the number of blocks used and the power dissipated of each corresponding block.

Provide Sample Calculation Here after numbers become available.

**Table 27. CDCE18005 Power Consumption**

| Internal Block (Power at 3.3V) | Power Dissipated per Block (Typical) | Number of Blocks per Device |
|---|---|---|
| Input Circuit | 18 mW | 1 |
| Output Divider | 185 mW | 5 |
| Output Buffer ( LVPECL) | 116 mW | 5 |
| Output Buffer (LVDS) | 76 mW | 5 |
| Output Buffer (LVCMOS) | 86 mW | 10 |

This power estimate determines the degree of thermal management required for a specific design. Employing the thermally enhanced printed circuit board layout shown in Figure 29 insures that the thermal performance curves shown in Figure 28 apply. Observing good thermal layout practices enables the thermal pad on the backside of the QFN-48 package to provide a good thermal path between the die contained within the package and the ambient air. This thermal pad also serves as the ground connection the device; therefore, a low inductance connection to the ground plane is essential.

Figure 29 shows a layout optimized for good thermal performance and a good power supply connection as well. The 7×7 filled via patter facilitates both considerations. Finally, the recommended layout achieves $\theta_{JA}$ = 27.3°C/W in still air and 20.3°C/W in an environment with 100 LFM airflow if implemented on a JEDEC compliant thermal test board.

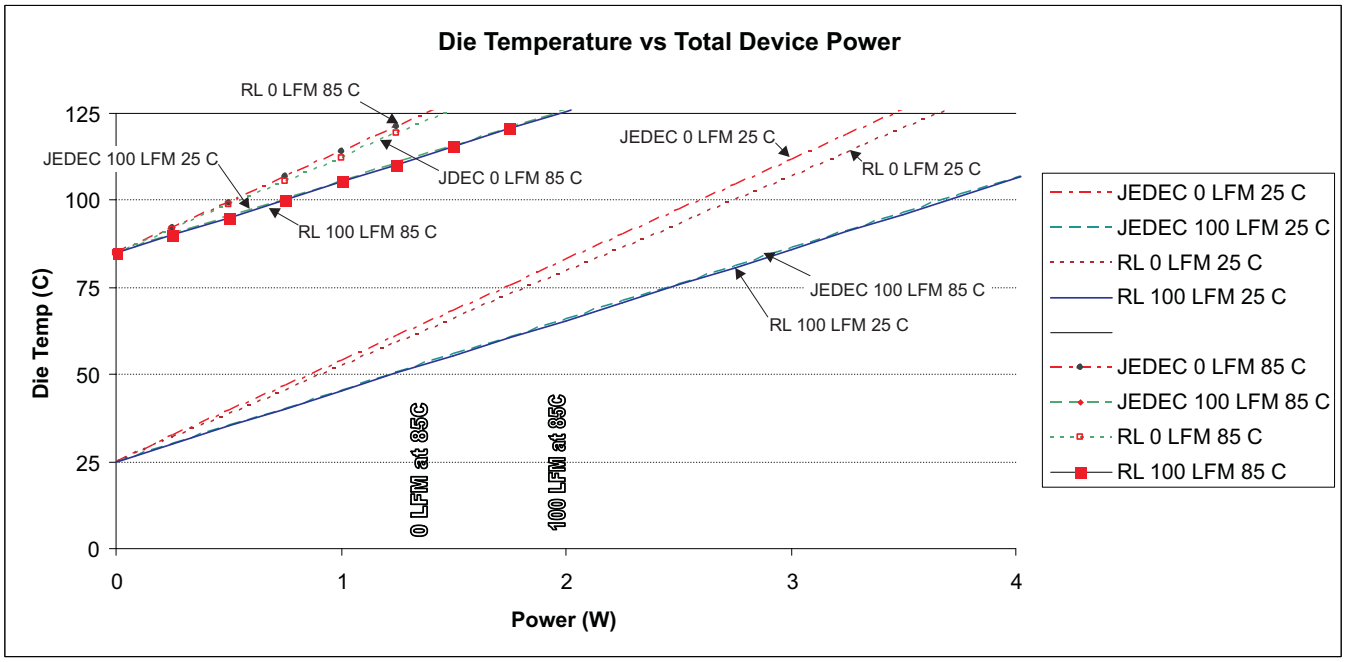



**Figure 28. CDCE18005 Die Temperature vs Device Power**

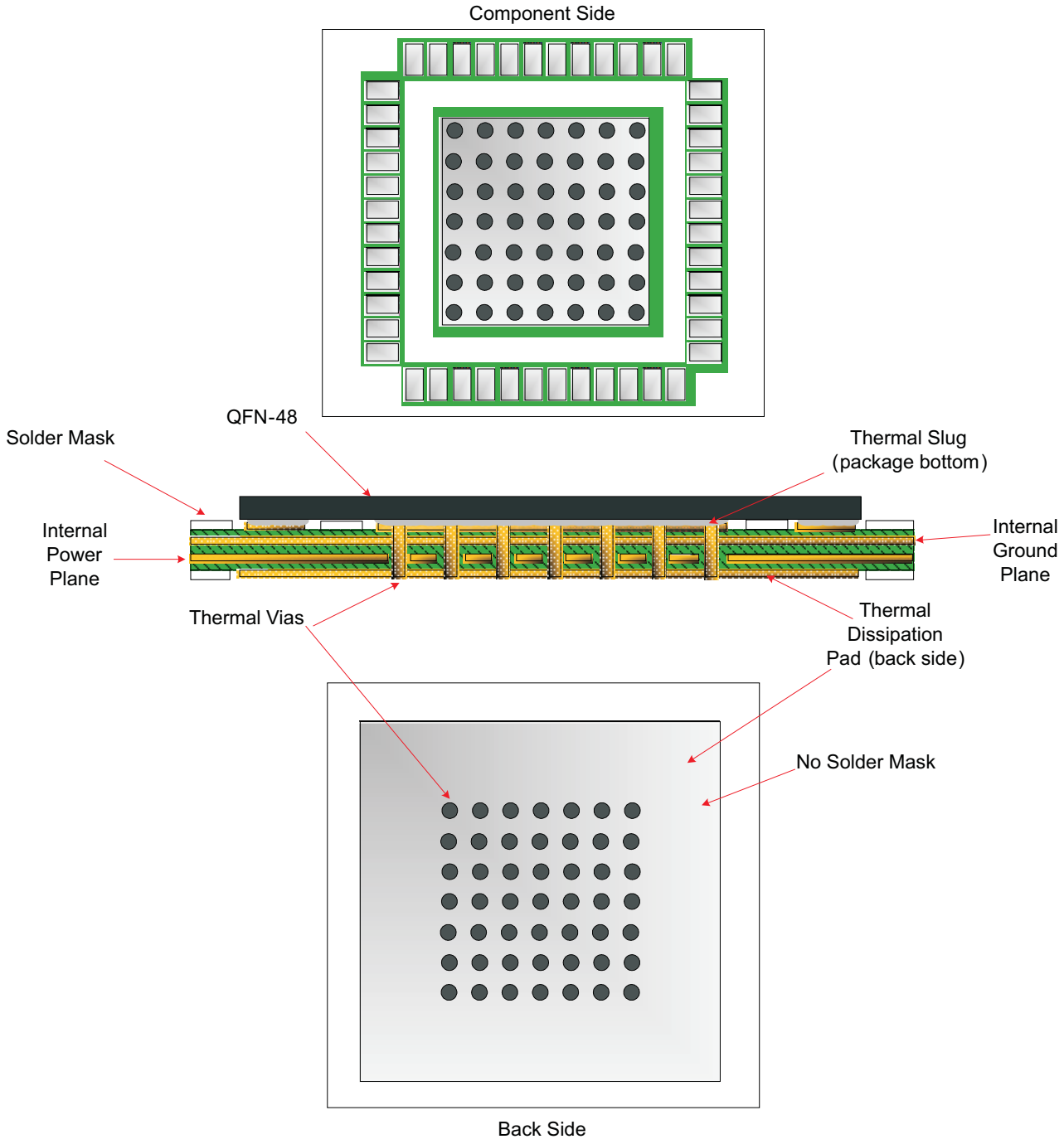



**Figure 29. CDCE18005 Recommended PCB Layout**

### CDCE18005 Power Supply Bypassing – Recommended Layout

Figure 30 shows two conceptual layouts detailing recommended placement of power supply bypass capacitors. If the capacitors are mounted on the back side, 0402 components can be employed; however, soldering to the Thermal Dissipation Pad can be difficult. For component side mounting, use 0201 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible.

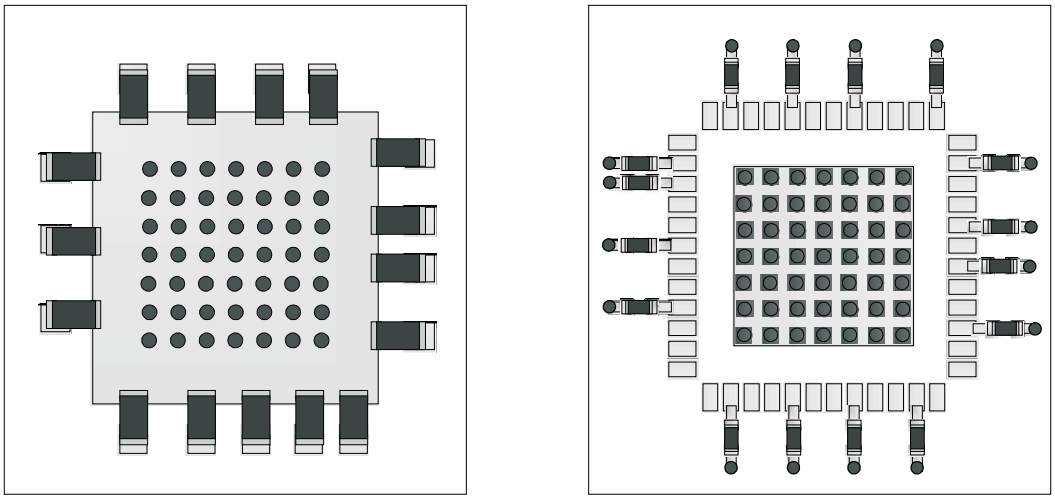



**Figure 30. CDCE18005 Power Supply Bypassing**

## APPLICATION INFORMATION AND GENERAL USAGE HINTS

### Fan-out Buffer

Each output of the CDCE18005 can be configured as a fan-out buffer (divider bypassed) or fan-out buffer with divide and skew control functionality.

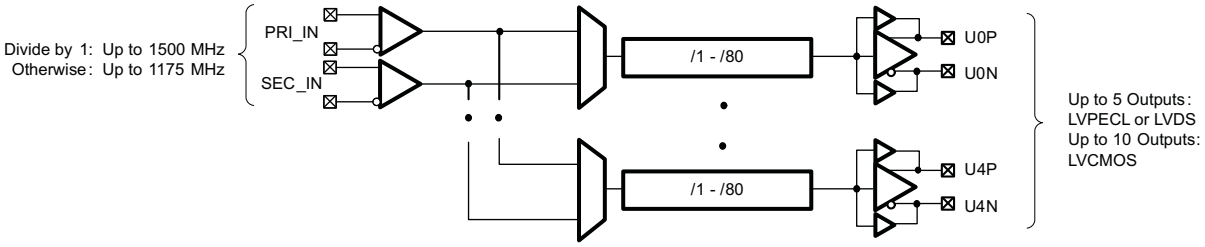



**Figure 31. CDCE18005 Fan-out Buffer Mode**

### Clock Generator

The CDCE18005 can generate 5–10 low noise clocks from a single crystal or crystal oscillator as follows:

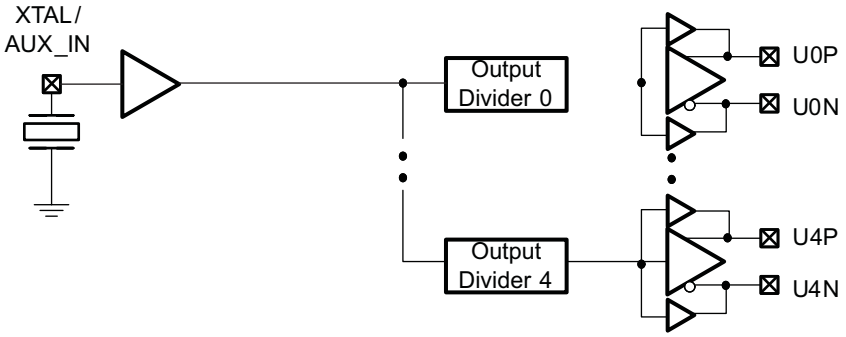



**Figure 32. CDCE18005 Clock Generator Mode**

### Clock Distribution – Mixed Mode

The following table presents a common scenario where the CDCE18005 can function as a clock switch that accepts LVDS and crystal inputs and drives LVDS, LVPECL and LVCMOS outputs.

| CLOCK FREQUENCY | INPUT/OUTPUT | FORMAT | NUMBER | CDCE18005 PORT | COMMENT |
|---|---|---|---|---|---|
| 491.52 MHz | Input | LVDS | 1 | SEC_IN | Reference |
| 125 MHz | Input | LVDS | 1 | PRI_IN | Reference from backplane |
| 10 MHz | Input | AT-Cut | 1 | AUX_IN | Low end crystal oscillator |
| 122.88 MHz | Output | LVDS | 1 | U0 | SerDes Clock |
| 491.52 MHz | Output | LVPECL | 1 | U1 | ASIC |
| 125 MHz | Output | LVPECL | 1 | U2 | FPGA |
| 30.72 MHz | Outputs | LVCMOS | 2 | U3 | ASIC |
| 10 MHz | Outputs | LVCMOS | 2 | U4 | CPU, DSP |

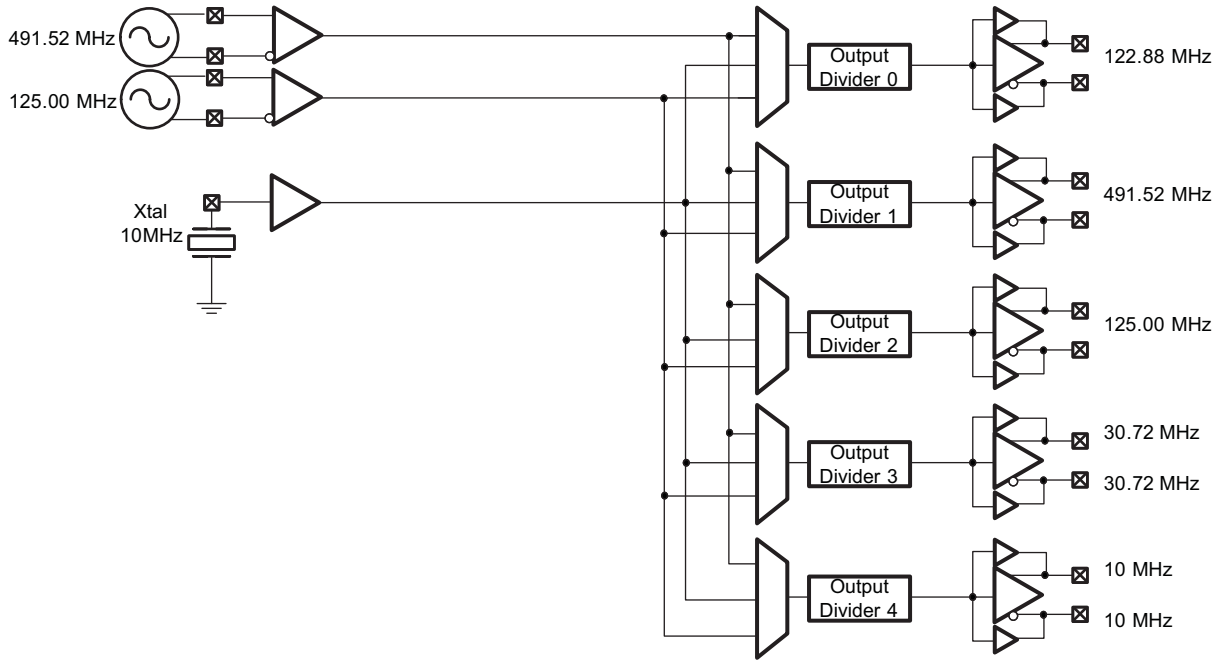



**Figure 33. CDCE18005 Mixed Mode Clock Distribution Example**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| CDCE18005RGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| CDCE18005RGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

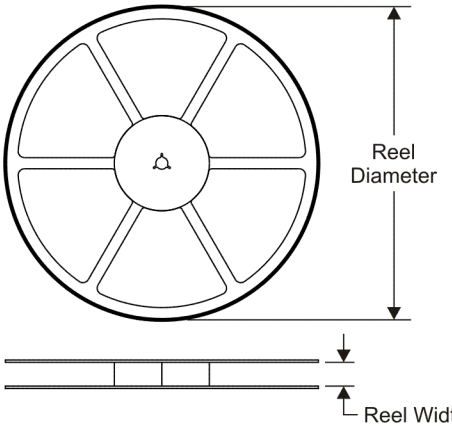
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

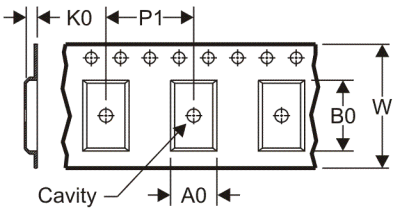
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

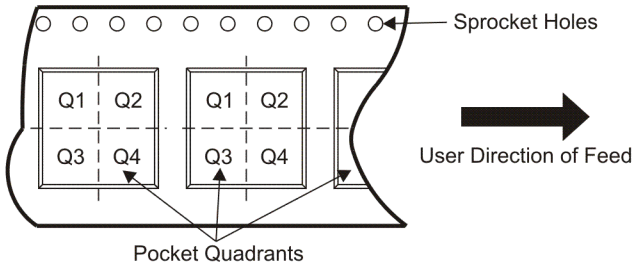



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

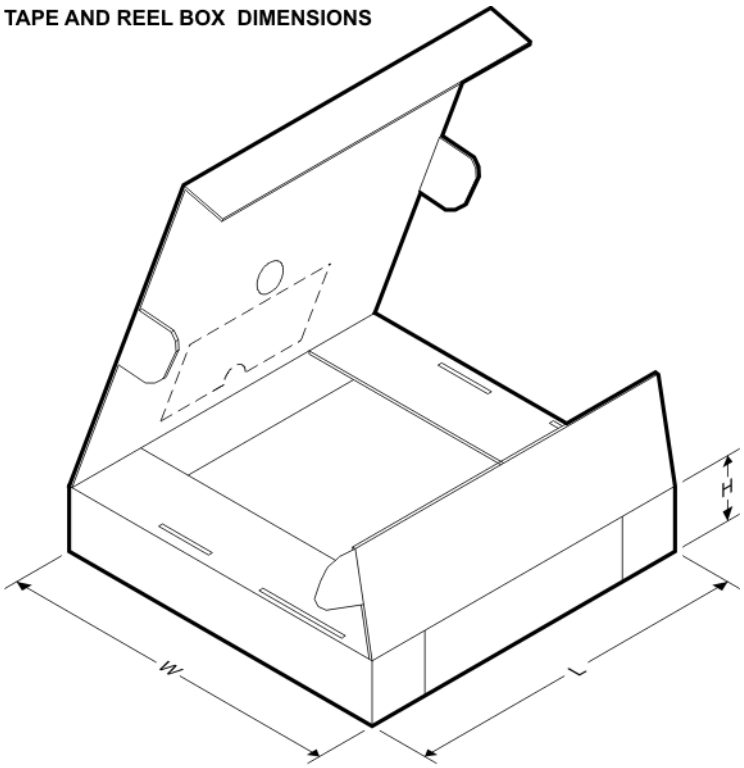
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CDCE18005RGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q2 |
| CDCE18005RGZT | VQFN | RGZ | 48 | 250 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q2 |

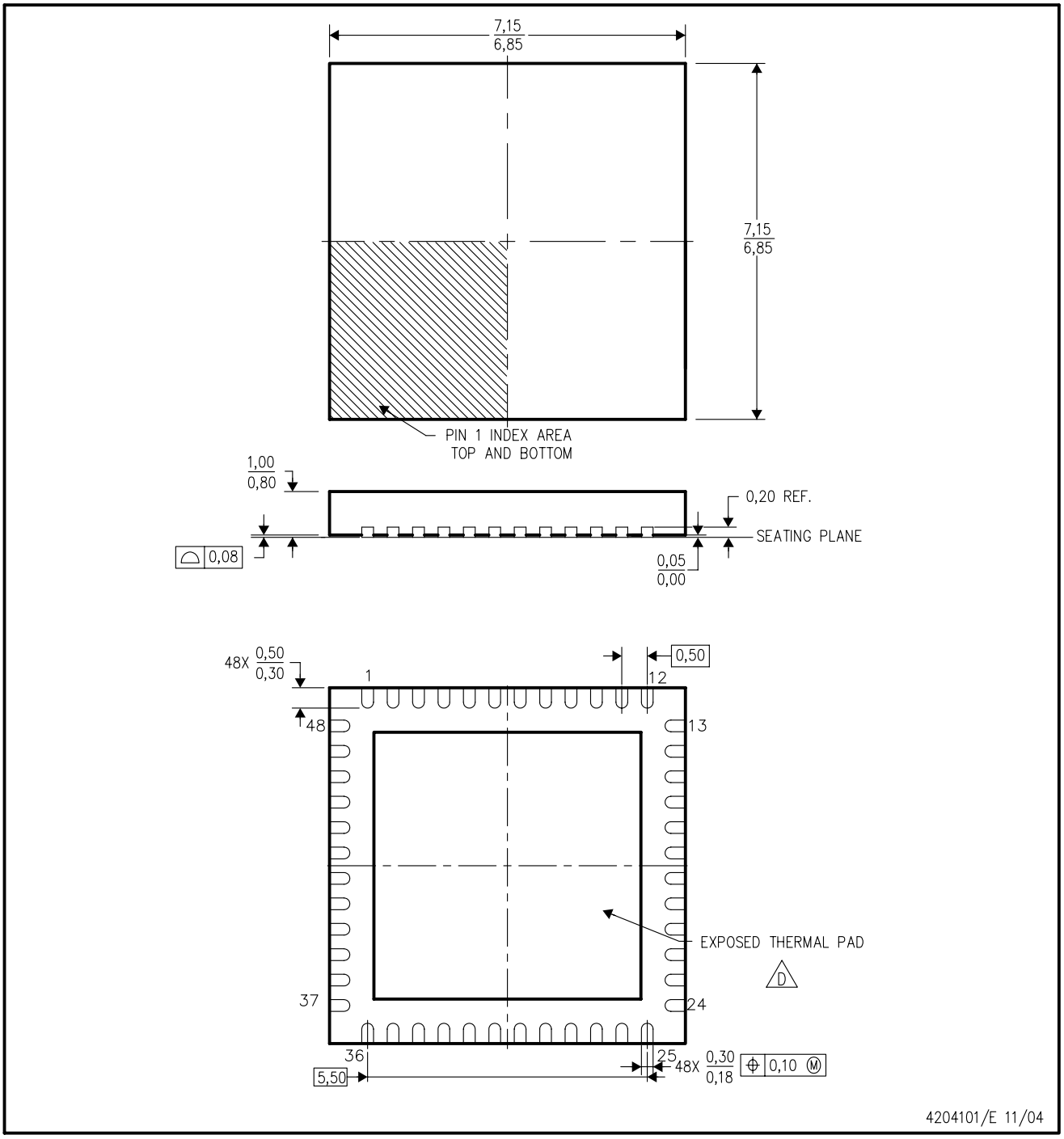
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CDCE18005RGZR | VQFN | RGZ | 48 | 2500 | 333.2 | 345.9 | 28.6 |
| CDCE18005RGZT | VQFN | RGZ | 48 | 250 | 333.2 | 345.9 | 28.6 |

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

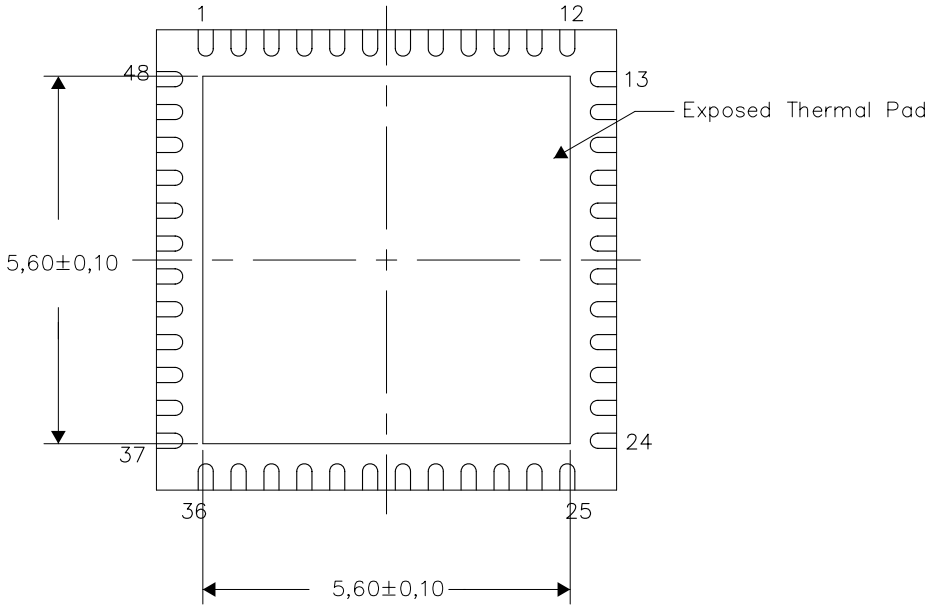
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

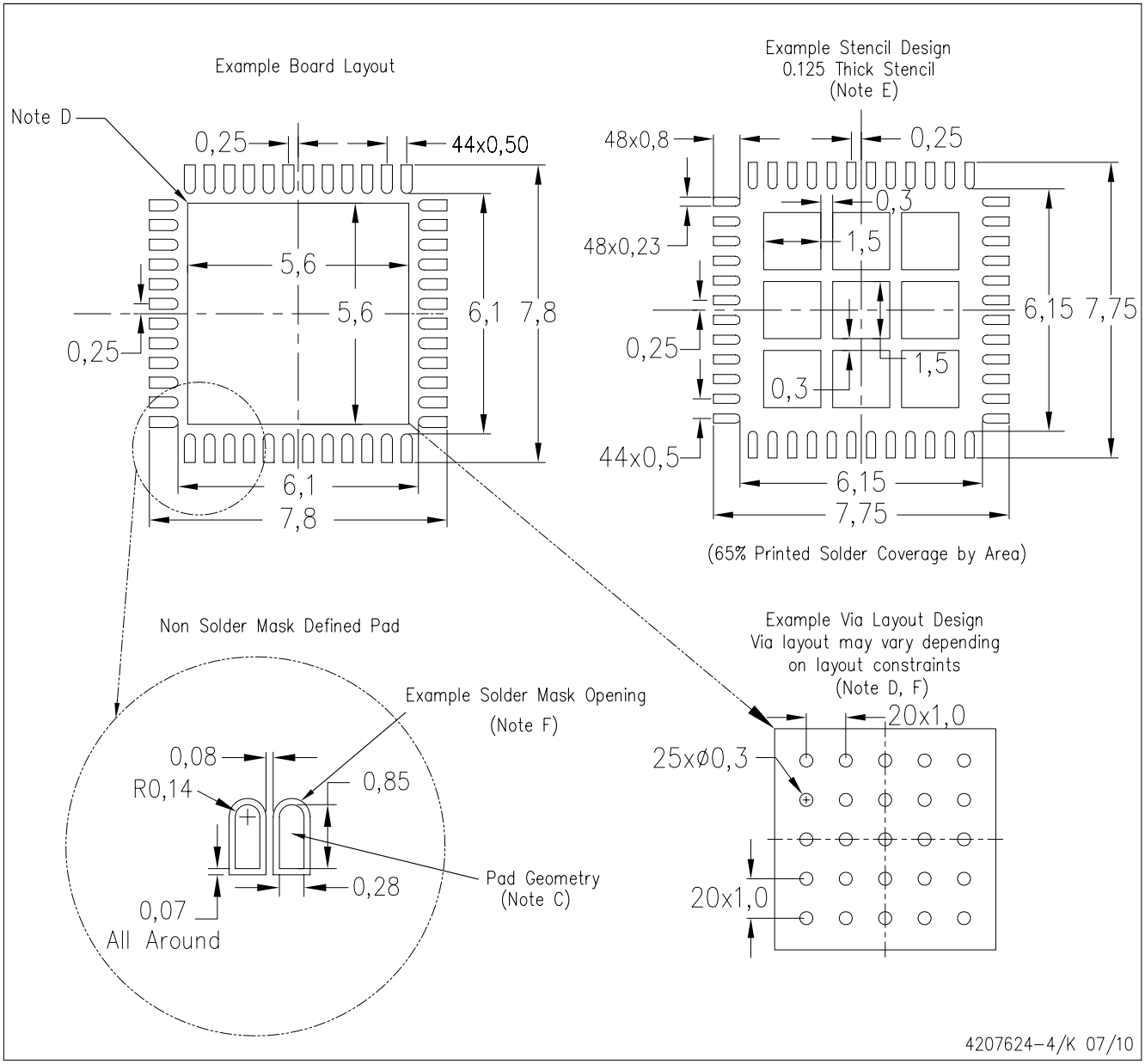



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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