TDK SEMICONDUCTOR CORP.

73M2910L Microcontroller

April 2000

DESCRIPTION

The 73M2910L high performance micro-controller is based on the industry standard 8-bit 8032 implemented in an advanced submicron CMOS process. The processor has the attributes of the 8032, including instruction cycle time, UART, timers, interrupts, 256 bytes of on-chip RAM and programmable I/O. The architecture has been optimized for low power portable modem or communication applications by integrating unique features with the core CPU.

A key feature is a user friendly HDLC Packetizer, accessed through the special function registers. It has a serial I/O, hardware support for 16 and 32-bit CRC, zero insert/delete control, a dedicated interrupt and a clear channel mode for by-passing the packetizer.

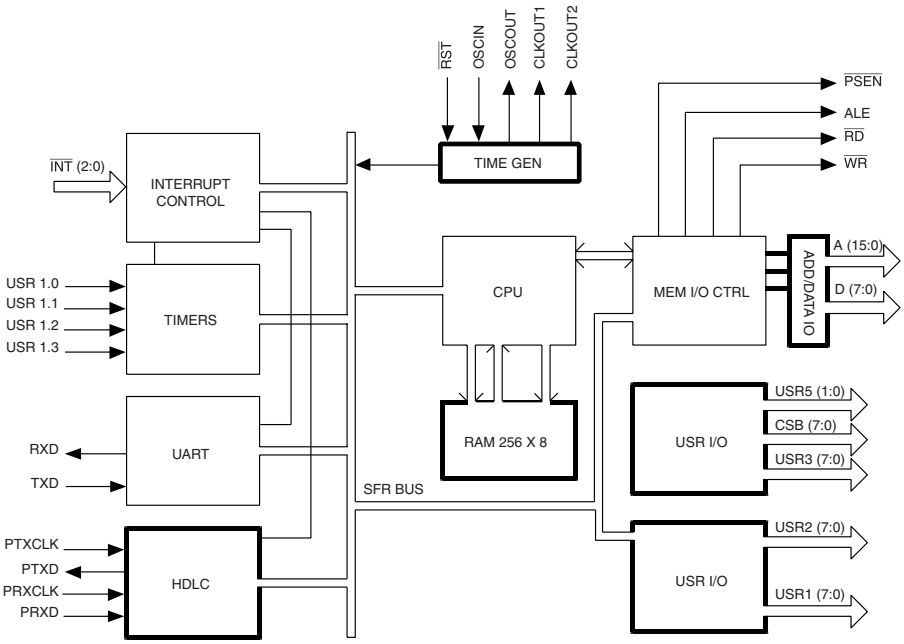
Other features include additional user programmable I/O with programmable bank select and chip select logic, designed to eliminate board level glue logic. It also includes two general-purpose input ports with programmable wakeup capability.

For devices that require non-multiplexed address and data buses, eight latched outputs for the low byte of the address are available. (continued)

FEATURES

- **8032 compatible instruction set**
- **44 MHz Operation from 3.3 to 5.5V**
- **HDLC support logic (Packetizer, 16 and 32 CRC, zero ID)**
- **24 pins for user programmable I/O ports**
- **8 pins programmable chip select logic or I/O for memory mapped peripheral eliminating glue logic**
- **3 external interrupt sources (programmable polarity)**
- **16 dedicated latched address pins**
- **Multiplexed data/address bus**
- **Instruction cycle time identical to 8032**
- **Buffered oscillator (or OSC/2) output pin**
- **1.8432 MHz UART clock available**
- **Bank select circuitry to support up to 128k of external program memory**
- **Also available in 100-Lead QFP and 100-Pin PGA packages**

BLOCK DIAGRAM



DESCRIPTION (continued)

The 73M2910L has two extra interrupt sources, an external interrupt and a HDLC interrupt. The HDLC interrupt has two registers associated with it; the HDLC Interrupt Register which is used to determine the source of the interrupt, and the HDLC Interrupt Enable Register that enables the source of the interrupt.

The state of the external interrupts can be read through a register allowing the interrupt pins to be used as inputs. The interrupt pins INT0 and INT1 can be either negative edge, positive edge or level triggered. The INT2 pin is always edge triggered.

Two buffered clock outputs have been added to support peripheral functions such as UARTs, modems and other clocked devices. The main internal processor clock frequency can be divided by 2 for power conservation in functional modes that only require half the clock speed.

Additional internal special function registers are used for firmware control over the HDLC Packetizer, the clocks and the programmable I/O ports.

To accommodate processor peripherals when operating at higher frequencies, the processor's timing has been altered to allow more address setup time for slower peripheral program ROM and memory mapped peripherals.

For low power applications the 73M2910L supports two power conservation modes: idle and power-down. In the power-down state the total current consumption is less than 10 µA at room temperature.

DEVELOPER'S NOTE:

The 73M2910L is also available in a 100-Pin PGA package for system developers. The PGA package is more convenient and reliable for development emulation systems than the other package styles. Emulation systems for the 73M2910L are available through Signum Systems, 11992 Challenger Court, Moorpark, CA 93021 (805) 523-9774.

8032 REFERENCE

This Document will describe the features unique to the 73M2910L. Please refer to a 8032 Programmer's Guide, Architectural Overview and Hardware Description for details on the instruction set, timers, UART, interrupt control, and memory structure.

REGISTER DESCRIPTION

INTERRUPTS

The core chip provides 8 sources of interrupt; 3 external interrupts, 3 timer interrupts, a serial port interrupt, and an HDLC interrupt. An external interrupt and an HDLC interrupt are unique to the 73M2910L. They do not exist in a normal 8032 product. Previously unused bits in the IE and IP registers are now serving functions for these additional interrupt sources. The interrupt vector addresses are as follows:

SOURCE	VECTOR ADDRESS
$\overline{\text{INT0}}$ (IE0)	003H
TF0	00BH
$\overline{\text{INT1}}$ (IE1)	013H
TF1	01BH
RI + TI	023H
TF2 + EXF2	02BH
$\overline{\text{INT2}}$ - ADDED INTERRUPT	033H
HDLC - ADDED INTERRUPT	03BH

The external interrupt sources, INT(2:0), come from dedicated input pins. The apparent polarity of these pins is individually controlled by bits in a special interrupt direction register, IDIR (address A9). The interrupt pins $\overline{\text{INT1}}$ and $\overline{\text{INT0}}$ can be either edge or level generated interrupts as indicated by bits 1 and 3 in the TCON Register (address 88). Pin $\overline{\text{INT2}}$ is always an edge generated interrupt. A flag is set when a falling transition (rising if IDIR bit 2 is set) on this pin is detected. This flag is automatically cleared when the interrupt is processed.

INTERRUPT ENABLE REGISTER (IE) SFR ADDRESS 0A8h
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EA	EX2	ET2	ES	ET1	EX1	ET0	EX0

NOTE: Bit 6 differs from the 8032. This is a reserved bit in the 8032 and is used as a mask bit for external interrupt 2 in the core implementation. When bit 6 is set to a 0, external interrupt 2 is disabled.

The mask bit for the HDLC interrupt source is bit 0 of the HDLC Control Register.

INTERRUPT PRIORITY REGISTER (IP) SFR ADDRESS 0B8h
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PHDLC	PX2	PT2	PS	PT1	PX1	PT0	PX0

NOTE: Bit 6 and bit 7 differ from the 8032. These are reserved bits in the 8032 and are used to determine the priority of external interrupt 2 and the HDLC in the core implementation. When bit 6 is set to a 1, the interrupt is set to the higher priority level.

INTERRUPTS (continued)

EXTERNAL INTERRUPT DIRECTION REGISTER (IDIR) SFR ADDRESS 092h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	$\overline{INT2}$	$\overline{INT1}$	$\overline{INT0}$	INTD2	INTD1	INTD0

These bits determine the polarity of the corresponding external signals INT(2:0) which will result in an interrupt and will also allow the user to directly read the logic level at the pads INT(2:0).

BITS (5:3) INT(2:0)

Bits (5:3) are read only bits that reflect the logic value at the corresponding pin. The value is not affected by bits (2:0).

BITS (2:0) Interrupt Polarity Control

If the bit is set to a 0, a falling edge will trigger the interrupt. If the bit is set to a 1, a rising edge will trigger the interrupt. Also, if the bit is set to a 1, level generated interrupts will occur when the corresponding pin is high and the internal pin signal to the timer controls will be inverted.

Bits 6 and 7 will always be read as 0's.

CLOCK CONTROL REGISTER SFR ADDRESS 0DAh
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Activity	CLK1 CTRL1	MCLK CTRL	CLK2EN	CLK2 CTRL1	CLK2 CTRL0	CLK1EN	CLK1 CTRL0

These bits determine the behavior at the CLK1OUT and CLK2OUT pins and allow the user to divide the main internal processor clock frequency by two for power conservation.

BIT 7

Bit 7 is an activity bit. It is cleared by a read of this register. If the activity bit is set it will prevent the 73M2910L from entering sleep mode.

BIT 6

When bit 6 = 1, CLK1OUT will be OSC/1.5 if bit 1 is a 1 and bit 0 is 0.

BIT 5	CLOCK OUT
0	OSC
1	OSC/2

BIT 5 Master Clock Control

When bit 5 is set to a 1 the internal processor clock is the oscillator frequency divided by 2. If this bit is a 0, the processor clock is the same frequency as the oscillator's.

BIT 4 Clock 2 Output Enable

Bit 4 enables the clock at the CLOCK 2 output pin if it is set to a 1. The CLOCK 2 pin output is held to a 0, by writing this bit to a 0. This will reduce system power if the clock pin is not used or if a power reduction mode is required.

BITS 3,2 Clock 2 Output Control

These bits determine the oscillator divisor for the CLOCK 2 output pin. They were designed to provide a 1.8432 MHz clock for an external UART given an oscillator frequency of 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz.

BIT 3	BIT 2	CLK 2 OUT	OSC FREQUENCY
0	0	OSC/7.5	13.824 MHz
0	1	OSC/6	11.059 MHz
1	0	OSC/12	22.118 MHz
1	1	OSC/10	18.432 MHz

BIT 1 Clock 1 Output Enable

Bit 1 enables the clock at the clock 1 output pin if it is set to a 1. The clock pin output is held to a 0, by writing a 0 to this bit. This will reduce system power if the clock pin is not used or if a power reduction mode is required.

Bit 6 is cleared to a 0 upon a reset.

BIT 0 Clock 1 Output Control

Bit 0 controls the frequency of the clock 1 output pin. The clock output is either the oscillator's output signal divided by two or a buffered oscillator output signal.

POWER SAVING MODES

Low Power Modes

The 73M2910L supports two power conservation modes, which are controlled by the PCON.1 and PCON.0 control bits of the PCON Register.

If PCON.0 is set, the 73M2910L will go into a power saving mode where the oscillator is running, clocks are supplied to the UART, timers, HDLC, and interrupt blocks, but no clocks are supplied to the CPU. Instruction processing and activity on the address and data ports is halted. Normal operation is resumed when an unmasked interrupt is requested or when a reset occurs.

If PCON.1 is set, the 73M2910L goes into its lowest power mode where the oscillator is halted. The total current consumption in this state should be less than 10 µa. The 73M2910L will start its oscillator and begin to return to normal operation when either a reset occurs, when a falling (rising if corresponding direction bit is set) edge of an unmasked external interrupt from pins INT(2:0) is detected, or when the USR5 (1:0) pins change to a state according to the USR5 port register. Edges used in wakeup modes are not filtered in the 73M2910L, so the user must be cautious of noise or small glitches inadvertently waking up the chip. From the time the edge that results in the wake up occurs, to the point at which an instruction is executed, depends on the oscillator start-up time. Three good oscillator pulses must be detected before the main internal clocks are generated.

During power-down mode, both the ALE and PSEN pins are pulled high since these signals often provide the output enable and chip enable for the ROM (active low). This ensures that the external components are in their lowest power state.

REGISTER DESCRIPTION (continued)

USR PROGRAMMABLE I/O

Port Control USR1, USR2, USR3, USR4, USR5

The core chip provides 32 user I/O pins. Each pin is programmed separately as either an input or as an output by a bit in a direction register. If the bit in the direction register is set to a 1, the I/O control will treat the corresponding pin as an input. If it is a 0, the pin will be treated as an output whose value is determined by the port data register. The USR1 and USR2 port registers are accessed through the internal SFR bus. The USR3 and USR4 ports are accessed through the external memory bus by a MOVX instruction. The USR4 port provides the user with an automatic chip select function if selected by the user. If the user does not require some (or any) of the chip select pin options, he may program the USR4 port pins to operate in the same way as USR3 port pins.

The USR Data Register contents determine pin values if chosen as an output. When reading from the data register's SFR address, the pin logic values are returned as data except when the port address is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data. When reading data from a data register that is mapped in the external memory space, the pin values are always returned as data.

The USR5 Register allows for 2 additional input pins. In normal operation these pins can be used as general purpose inputs. In power-down mode, the user can program either rising or falling transitions or logical combinations of these pins to wake up the chip.

USR 1 PORT

USR1 DATA SFR Address 90h
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR1.7	USR1.6	USR1.5	USR1.4	USR1.3	USR1.2	USR1.1	USR1.0

Bits in this register will be asserted on the USR1(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR1(7:0) except when address 90h is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data.

USR1 port signals are also used as timer controls. In applications where the external signals are required for timer count modes, the corresponding port pin should be configured as an input.

USR1.0 bit = TIMER0 T0 PIN
USR1.1 bit = TIMER1 T1 PIN
USR1.2 bit = TIMER2 T2 EX PIN
USR1.3 bit = TIMER2 T2 PIN

USR1 Port Direction (DIR1) SFR Address 91h
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR1.7	DIR1.6	DIR1.5	DIR1.4	DIR1.3	DIR1.2	DIR1.1	DIR1.0

This register is used to designate the USR1 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR1 pin is programmed as an output that will be driven by the corresponding USR1 data register bit. If the register bit is a 1, the corresponding pin will be treated as an input.

After a reset, the USR1 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 1 internally. The pins will assume normal I/O operation once the processor has written the port direction register. This feature will ensure a low current state at reset (you don't want to drive out against external inputs, and you don't want floating inputs).

USR2 PORT

USR2 Port Data SFR Address 0D8H
Bit Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR2.7	USR2.6	USR2.5	USR2.4	USR2.3	USR2.2	USR2.1	USR2.0

Bits in this register will be asserted on the USR2(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR2(7:0) except when address 0D8h is the destination address for a read-modify-write instruction. In this case, the latched register values are returned as data.

USR2 Port Direction (DIR2) SFR Address 0D9H
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR2.7	DIR2.6	DIR2.5	DIR2.4	DIR2.3	DIR2.2	DIR2.1	DIR2.0

This register is used to designate the USR2 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR2 pin is programmed as an output that will be driven by the corresponding USR2 I/O data register bit. If the register bit is a 1, the corresponding pin will treated as an input.

After a reset, the USR2 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 1 internally. The pins will assume normal I/O operation once the processor has written the port direction register. This feature will ensure a low current state at reset (you don't want to drive out against external inputs, and you don't want floating inputs).

USR3 PORT

USR3 Port Data External address 0000h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR3.7	USR3.6	USR3.5	USR3.4	USR3.3	USR3.2	USR3.1	USR3.0

Bits in this register will be asserted on the USR3(7:0) pins if the corresponding direction register bit is a 0. Reading this SFR's address will return data reflecting the values of pins USR3(7:0).

If the bank select feature is chosen, the USR3.7 pin acts as address bit 17 and USR3 data bit 7 is ignored.

USR3 PORT (continued)

USR3 I/O Port Direction (DIR3) External Address 0001h
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR3.7	DIR3.6	DIR3.5	DIR3.4	DIR3.3	DIR3.2	DIR3.1	DIR3.0

This register is used to designate the USR3 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR3 pin is programmed as an output that will be driven by the corresponding USR3 data register bit. If the register bit is a 1, the corresponding pin will be treated as an input.

After a reset, the USR3 pins will present a high impedance output state and the input values will not be driven from the pin, but will be driven to a 1 internally. The pins will assume normal I/O operation once the processor has written the USR3 port direction register. This feature will ensure a low current state at reset.

If the bank select feature is chosen, USR3.7 pin is forced to be an output.

BANK SELECT (BNKSEL) EXTERNAL ADDRESS 0002h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B7	B6	B5	B4	B3	BSEN	BS1	BS0

This register is used to accommodate systems where more than 64 kBytes (up to 128 kBytes) of program memory are required. Pin USR3.7 acts as an address pin, A16, if BSEN is set to a 1 and the processor is fetching an instruction and not data memory. If BSEN is set to a 1, A15 is also modified during instruction fetches as shown below. If BSEN is a 0, no alterations to address bit A15 are made, and pin USR3.7 is a function of USR3 bit 7 and DIR3 bit 7.

Bits (7:3) are general purpose read/write register bits.

A15	Value of the 16th address bit as it appears at pin A15.
A15'	Address from port 2 internal logic, the value that will appear as the most significant address bit if no bank select feature is chosen.
A16	Value of the 17th and MSB of the instruction address seen at the USR3.7 port pin, if the bank select feature is selected. If the bank select feature is not selected, USR3.7 acts as a normal USR3 I/O port pin.

BSEN	BS1	BS0	A15'	A15	A16	ADDRESS
0	*	*	0	0	USR3.7	0K - 32K
0	*	*	1	1	USR3.7	32K - 64K
1	0	0	0	0	0	0K- 32K
1	0	0	1	1	0	32K - 64K
1	0	1	0	0	0	0K - 32K
1	0	1	1	0	1	64K - 96K
1	1	0	0	0	0	0K - 32K
1	1	0	1	1	1	96K- 128K
1	1	1	0	0	0	0K- 32K
1	1	1	1	0	1	64K - 96K

* = Don't care

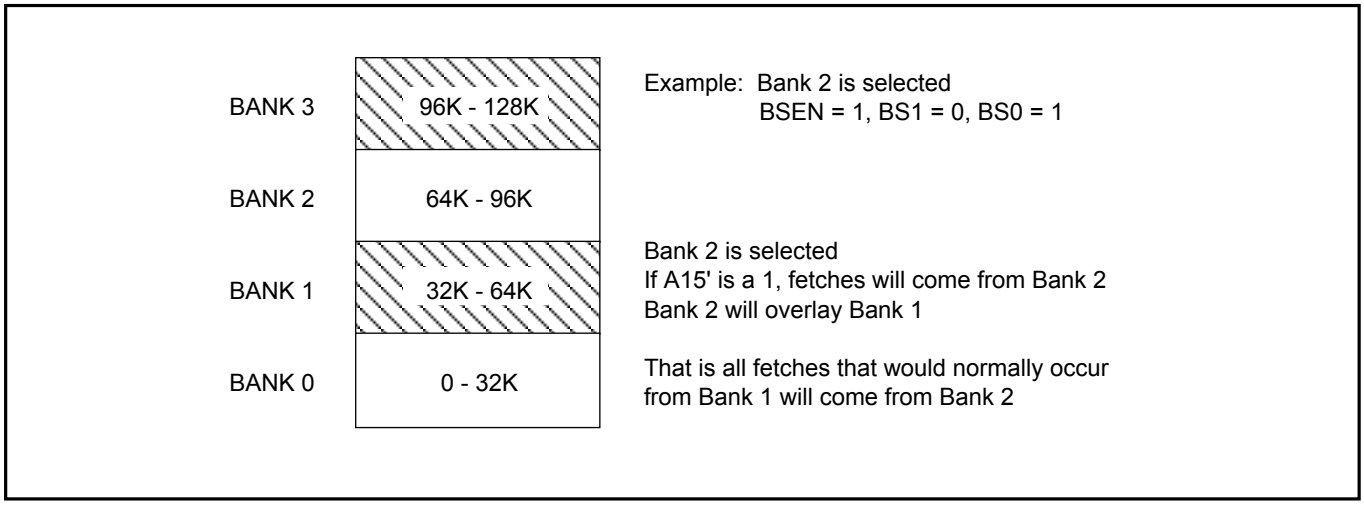


FIGURE 1: Bank Select

USR PROGRAMMABLE I/O (continued)

USR4 PORT

USR4 Port Data External Address 0003h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR4.7	USR4.6	USR4.5	USR4.4	USR4.3	USR4.2	USR4.1	USR4.0

Bits in this register will be asserted on the USR4(7:0) pins if the corresponding direction register bit is a 0 and if the corresponding bit in the Chip Select Enable Register, 0005, is set to a 0. Reading this register will return data reflecting the values of pins USR4(7:0).

USR4 I/O Port Direction (DIR4) External Address 0004h
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR4.7	DIR4.6	DIR4.5	DIR4.4	DIR4.3	DIR4.2	DIR4.1	DIR4.0

This register is used to designate the USR4 pins as either inputs or outputs. If the register bit is reset to a 0, the corresponding USR4 pin is programmed as an output that will be driven by the corresponding USR4 I/O data register bit if the corresponding bit in the Chip Select Enable Register, 0005, is set to a 0. If the register bit is a 1, the corresponding pin will treated as an input only if the corresponding bit in register 0005 is set to a 0.

After a reset, the USR4 pins will act as chip select outputs.

USR4 Port Chip Select Enable (CSEN) External Address 0005h
Byte Addressable
Reset State FFh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSEN 7	CSEN 6	CSEN 5	CSEN 4	CSEN 3	CSEN 2	CSEN 1	CSEN 0

This register is used to designate the USR4 pins as either user programmable I/Os or as chip select (CS0B - CS7B) functions on a pin by pin basis. This feature is designed to help reduce external glue logic for peripheral memory mapped devices. The chip select function is programmed by setting the appropriate bits in the CSEN Register. When a chip select pin is enabled by setting the corresponding CSEN bit to a 1, all data and direction information from registers 0003 and 0004 for this bit are ignored and the selected port becomes an output. If the bit is reset to a 0, the pin will be treated as a normal programmable user I/O pin as defined by registers 0003 and 0004.

The chip select pins have a defined memory map. The intent is that the outputs can be wire OR'ed together for a flexible selection of peripheral chip selects. All chip selects will be disabled (forced to a logic 1. It is assumed that all chip selects are active low) after the read or write is completed, and the appropriate chip select will be enabled as the next new external addresses is asserted. After a reset, the CSB pull-up devices are all enabled, that is, all chip select outputs are high. Users must account for this if these pins are intended to be general purpose I/Os.

The chip selects partition a 64K memory space as follows:

CHIP SELECT PIN	ADDRESS	# BYTES
RESERVED FOR INTERNAL USE	0000H - 00FFH	256
CS0 (USR4.0)	0100H - 01FFH	256
CS1 (USR4.1)	0200H - 03FFH	512
CS2 (USR4.2)	0400H - 07FFH	1K
CS3 (USR4.3)	0800H - 0FFFH	2K
CS4 (USR4.4)	1000H - 1FFFH	4K
CS5 (USR4.5)	2000H - 3FFFH	8K
CS6 (USR4.6)	4000H - 7FFFH	16K
CS7 (USR4.7)	8000H - FFFFH	32K

NOTE: External addresses 0000H-00FFH may not be read. These are reserved for 73M2910L internally defined registers

USR5 PORT

USR5 Port Register External Address 0006h
Byte Addressable
Reset State 60h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
USR5EN	USR5.0	USR5.1	POL5.0	POL5.1	ACTE0	ACTE1	AND01

This register allows user programmable wakeup capability. If this is not required, this register can be used to read external signals at the USR5.1 and USR5.0 pins.

Bit 7 USR5 Input Port Enable

Bit 7 is used to enable the USR5.1 and USR5.0 input circuitry. If this bit is a 0, the USR5 pin output circuitry is driven to a known level internally and any signal level at the pin is ignored. When set to a 1 the pin input circuitry is enabled and the values of these pins are reflected in bits 6 and 7. If these pins are not connected at the board level, this bit should remain at a 0 to keep the pin input circuitry from drawing unnecessary current.

The USR5 Register can be programmed such that a transition (bit 4 determines rising or falling) of USR5.0, a transition (bit 3 determines rising or falling) of USR5.1, or the logical combination of USR5.0 (bit 4 determines high or low level) AND USR5.1 (bit 3 determines high or low level) can wakeup the processor from its power-down mode.

BIT 6 USR5.0

Bit 6 reflects the value of chip pin USR5.0 if the USR5EN bit is set to a 1.

BIT 5 USR5.1

Bit 5 reflects the value of chip pin USR5.1 if the USR5EN bit is set to a 1.

USR5 PORT (continued)

BIT 4 USR5.0 Polarity

Bit 4 determines which edge or level is used in the wakeup detection circuit. A low level selects a rising transition and the true pin value of USR5.0 to the wakeup detection circuit. When this bit is set to a 1, a falling transition and complemented USR5.0 value is presented to the wakeup detection circuit.

BIT 3 USR5.1 Polarity

Bit 3 determines which edge or level is used in the wakeup detection circuit. A low level selects a rising transition and the true pin value of USR5.1 to the wakeup combinatorial circuit. When this bit is set to a 1, a falling transition and complemented USR5.1 value is presented to the wakeup detection circuit.

BIT 2 USR5.0 Edge Activity Enabled

When bit 2 is set to a 1, a transition of USR5.0 of the appropriate level as dictated by bit 4, will wake up the processor. If this bit is reset to a 0, edge activity on this pin is ignored.

BIT 1 USR5.1 Edge Activity Enabled

When bit 1 is set to a 1, a transition of USR5.0 of the appropriate level as dictated by bit 3, will wake up the processor. If this bit is reset to a 0, edge activity on this pin is ignored.

BIT 0 Combinatorial AND of USR5.0 and USR5.1 Level Enabled

When bit 0 is set to a 1, the value USR5.0 or its complimented value as dictated by bit 3, AND'ed with the value USR5.1 or its complimented value as dictated by bit 2, will wake up the processor. If this bit is reset to a 0, the levels of USR5.0 and USR5.1 are ignored.

USR5.0	USR5.1	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	WAKEUP
*	*	*	*	0	0	0	NO
0-1	*	0	*	1	*	*	YES
1-0	*	1	*	1	*	*	YES
*	0-1	*	0	*	1	*	YES
*	1-0	*	1	*	1	*	YES
0	0	1	1	*	*	1	YES
1	0	0	1	*	*	1	YES
0	1	1	0	*	*	1	YES
1	1	0	0	*	*	1	YES

* = Don't care

HDLC PACKETIZER

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDLC CONTROL 0 (HDLC0)	C0	WRXD	WPTXD	TXD	PRXD	RXD CTRL1	RXD CTRL0	PTXD CTRL1	PTX CTRL0
HDLC CONTROL 1 (HDLC1)	C1	RESET	CCIT	CRC PRE	RXCRC32	RXCRC16	TXCRC32	ZERO ID	HDLC INTEN
HDLC TX CONTROL (HTXC)	C2	0	0	0	DIV16 CLK	SEND ABORT	SEND CRC	SEND DATA	SEND FLAG
HDLC STATUS (HSTAT)	C3	INVAL CRC32	INVAL CRC16	TX UNDERRUN	RX UNDERRUN	INVAL FLAG	ABORT DETECT	IDLE DETECT	FLAG DETECT
HDLC INT ENABLE (HIE)	C4	TX RDY IE	RX RDY IE	TX RDY EN	RX RDY EN	INVAL FLAG IE	ABORT IE	IDLE IE	FLAG IE
HDLC INT SOURCE (HINT)	C5	0	0	0	0	0	NEW STATUS	RX READY	TX READY
RX DATA (RXD)	C6	RXDAT7	RXDAT6	RXDAT5	RXDAT4	RXDAT3	RXDAT2	RXDAT1	RXDAT0
TX DATA (TXD)	C7	TXDAT7	TXDAT6	TXDAT5	TXDAT4	TXDAT3	TXDAT2	TXDAT1	TXDAT0

FIGURE 2: HDLC SFR Registers

HDLC CONTROL REGISTERS

HDLC CONTROL REGISTER 0 (HDLC0) SFR ADDRESS 0C0h

Bit Addressable Reset State 00XX 0000 b
Bits 5 and 4 are read only bits

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WRXD	WPTXD	TXD R	PRXD R	RXD CTRL1	RXD CTRL0	PTX CTRL1	PTX CTRL0

This register controls the basic set-up of the DTE and modem pins RXD, TXD, PRXD, and PTXD.

BIT 7 WRXD

Bit 7 allows the processor to write directly to the 73M2910L RXD output pin. The value of bit 7 will appear at the RXD pin only if bit 3 is a 1 and bit 2 is a 1.

BIT 6 WPTXD

Bit 6 allows the processor to write directly to the 73M2910L PTXD output pin. The value of bit 6 will appear at the PTXD pin only if bit 1 is a 1 and bit 0 is a 0.

BIT 5 TXD

Bit 5 is a read only bit that reflects the value at the 73M2910L TXD input pin.

BIT 4 PRXD

Bit 4 is a read only bit that reflects the value at the 73M2910L PRXD input pin.

HDLC Control register 0 (hdlc0) sfr address 0c0H (continued)

BITS 3,2 RXD Control

Bit 3 and bit 2 control the source of the 73M2910L RXD output pin. This output goes to the DTE's RS232 interface. The source of this signal can be the core's UART TXD output, the PRXD output from a modem peripheral (clear channel), the DTE's TXD (echo), or the value written into bit 7 of this register.

BIT 3	BIT 2	RXD OUTPUT
0	0	UART TXD Output
0	1	PRXD Buffered (clear channel)
1	0	TXD Buffered (echo)
1	1	WRXD (bit 7)

BITS 1,0 PTXD Control

Bit 1 and bit 0 control the source of the 73M2910L PTXD output pin. This output goes to the modem's TX data input. The source of this signal can be the core's HDLC TX output, the DTE's TXD output (clear channel), or the value written into bit 6 of this register.

BIT 1	BIT 0	PTXD OUTPUT
0	0	HDLC TX Output
0	1	TXD Buffered (clear channel)
1	0	WPTXD (bit 6)
1	1	0

HDLC CONTROL REGISTER 1 (HDLC1) SFR ADDRESS 0C1h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDLC RST	CCITT	CRC PRE	RXCRC 32	RXCRC 16	TXCRC CTRL	ZERO ID	HDLC INTEN

This register controls the basic set-up of the HDLC block. This register will be written during initialization and not during normal message processing.

BIT 7 HDLC Software Reset

When bit 7 is a 1, the HDLC circuit is reset and held in a low power state and no interrupts from the HDLC circuitry will be generated. When a 0 is written to this bit, the HDLC circuit will behave according to its control bits.
Bit 7 and the power-on-reset signal are OR'ed together to form a reset signal for the HDLC block.

Bit 7 is cleared to a 0 upon a power-up-reset.

BIT 6 CRC Type Control

Bit 6 selects the CRC algorithm used in the 16-bit CRC calculation. There are two types of 16-bit CRCs commonly used, CRC16 and the CCITT 16-bit CRC. If this bit is set to a 1, the CCITT type is selected.

Bit 6 is cleared to a 0 upon a reset.

BIT 5 CRC Preset Value

Bit 5 selects the reset value for the CRC generator and receiver. If this bit is set to a 1, the CRC generator and receiver are initialized to ones and if this bit is reset to a 0, they are initialized to 0s. This bit should be set to a 1 for most CCITT polynomials.

Bit 5 is cleared to a 0 upon a reset.

BITS 4,3 RX CRC Control

Bit 4 and bit 3 determine the type of CRC remainder that will be checked at the end of a received frame. There is a 16-bit CRC, and a 32-bit CRC that the HDLC block can support. If both bit 4 and bit 3 are reset, bits 7 and 6 of the HDLC Status Register will be held to a 0. If both bit 4 and bit 3 are 1s, a special CRC search mode is enabled where both bits 7 and 6 of the HDLC Status Register are enabled. This mode is used during a connection to determine which CRC is used by the initiating modem. If the 16-bit CRC remainder is not matched at the end of the received frame, then bit 6 of the HDLC Status Register is set. If the 32-bit CRC remainder is not matched at the end of the received frame, then bit 7 of the HDLC Status Register is set. Once the correct CRC type is established during a connection, either bit 4 or bit 3 should be set to a 1 enabling the appropriate invalid CRC status bit.

BIT 4	BIT 3	CRC TYPE
0	0	NO CRC Check
0	1	Enable CRC16 Status
1	0	Enable CRC32 Status
1	1	Enable CRC16 Status and CRC32 Status

BIT 2 TXCRC Control

Bit 2 controls the CRC type to be transmitted. If bit 2 is reset to a 0, a 16-bit CRC will be transmitted with the SEND CRC command. If bit 2 is set to a 1, a 32-bit CRC will be transmitted.

BIT 1 Zero Insert/Delete Control

When bit 1 is set to a 1, a 0 will be transmitted if either the send data or send CRC bits of the HDLCTX control are set after five consecutive 1s have been transmitted. Also, when this bit is set, a 0 will be removed from the received data stream if it immediately follows a pattern of a 0 followed by five consecutive ones. If bit 1 is reset to a 0, no 0s will be inserted during transmission, and no 0s will be deleted during reception.

Bit 1 is cleared to a 0 upon a reset.

BIT 0 HDLC Interrupt Enable

When bit 0 is reset to a 0, the HDLC will be prevented from generating an interrupt. The status bits that indicate the source of the interrupt can still be set allowing the HDLC block to be serviced in a polled mode.

Bit 0 is cleared to a 0 upon reset.

HDLC CONTROL REGISTERS (continued)

HDLC TX CONTROL REGISTER (HTXC) SFR ADDRESS 0C2h
Byte Addressable
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	DIV16 CLK	SEND ABORT	SEND CRC	SEND DATA	SEND FLAG

This register is used to control the source of data that appears on the PTXD pin. Bits are shifted out on every rising edge of the PTXCLK pin input. If no control bits are set, or more than one TX control bit is set, the PTXD pin will go to a binary 1.

BITS 7-5 Always 0

BIT 4 16X Clock Select

Under normal synchronous operation, the PTXCLK and PRXCLK are used to receive and transmit data PRXD and PTXD. The clock rate is equal to the data rate. In asynchronous modes, a clock 16 times the bit rate is provided at PTXCLK and PRXCLK.

When bit 4 is set to a 1 during asynchronous operation, the clocks at the PTXCLK and PRXCLK input pins are divided by 16 to provide transmit and receive shift clocks. An internal clock for sampling incoming PRXD data is synchronized by detecting any edge on the PRXD data pin. The rising edge of this internal clock, used to sample incoming data, is delayed from the falling data edge by 8 PRXCLK periods and will continue at this phase and at a PRXCLK/16 frequency until another PRXD edge is detected.

If bit 4 is reset to a 0, the rising edge of PTXCLK is used to sample the data at PRXD, and the falling edge of PTXCLK is used to shift new data onto PTXD.

BIT 3 Abort

When bit 3 is set to a 1, a series of consecutive ones will immediately be transmitted through the PTXD pin on every falling edge of PTXCLK. The message will have been aborted after 2 TX ready interrupts are received. No zeros will be inserted during the abort transmission.

BIT 2 Send CRC

When bit 2 is set, the bytes in the TX CRC generator will be inverted and serially transmitted to the PTXD output on the falling edge on PTXCLK as soon as the present data byte transmission is completed. If bit 1 of the HDLC Control Register is a 0, a 0 will be inserted into the CRC data stream after five consecutive ones are transmitted. As soon as the last bit of the CRC is sent, a series of flags will be automatically sent until another TX control bit is set. No TX ready interrupts will be generated during the transmission of the CRC bytes. A TX ready interrupt will be generated as the first bit of each flag byte is transmitted indicating that the CRC transmission has been completed. This should be cleared by a dummy write to the TX Data Register.

BIT 1 Send Data

When bit 1 is set, the data is the TX Data Register will be serially transmitted through the PTXD pin on every falling edge of PTXCLK, LSB first. If bit 1 of the HDLC Control Register is a 0, a 0 will be inserted into the data stream after five consecutive 1s are transmitted. After all eight data register bits have been sent, the HDLC will continue to send data by loading the parallel serial transmit register with new transmit register data, unless either a TX underrun is detected or one of the other TX control bits has been set. This bit will be cleared by the HDLC circuitry as soon as a TX underrun is detected. A TXRDY interrupt will be generated as the first data of each data byte is transmitted. Bit 1 will be cleared to a 0 upon a reset.

BIT 0 Send Flag

When bit 0 is set, a pattern of 7E will be transmitted to the PTXD output as soon as either the next data byte or CRC has completed transmission. No 0s will be inserted during the flag transmission. When bit 0 is reset back to a 0, the HDLC circuitry will complete the flag byte in progress and then transmit according to bits in the TX Control Register. TX ready interrupts will be generated as each byte of flag transmission is initiated.

HDLC STATUS REGISTER (HSTAT) SFR ADDRESS 0C3h
Byte Addressable
Read Only Register
Reset State 00h

If any of the HDLC status bits are set, bit 1 of the HDLC Interrupt Register (new status) will be set if the corresponding bit in the HDLC Interrupt Enable Register is set.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INVAL CRC32	INVAL CRC16	TX UNDRN	RX OVRN	INVAL FLAG	ABORT DET	IDLE DET	FLAG DET

BIT 7 Invalid CRC 32

Bit 7 will be set if the CRC search mode or the 32-bit CRC is enabled by the HDLC Control Register and an incorrect remainder for the 32-bit CRC is detected at the last received byte prior to receiving a flag.

Bit 7 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 6 Invalid CRC 16

Bit 6 will be set if the CRC search mode or the 16-bit CRC is enabled by the HDLC Control Register and an incorrect remainder for the 16-bit CRC is detected at the last received byte prior to receiving a flag.

Bit 6 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 5 TX Underrun

When Bit 5 is set, a transmit underrun condition has been detected. This is a condition where the HDLC has finished transmitting a message byte, but no new data has been loaded into the TX Data Register, and no other transmit control bit has been set. This bit will be set only if the send data bit, bit 1 of the TX Control Register is set. The transmit data is double buffered since the TX Data Register is downloaded into a TX Serial Register when the HDLC begins to transmit a new data byte. At the time of loading the TX Serial Register, a TX ready interrupt is generated. This interrupt must be serviced by either loading a new data byte (the next data byte to be transmitted) into the TX Data Register, or by setting another TX control bit, before the current data byte has completed transmission (at which point another TX ready interrupt would be generated). If a TX underrun is detected, the HDLC will abort the current transmission by sending continuous ones and will reset the send data control bit in the TX Control Register.

Bit 5 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

HDLC STATUS REGISTER (HSTAT) SFR ADDRESS 0C3h (continued)

BIT 4 RX Overrun

When bit 4 is set, a receive overrun condition has been detected. This is a condition where the HDLC has received a new byte, but the last received data byte has not yet been read from the RX Data Register. As soon as a new data byte has been received in an eight-bit serial register, it is loaded into the RX Data Register and a new RX data interrupt is generated. If this interrupt is not serviced by reading the RX Data Register during the time another new data byte is received, the RX overrun status bit will be set. The new received data will not overwrite the older unread data.

Bit 4 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 3 Invalid Flag

When bit 3 is set, an invalid flag has been detected. This is a condition where a 7E pattern with no inserted 0s is detected, and this pattern did not originate on a byte boundary. Note, two consecutive flags may share a 0, so that the second (or subsequent) flag may not appear to be on a byte boundary. This condition does not result in an invalid flag indication.

Bit 3 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 2 Abort Detect

When bit 2 is set, an abort condition has been detected. This is a condition where seven consecutive ones, with no inserted zeros, are received after an active state. Bit 2 will be cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 1 Idle Detect

When bit 1 is set, the first indication of an idle state is detected. An idle state is declared when 15 consecutive ones, with no inserted zeros, are received after an active state.

Bit 1 will be cleared upon a reset and is cleared by a read of the HDLC Stat Register.

BIT 0 Flag Detect

When bit 0 is set, the HDLC has received a 7E pattern with no inserted 0's. Bit 0 will by cleared upon a reset and is cleared by a read of the HDLC Stat Register.

HDLC INTERRUPT ENABLE REGISTER (HIE) SFR ADDRESS 0C4h
Byte Addressable
Reset State 00h

If the bit is set, the corresponding interrupt source is enabled.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX RDY IE	RX RDY IE	TX RDY EN	RX RDY EN	INVAL FLG IE	ABORT IE	IDLE IE	FLAG IE

BIT 7 Transmitter Ready Interrupt Enable

When bit 7 is set, an HDLC interrupt will be generated if bit 0 (TX RDY) of the HDLC Interrupt Register is also set. If bit 7 is reset to a 0, no HDLC interrupt indication will be given as TX RDY is set. This interrupt enable allows the TX RDY to be a polled bit. Note that bit 5 of this register is a pre-mask to the TX RDY bit, that is, it will prevent the TX RDY bit from ever being set.

BIT 6 Receiver Ready Interrupt Enable

When bit 6 is set, an HDLC interrupt will be generated if bit 1 (RX RDY) of the HDLC Interrupt (HINT) Register is also set. If bit 6 is reset to a 0, no HDLC interrupt indication will be given as RX RDY is set. This interrupt enable allows the RX RDY to be a polled bit. Note that bit 4 of this register is a pre-mask to the RX RDY bit, that is, it will prevent the RX RDY bit from ever being set.

BIT 5 Transmit Ready Enable

Bit 5 is used to enable the TX RDY and TX underrun interrupt sources. When bit 5 is set, the transmitter ready indication will set bit 0 of the HDLC Interrupt Register. The TX RDY indication will go active as the first bit of a message byte is being transmitted, except during CRC transmission. Also, if this bit is set, the TX underrun condition will result in a new status interrupt. If bit 5 is reset to a 0, bit 0 of the HDLC Interrupt Register will not be set, and no corresponding HDLC interrupt will be generated. Also, a TX underrun condition, as indicated by bit 5 of the HDLC Status Register, will not result in an HDLC interrupt or in setting the new status interrupt bit.

BIT 4 Receiver Ready Enable

Bit 4 is used to enable the RX RDY and RX overrun interrupt sources. When bit 4 is set, the receiver ready indication will set bit 1 of the HDLC Interrupt (HINT) Register. The RX RDY indication will go active when a data byte (a byte that is not a flag, idle, or an abort pattern) is loaded into the RX Data Register. Also, if this bit is set, the RX overrun condition will result in a new status interrupt. If bit 4 is reset to a 0, bit 1 of the HDLC Interrupt Register will not be set, and no corresponding HDLC interrupt will be generated. Also, a RX overrun condition, as indicated by bit 4 of the HDLC Status (HSTAT) Register, will not result in a HDLC interrupt or in setting the new status interrupt bit.

BIT 3 Invalid Flag Interrupt Enable

When bit 3 is set, a HDLC interrupt will be generated if bit 3 (INVALID FLAG) of the HDLC Status (HSTAT) Register is also set. If bit 3 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt (HINT) Register will not be set as a result of an invalid flag boundary detection and no HDLC interrupt will be generated.

BIT 2 Abort Detect Interrupt Enable

When bit 2 is set, a HDLC interrupt will be generated if bit 2 (ABORT DETECT) of the HDLC Status (HSTAT) Register is also set. If bit 2 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt (HINT) Register will not be set as a result of an abort pattern detection and no HDLC interrupt will be generated.

BIT 1 Idle Detect Interrupt Enable

When bit 1 is set, an HDLC interrupt will be generated if bit 1 (IDLE DETECT) of the HDLC Status (HSTAT) Register is also set. If bit 1 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt (HINT) Register will not be set as a result of an idle pattern detection and no HDLC interrupt will be generated.

HDLC INTERRUPT ENABLE REGISTER (HIE) SFR ADDRESS 0C4h (continued)

BIT 0 Flag Detect Interrupt Enable

When bit 0 is set, a HDLC interrupt will be generated if bit 0 (FLAG DETECT) of the HDLC Status (HSTAT) Register is also set. If bit 0 is reset to a 0, bit 2 (NEW STATUS) of the HDLC Interrupt (HINT) Register will not be set as a result of a flag pattern detection and no HDLC interrupt will be generated.

HDLC INTERRUPT SOURCE REGISTER (HINT) SFR ADDRESS 0C5h
Byte Addressable
Read Only Register
Reset State 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	NEW STATUS	RXRDY	TXRDY

This register is used to determine the source of HDLC interrupts. If one or more of these register bits are set, the corresponding HDLC interrupt will go active if bit 0 of the HDLC Control 1 (HDLC1) Register is set to a 1.

BIT 2 New Status

When bit 2 is set, an unmasked HDLC status bit from the HDLC Status (HSTAT) Register is set.

Bit 2 will by cleared upon a reset and is cleared by a read of the HDLC Status Register.

BIT 1 RX Ready

When bit 1 is set, a new received byte has been loaded into the RX Data (RXD) Register. Note, received bits that are flag, abort, or idle patterns are not considered data, and will not be loaded into the RX Data Register. All inserted 0s have been removed from this byte. The RX Data Register must be read prior to the completed reception of the next data byte.

Bit 1 will by cleared upon a reset and is cleared by a read of the RX Data Register.

BIT 0 TX Ready

Bit 0 is set if any HDLC TX control (HTXC) bits 3:0 are set as the first bit of data, flag or an idle byte is being transmitted. While transmitting the current byte, the HDLC state machines are ready for commands pertaining to the next byte to be transmitted. A new data byte must be loaded into the TX Data (TXD) Register to clear the TX ready status bit.

Bit 0 will by cleared upon a reset and is cleared by writing to the TX Data Register.

RX DATA REGISTER (RXD) SFR ADDRESS 0C6h
Byte Addressable
Read Only Register
Reset State XXh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RX DAT7	RX DAT6	RX DAT5	RX DAT4	RX DAT3	RX DAT2	RX DAT1	RX DAT0

BITS 7-0 Received Data Byte

Bit 7 through bit 0 is the received data byte (LSB is received first) with all inserted 0s removed. A data ready interrupt will be generated when a new data byte is received. Reading this register will clear the data ready interrupt.

TX DATA REGISTER (TXD) SFR ADDRESS 0C7h
Byte Addressable
Write Only Register
Reset State XXh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX DAT7	TX DAT6	TX DAT5	TX DAT4	TX DAT3	TX DAT2	TX DAT1	TX DAT0

BITS 7-0 Transmit Data Byte

Bit 7 through bit 0 will be transmitted at the next byte boundary (LSB first) if the HDLC TX control send data bit is set. The HDLC will insert all necessary 0s. A TX ready interrupt will be generated when a new data byte can be loaded into the TX Data Register. Writing this register will clear the TX ready interrupt.

REGISTER DESCRIPTION (continued)

CRC GENERATION

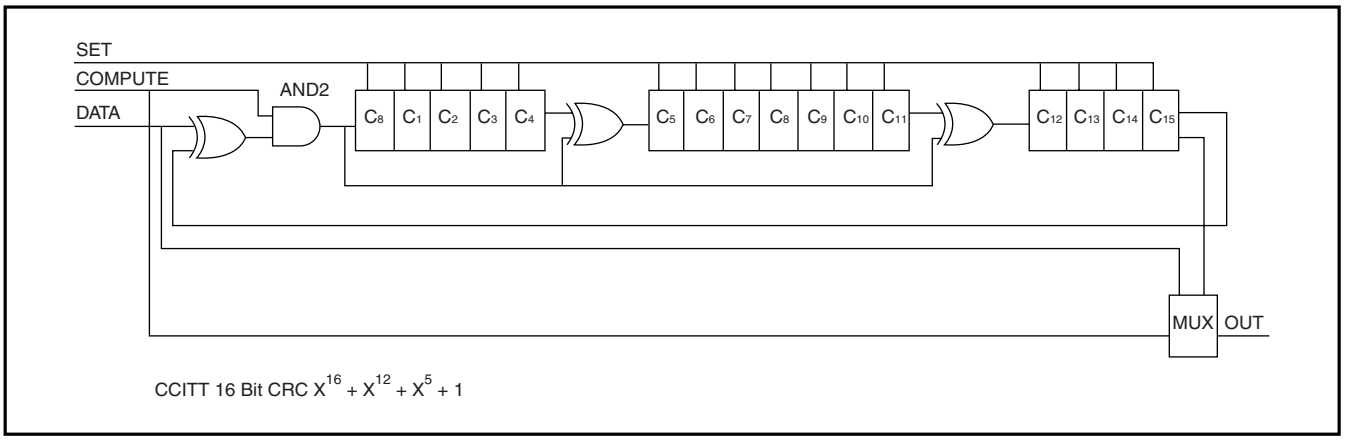


FIGURE 3: CCITT TYPE

CCITT Type

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all ones. The bits are shifted in and operated on by the generating polynomial, $X^{16} + X^{12} + X^5 + 1$. During CRC transmission, the bytes in the CRC generating logic are inverted and transmitted, high order bit first.

The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator (also $X^{16} + X^{12} + X^5 + 1$) should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1111 0000 1011 1000 (X^0 through X^{15}, respectively) should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

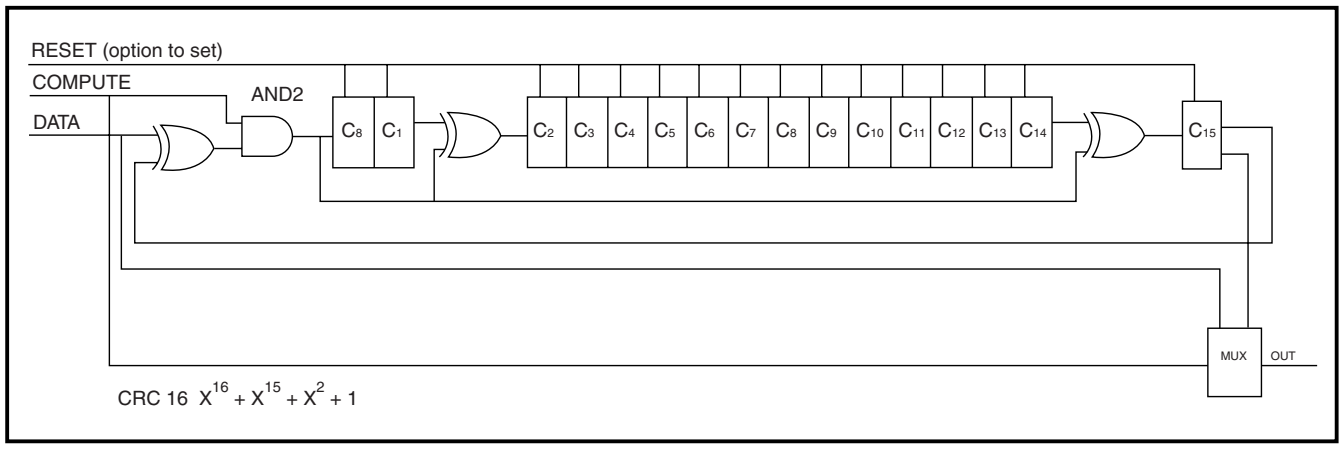


FIGURE 4: CRC 16

CRC 16

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all 0s. The bits are shifted in and operated on by the generating polynomial, $X^{16} + X^{12} + X^5 + 1$. During CRC transmission, the bytes in the CRC generating logic are transmitted, high order bit first.

The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator (also $X^{16} + X^{12} + X^5 + 1$) should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1111 0000 1011 1000 should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

CRC GENERATION (continued)

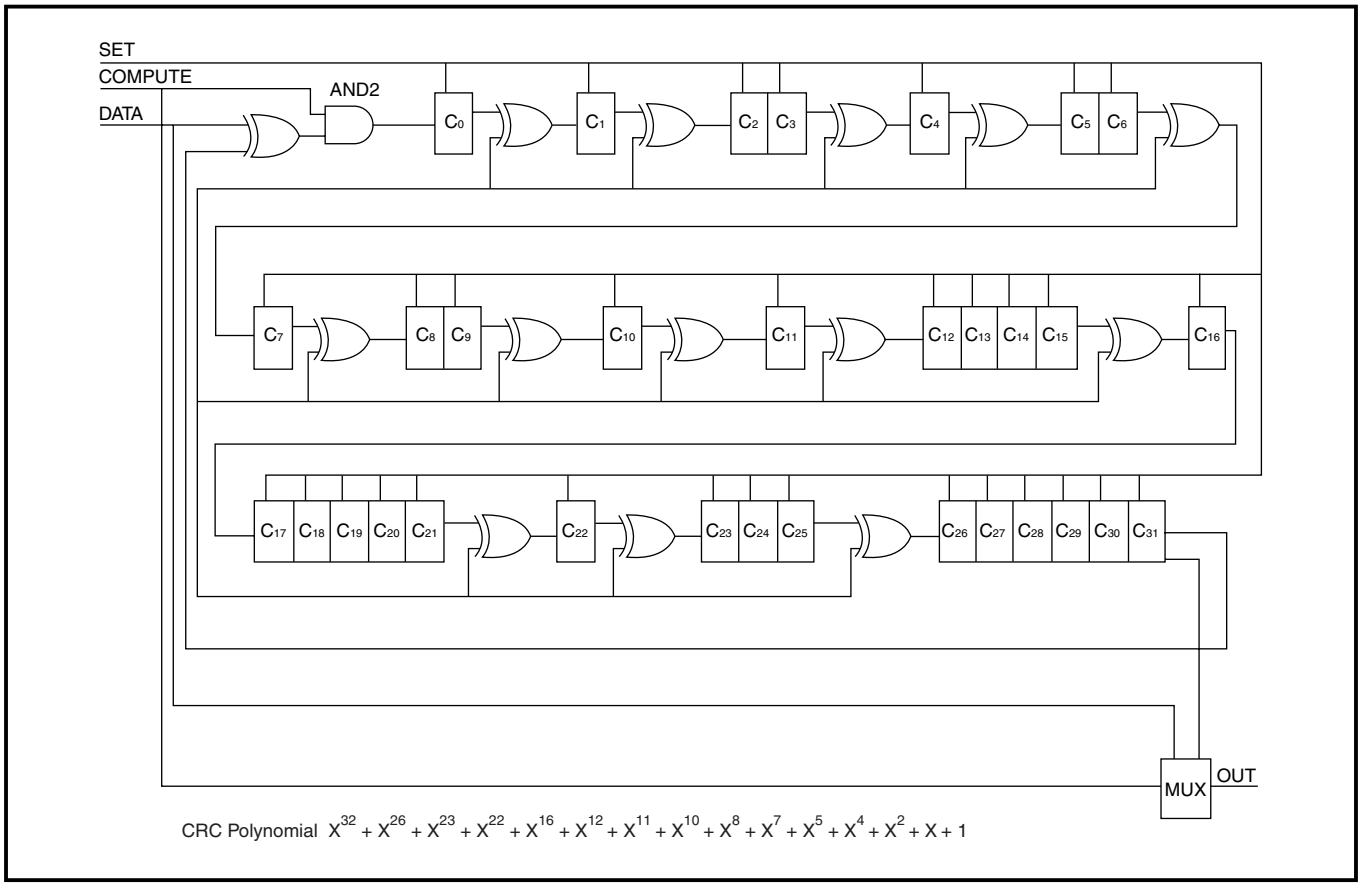


FIGURE 5: 32-BIT CRC

CRC 32

The CRC check field is generated by the transmitter. The computation starts with the first transmitted bit after the opening flag and stops at the last data bit prior to the frame check sequence bytes, and excludes inserted 0s. The CRC generating logic is initialized to all ones. The bits are shifted in and operated on by the generating polynomial, $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$. During CRC transmission, the bytes in the CRC generating logic are inverted and transmitted, high order bit first. The receiver also initializes its CRC computation logic to all ones after the beginning flag. Its polynomial generator should see the same value as the transmitter's polynomial generator as the last data bit is received. Note the receiver's polynomial generator does not process inserted 0s. After the bytes are received in the frame check sequence, a remainder of 1101 1110 1011 1011 0010 0000 1110 0011 (X^0 through X^{32}, respectively) should be detected in the receiver's polynomial generator. If this is not the case, it is assumed that the preceding frame was in error and an invalid CRC is declared.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
PSEN	O	Program store enable. This output occurs only during a fetch to external program memory.
RESET	I	Input which is used to initialize the processor.
VND	GND	Negative digital voltage ground
OSCIN	I	Crystal input for internal oscillator, also input for external source.
OSCOUT	O	Crystal oscillator output.
VPD	I	Positive digital voltage (+5V Digital Supply)
CLKOUT1	O	Clock output programmable either OSC/2, OSC/1 or logic 0.
CLKOUT2	O	Clock output 1.8432 MHz clock for an external UART given an oscillator frequency of 11.0592 MHz, 22.1184 MHz, 18.432 MHz, or 13.824 MHz.
TXD	I	Serial input port to 73M2910L from DTE same as RXD UART input.
RXD	O	Serial output port of 73M2910L UART to DTE.
PTXCLK	I	Input clock used to transmit data PTXD.
PTXD	O	HDLC Packetizer TX output. This pin can also be programmed to the DTE's TXD output (clear channel) or the value written into bit 6 of the HDLC Control Register. Connects to modem device TXD.
PRXCLK	I	Input clock used to receive data PRXD.
PRXD	I	Serial input port (from modem device) to HDLC Packetizer.
$\overline{INT}(0)$-$\overline{INT}(2)$	I	External interrupt 0,1 and 2.
USR1.0 - USR1.7	I/O	USR programmable I/O port.
USR2.0 - USR2.7	I/O	USR programmable I/O port.
USR3.0 - USR3.7	I/O	USR programmable I/O port. If the bank select feature is chosen, USR (7) acts as address bit 17 and USR3 data bit 7 is ignored. Register BNKSEL bit 2 (BSEN) enables bank select, bit 1 (BS1) and bit 0 (BS0) select the appropriate bank.
USR4.0 - USR4.7	I/O	USR programmable I/O port also chip select enable.
USR5.0 - USR5.1	I/O	General purpose input port, can also be used for wakeup.
RD	O	Output strobe activated during a bus read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory.
WR	O	Output strobe during a bus write. Used as a write strobe to external data memory.
ALE	O	Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.
AD(0)-AD(7)	I/O	Data bus lines-I/O for devices that require multiplexed address and data bus.
A(0)-A(15)	O	Address bus lines-output latched address for devices that require separate data and address bus.
NO CONNECTS(NC)		No connections, leave open. Not a user pin.

MEMORY MAPS

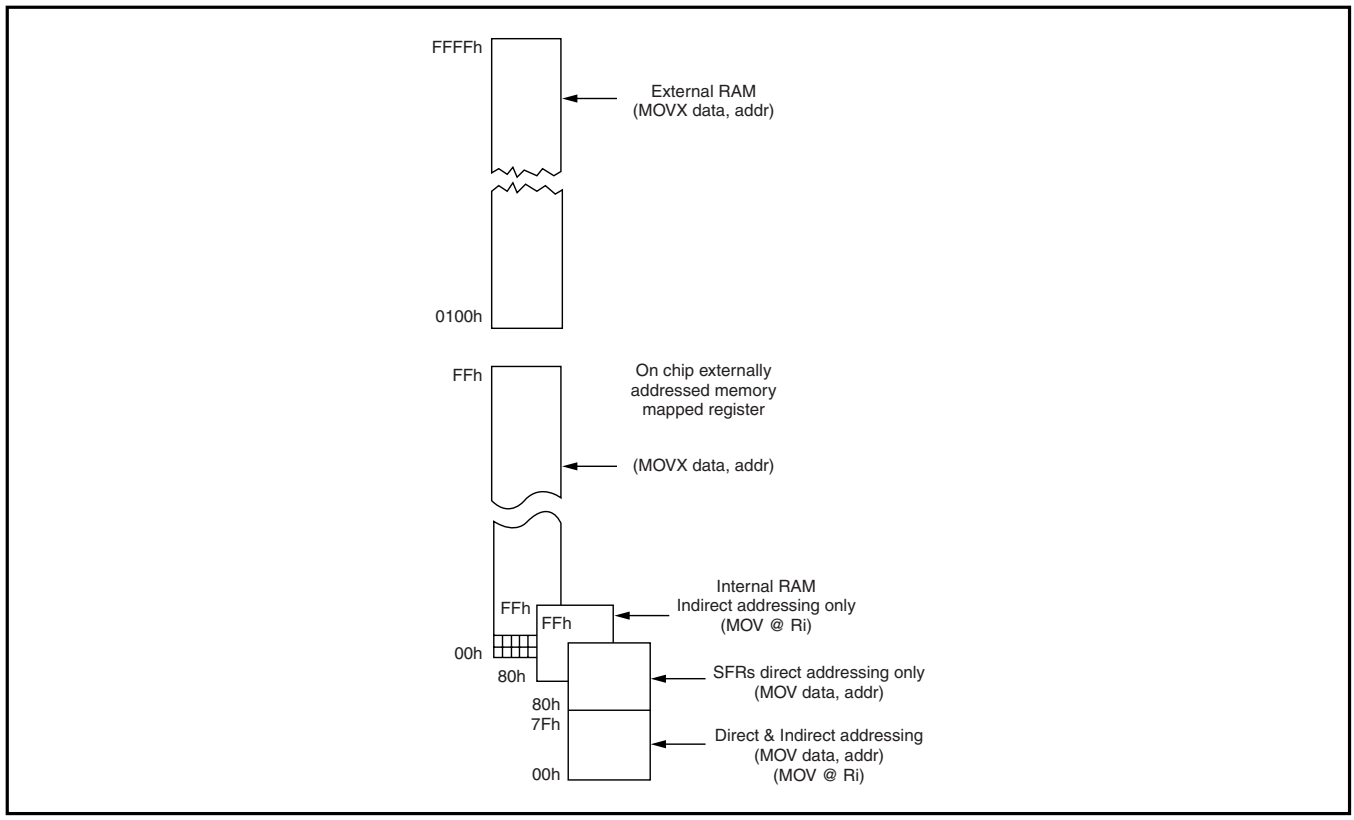


FIGURE 6: Memory Map

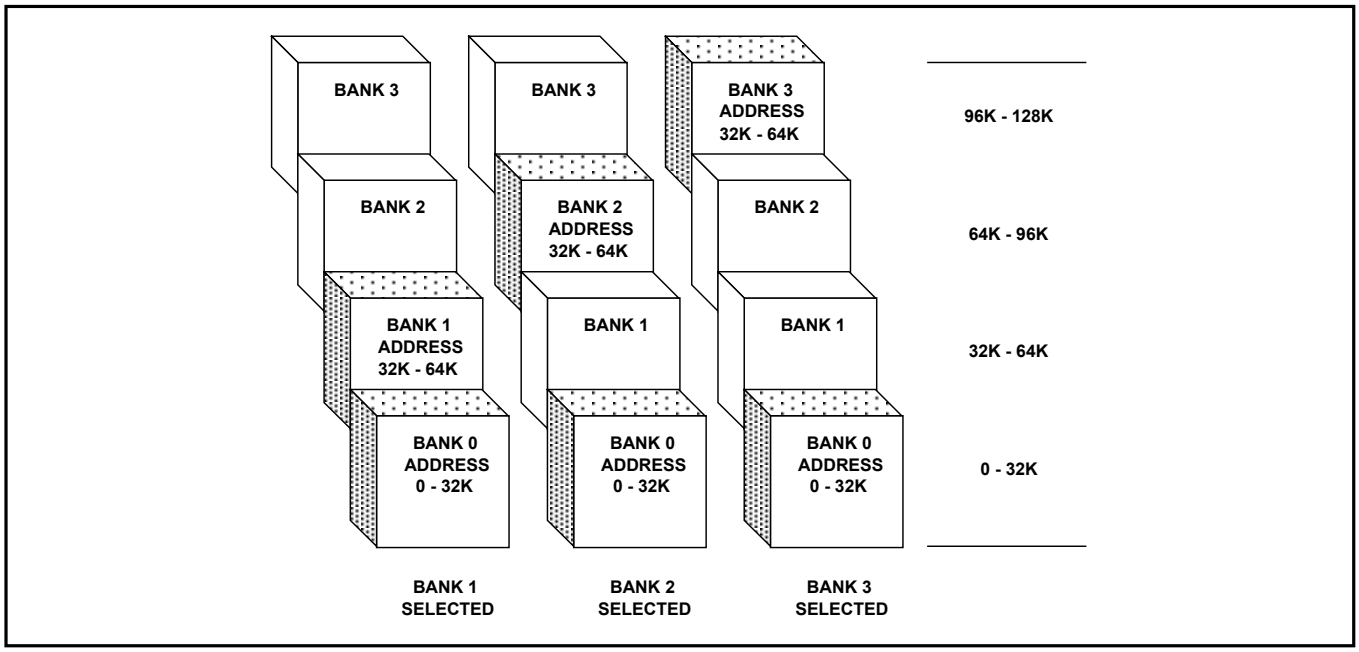


FIGURE 7: 128K of Bank-Selected Program Memory

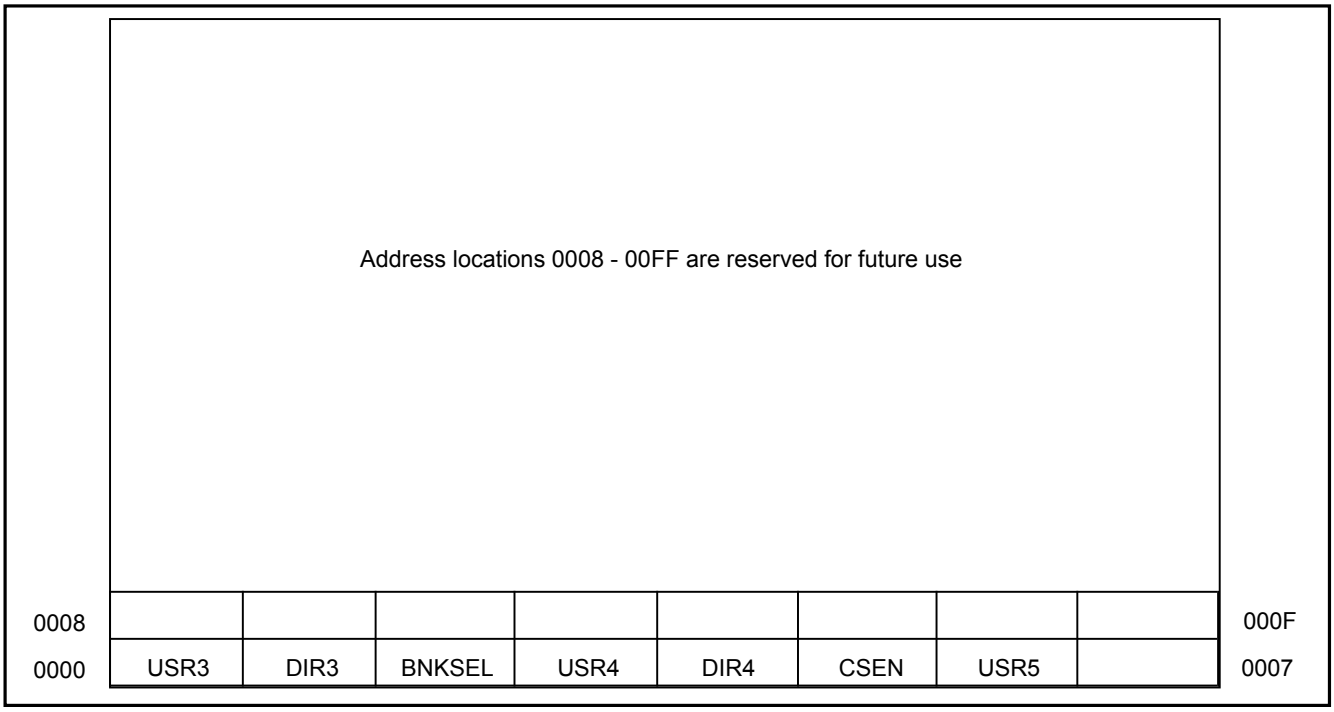


FIGURE 8: Memory Mapped Registers

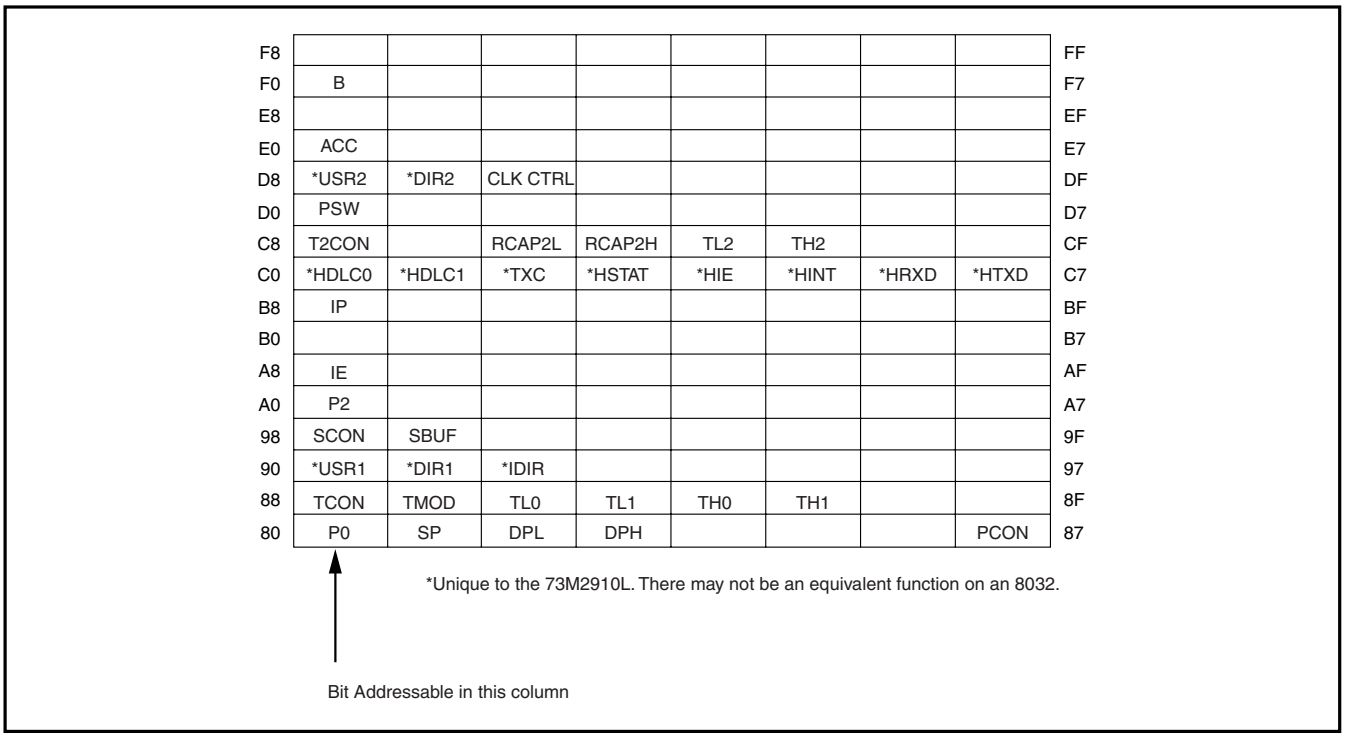


FIGURE 9: 73M2910L SFR Map

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Recommended conditions apply unless otherwise specified.

PARAMETER	RATING
Supply Voltage	-0.5 to +7.0V
Pin Input Voltage	-0.5 to Vcc +0.5V
Storage Temperature	-55 to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	3 to 5.5V
Oscillator Frequency	DC to 44 MHz
Operating Temperature	-40 to +85°C

DC CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input Low Voltage (Except PTXCLK, PRXCK, OSCIN, RESET, TEST)	VIL		-0.5		0.2 Vcc 0.1	V
Input Low Voltage OSCIN, RESET, TEST	VIL		-0.5		0.2 Vcc	V
Input Low Voltage PTXCLK, PRXCLK	VIL		-0.5		0.2Vcc-0.3	V
Input High Voltage (Except OSCIN, RESET, TEST)	VIH		0.5 Vcc		Vcc + 0.5	V
Input High Voltage OSCIN, RESET, TEST	VIH		0.7 Vcc		Vcc + 0.5	V
Output Low Voltage (Except OSCOUT)	VOL	Iol = 3.2 mA			0.45	V
Output Low Voltage OSCOUT	VOLOSC	Iol = 1.5 mA			0.7	V
Output High Voltage (Except OSCOUT)	VOH	Ioh = -3.2 mA	Vcc - 0.45			V
Output High Voltage OSCOUT	VOHOSC	Ioh = 1.5 mA	Vcc - 0.7			V
Input Leakage Current	IIL	Vss < Vin < Vcc			±10	µA
Maximum Power Supply Normal Operation	IDD1	22 MHz 30 pF/pin			40	mA
Maximum Power Supply idle mode	IDD2	22 MHz			10	mA

DC CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Maximum Power Supply power-down mode	IDD3				10	µA
Pin Capacitance	CIO	@1 MHz			10	pF

AC TIMING

The 73M2910L timing is very similar to the 8032 except in AD(7:0), the multiplexed address data port known as port 0 in the 8032. Its timing has been altered somewhat to allow more address setup time for peripheral program ROM and memory mapped peripherals. This is important for operation above 22 MHz. The 8032 has a “dead” cycle of one oscillator period between the time PSEN goes high, indicating that the instruction ROM will release the AD(7:0) bus, to the time the processor will assert address on the AD(7:0) bus. This dead time of one whole oscillator cycle has been shortened to approximately 15 ns after the PSEN (or RD) signal is sensed to be high.

The timing specification for TPXIZ and TRHDZ of a maximum of 20 ns can be violated at the expense of increased operating current. The 73M2910L will begin asserting the AD(7:0) bus approximately 20 ns after PSEN or RD go high. This should be ample time for the control signals in the peripheral device to turn off their pad drivers. If the peripheral device does not release the bus promptly, there will be a short time where there is contention on the AD(7:0) bus between the processor and peripheral. This should not prevent proper operation, but it will increase operating current slightly.

EXTERNAL PROGRAM MEMORY READ TIMING

Oscillator Frequency	FOSC		0		44	MHz
Oscillator Period	TOSC		22.7			ns
ALE Pulse Width	TLHLL		2TOSC-10			ns
Address Valid To ALE Low	TAVLL		TOSC			ns
Address Valid ALE Low	TLLAX		TOSC-10			ns
ALE Low to PSEN Low	TLLPL		TOSC-10			ns
$\overline{\text{PSEN}}$ Pulse Width Low	TPLPH		3TOSC-20			ns
$\overline{\text{PSEN}}$ Low to Valid Inst In	TPLIV				3TOSC-50	ns
Address to Valid Inst In	TAVIV				6TOSC-32	ns
Input Instr Hold-$\overline{\text{PSEN}}$ High		TPXIX		0		ns
PSEN Instr Float-$\overline{\text{PSEN}}$ High		TPXIZ			20+	ns
PSEN Low to Address HighZ		TPLAZ			10	ns

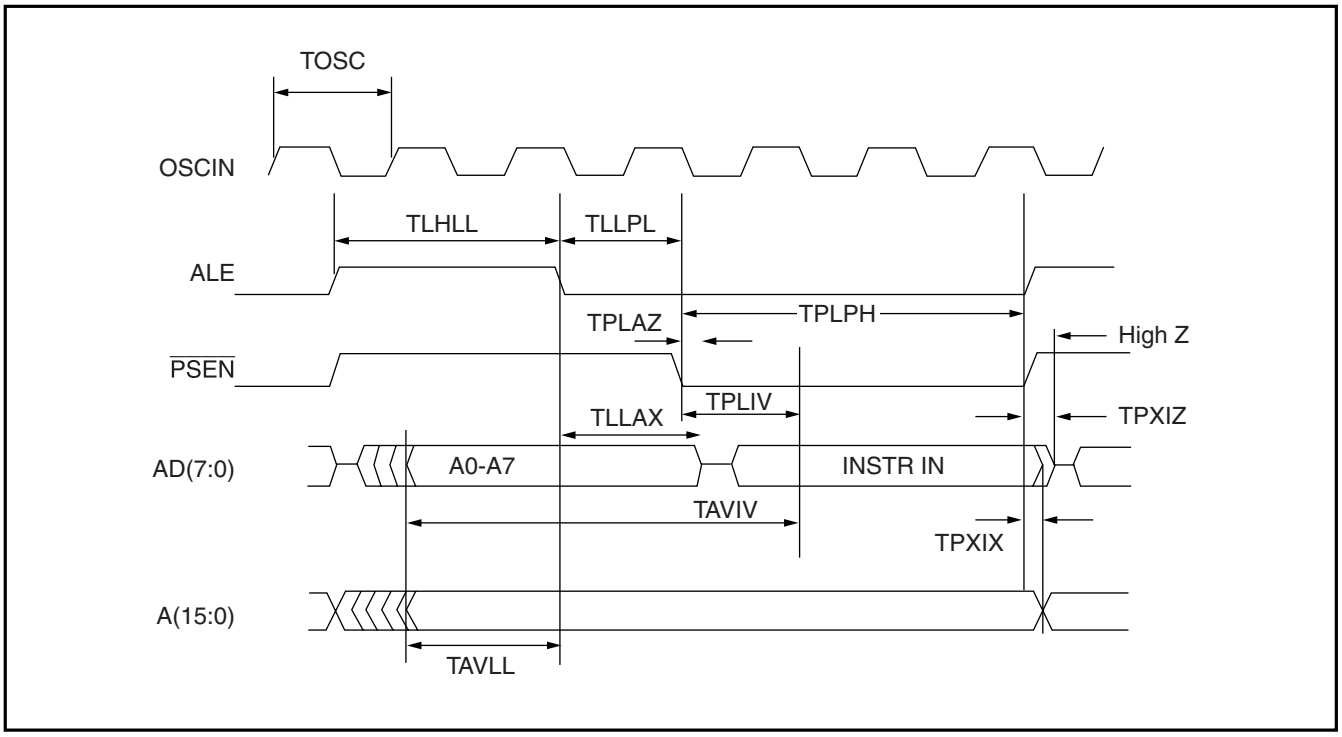


FIGURE 10: External Program Memory Read Cycle

AC TIMING (continued)

EXTERNAL DATA READ AND WRITE TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
RD Pulse Width	TRLRH		6TOSC-20			ns
WR Pulse Width	TWLWH		6TOSC-20			ns
RD Low to Valid Data In	TRLDV				5TOSC-50	ns
Data Hold After RD	TRHDX		0			ns
Data Float After RD	TRHDZ				20+	ns
ALE Low to Valid Data In	TLLDV				8TOSC-50	ns
ALE Low to RD or WR Low	TLLWL		3TOSC-20		3TOSC+20	ns
Data Valid to WR Low	TQVWX		TOSC			ns
Data Hold After WR High	TWHQX		TOSC-10			ns
RD Low to Address Float	TRLAZ				10	ns

ELECTRICAL SPECIFICATIONS (continued)

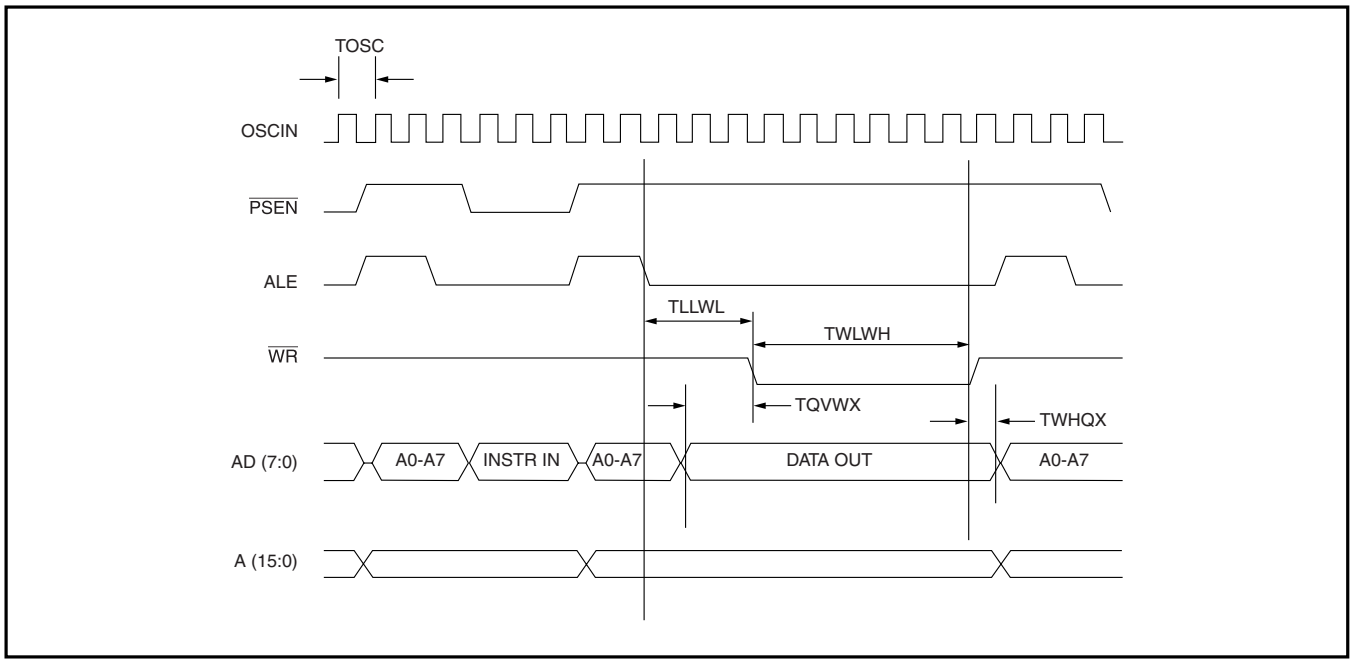


FIGURE 11: External Data Memory Write Cycle

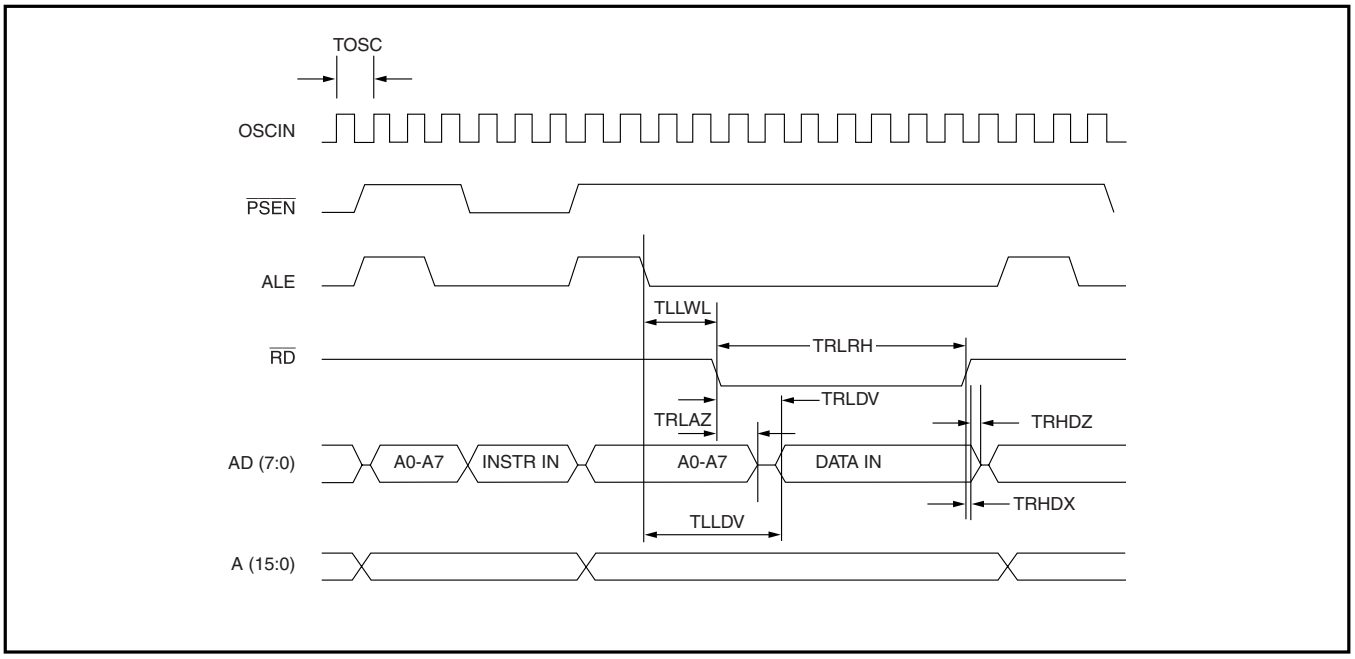
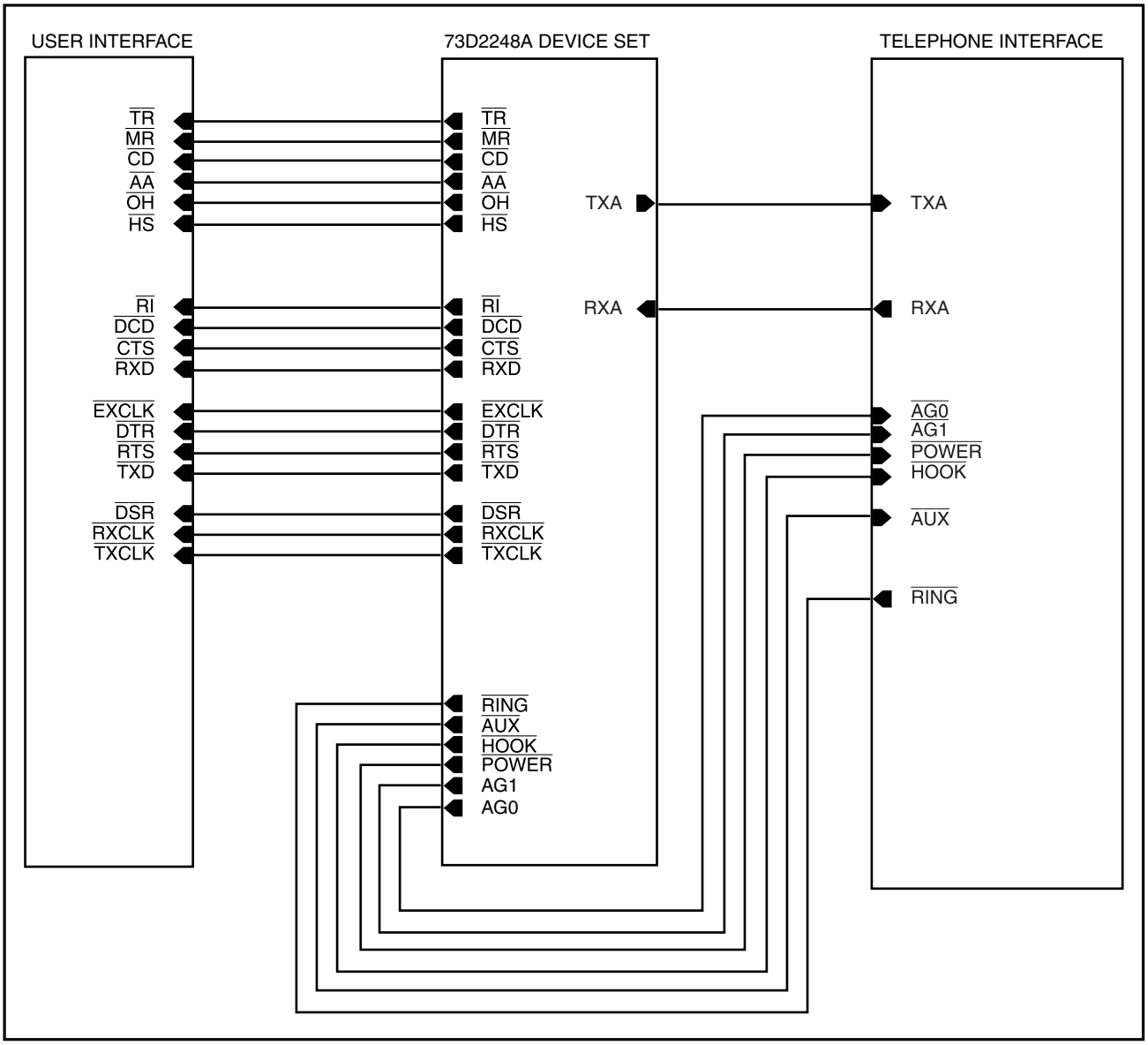


FIGURE 12: External Data Memory Read Cycle



Note: The 73D2248A Device Set is comprised of the 73M2910L and 73K224L.

FIGURE 13: Modem Block Diagram

ELECTRICAL SPECIFICATIONS (continued)

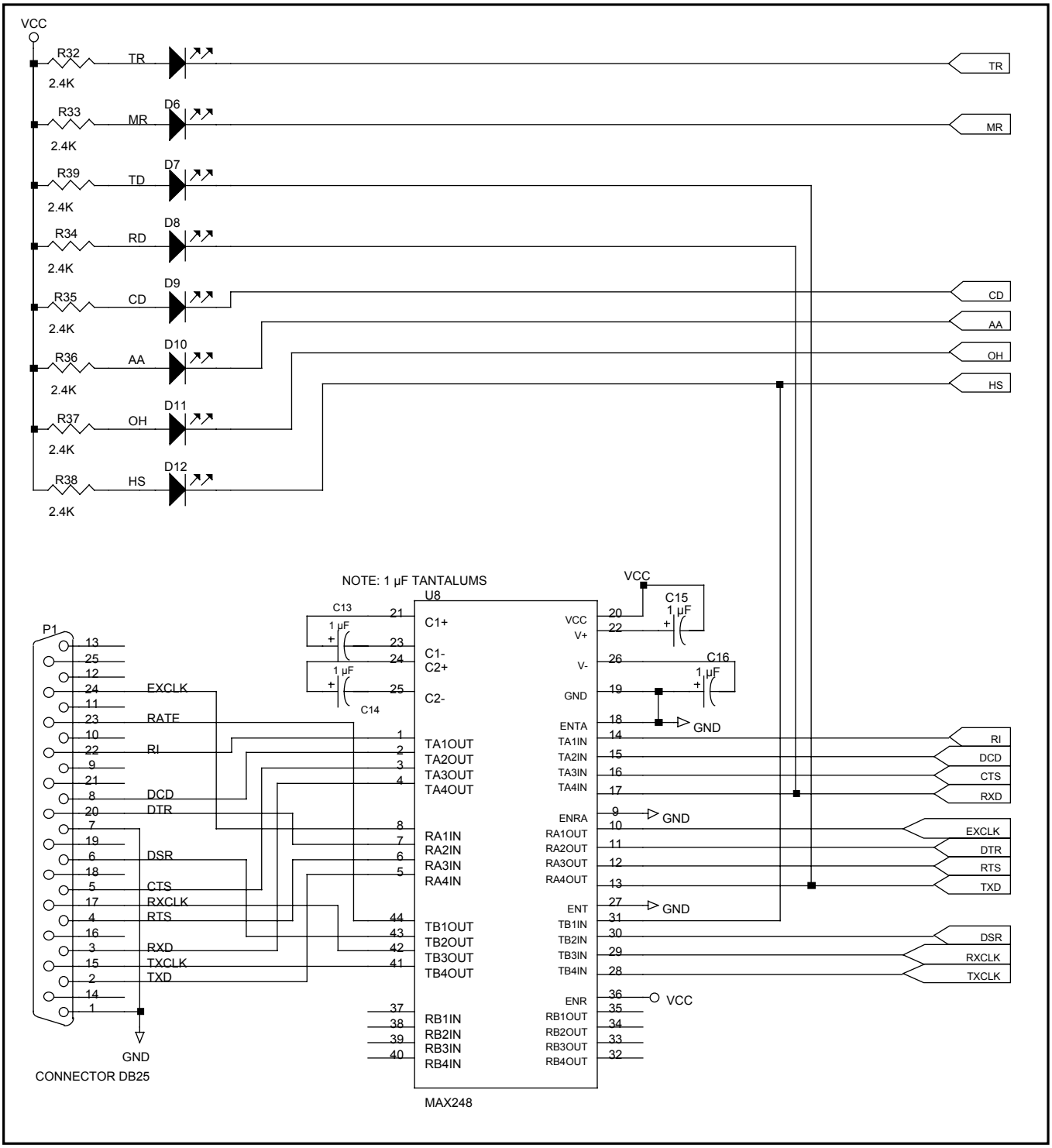


FIGURE 14: Display and User Interface

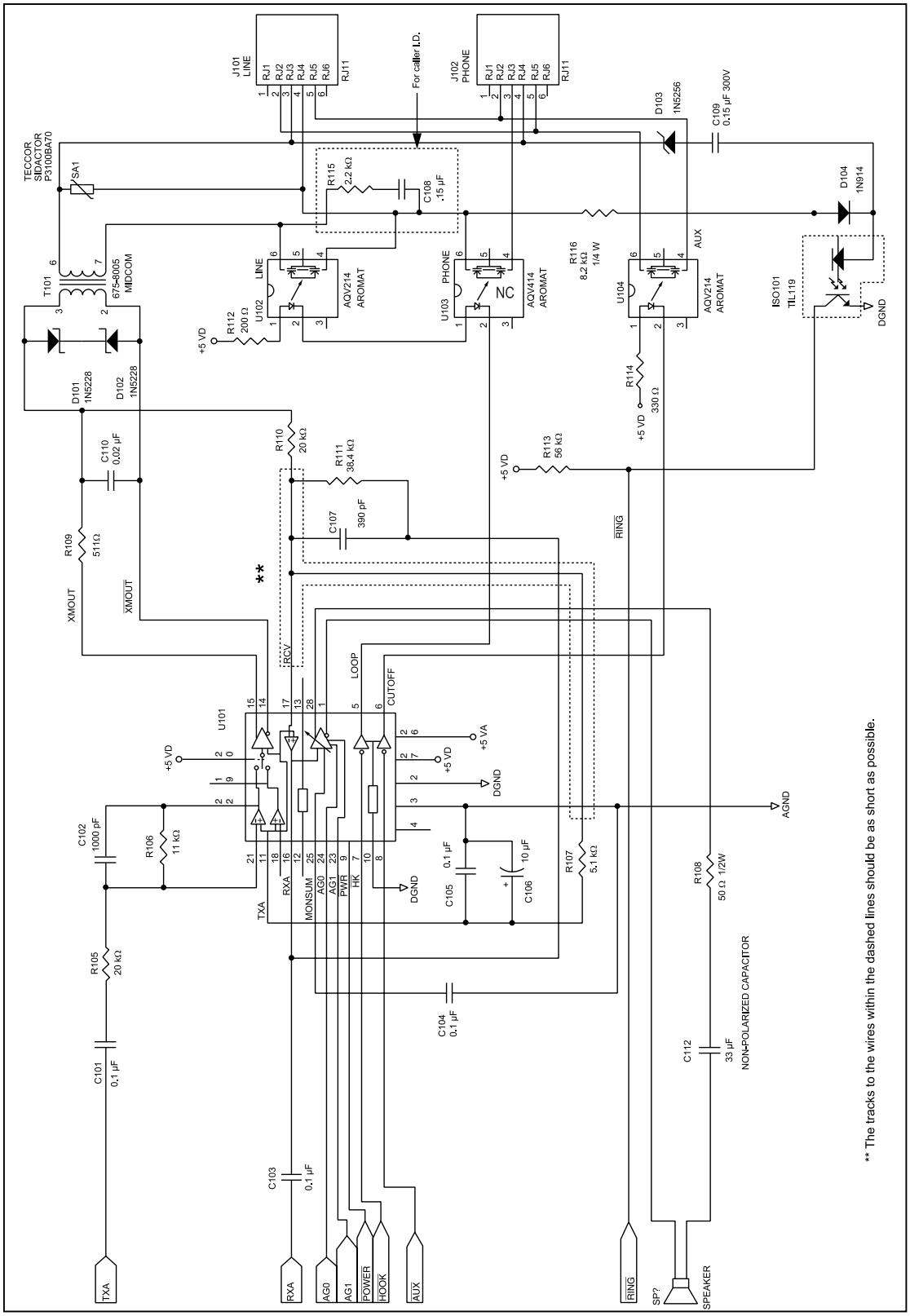


FIGURE 15: Telephone Interface

ELECTRICAL SPECIFICATIONS (continued)

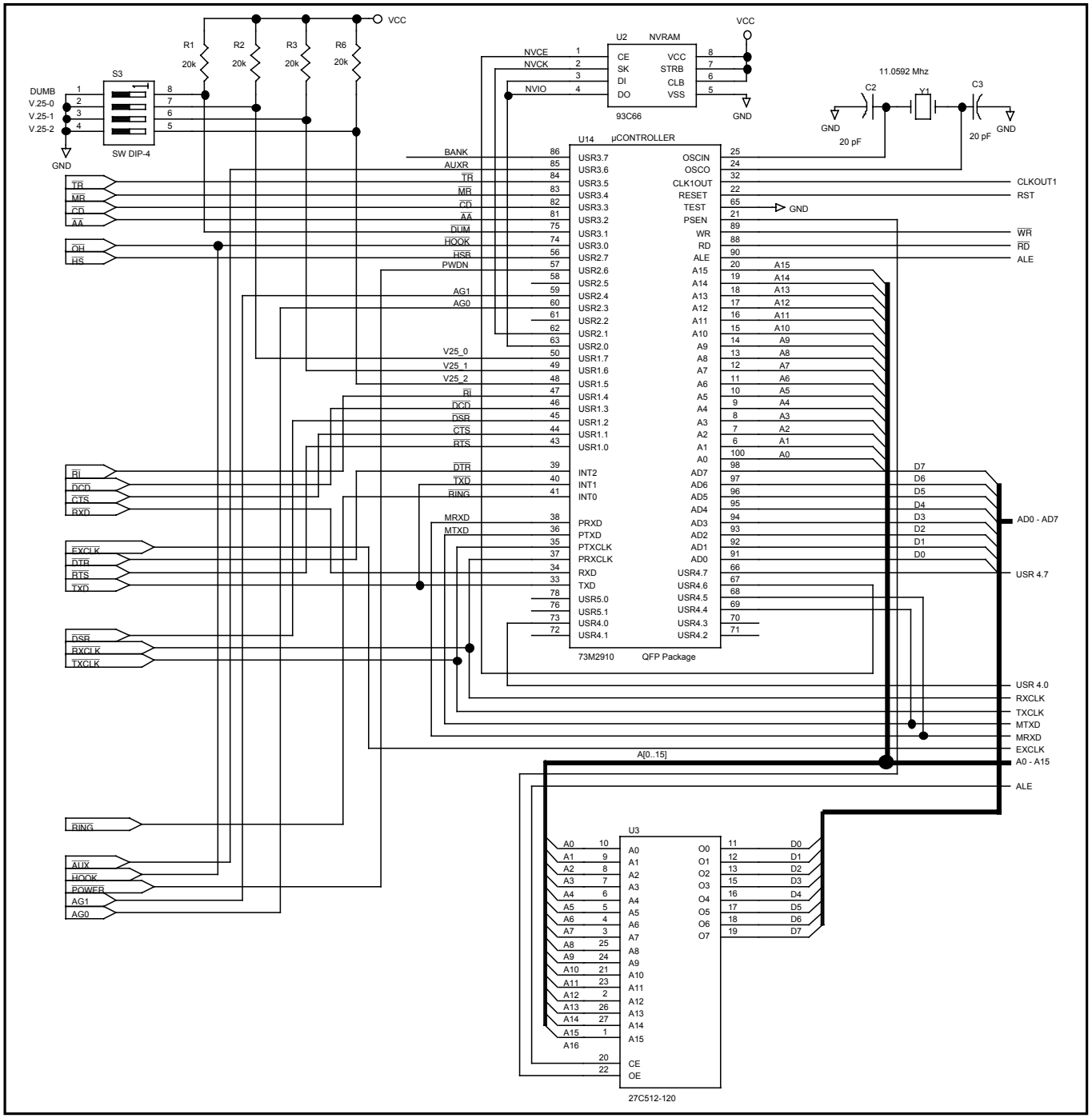


FIGURE 16A: MODEM SYSTEM INTERCONNECT - FRONT END

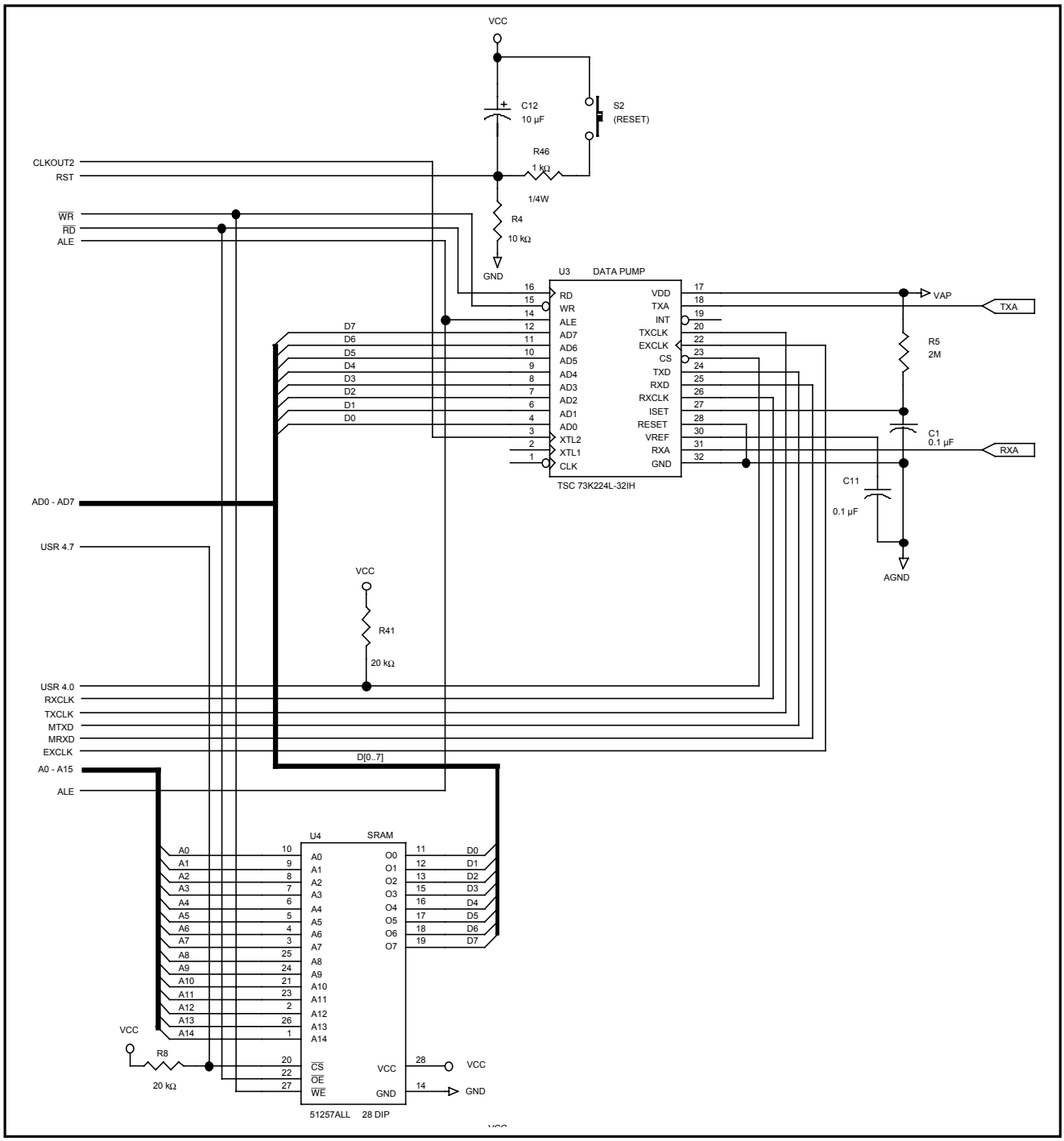


FIGURE 16B: MODEM SYSTEM INTERCONNECT - BACK END

ELECTRICAL SPECIFICATIONS (continued)

100-Pin PGA

(For development purposes only; not a production package.)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
B2	NO CONNECT	M7	$\overline{WR}$
B1	NO CONNECT	L7	ALE
C1	USR2.6	N7	D0
C2	USR2.7	N8	D1
D2	USR2.5	M8	D2
D1	USR2.4	L8	D3
E2	USR2.3	N9	D4
E1	USR2.2	M9	D5
F3	USR2.1	N10	D6
F2	USR2.0	M10	D7
F1	VPD	N11	VPD
G2	GND	N12	A0
G3	USR4.7	M11	NO CONNECT
G1	USR4.6	N13	NO CONNECT
H1	USR4.5	M12	NO CONNECT
H2	USR4.4	M13	NO CONNECT
H3	USR4.3	L12	NO CONNECT
J1	USR4.2	L13	A1
J2	USR4.1	K12	A2
K1	USR4.0	K13	A3
K2	USR3.0	J12	A4
L1	USR3.1	J13	A5
M1	USR5.1	H11	A6
L2	NO CONNECT	H12	A7
N1	NO CONNECT	H13	A8
M2	NO CONNECT	G12	A9
N2	NO CONNECT	G11	A10
M3	USR5.0	G13	A11
N3	USR3.2	F13	A12
M4	USR3.3	F12	A13
N4	USR3.4	F11	A14
M5	USR3.5	E13	A15
N5	USR3.6	E12	$\overline{PSEN}$
L6	USR3.7	D13	RESET

100-Pin PGA (continued)

(For development purposes only; not a production package.)

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
M6	GND	D12	GND
N6	RD	C13	OSCOUT
B13	OSCIN	B7	$\overline{\text{INT1}}$
C12	NO CONNECT	C7	$\overline{\text{INT0}}$
A13	NO CONNECT	A7	GND
B12	NO CONNECT	A6	USR1.0
A12	CLK2OUT	B6	USR1.1
B11	VPD	C6	USR1.2
A11	CLK1OUT	A5	USR1.3
B10	TXD	B5	USR1.4
A10	RXD	A4	USR1.5
B9	PTXCLK	B4	USR1.6
A9	PTXD	A3	USR1.7
C8	PRXCLK	A2	NO CONNECT
B8	PRXD	B3	NO CONNECT
A8	$\overline{\text{INT2}}$	A1	NO CONNECT

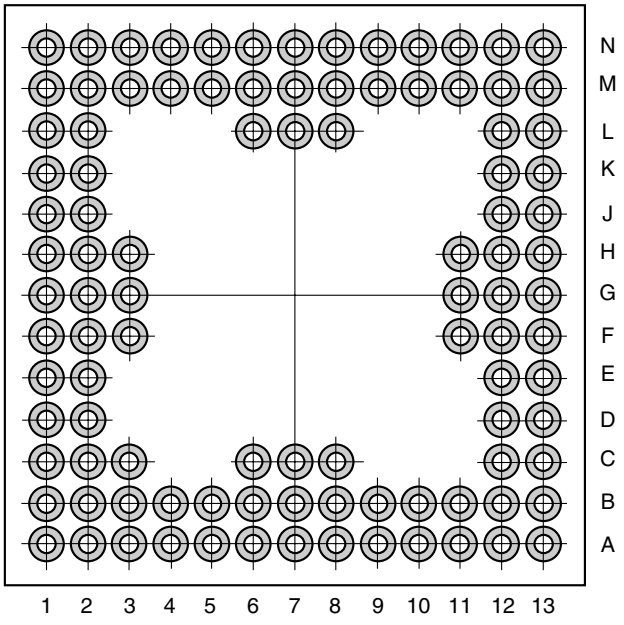
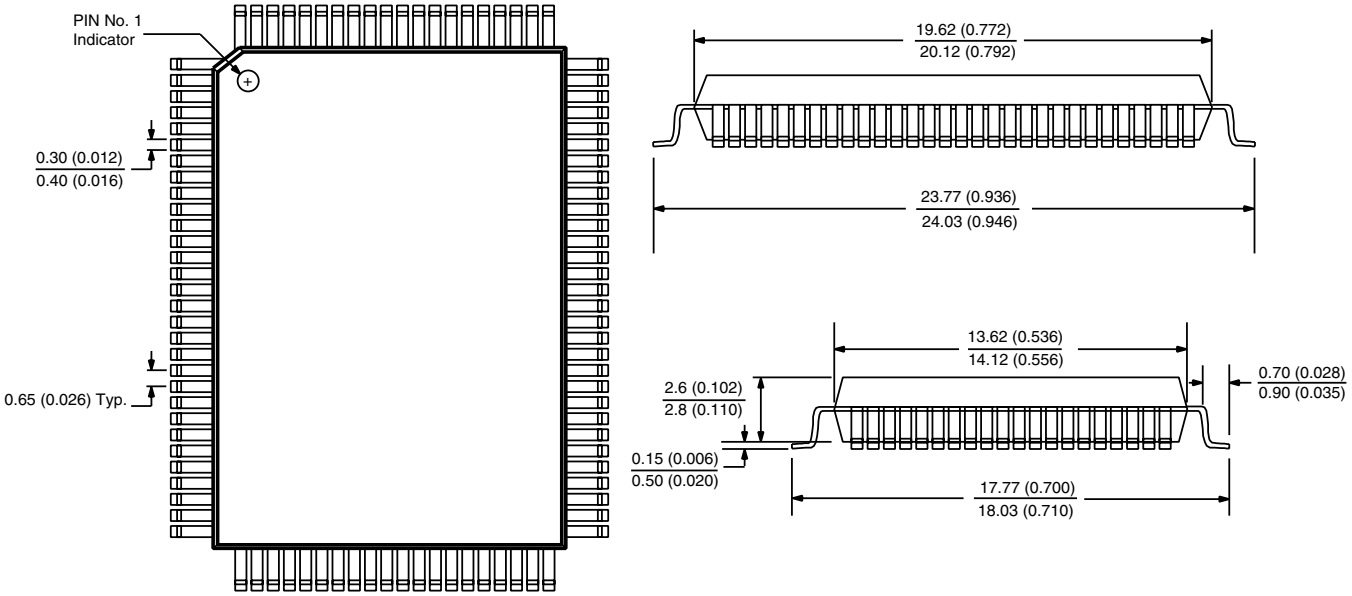


FIGURE 17: 100-Pin Grid Array (PGA) Package (Bottom View)

MECHANICAL SPECIFICATIONS

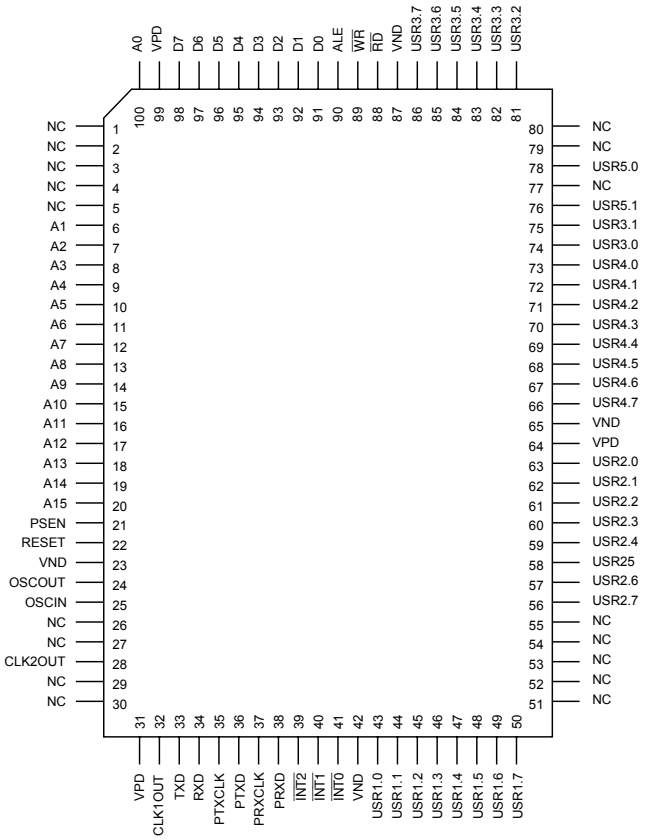
100-Lead QFP



PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-Lead QFP
73M2910L-IG

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
73M2910L 100-Lead QFP	73M2910L-IG	73M2910L-IG

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