16-BIT, 1-MSPS, PSEUDO-BIPOLAR DIFFERENTIAL SAR ADC WITH ON-CHIP ADC DRIVER (OPA) AND 4-CHANNEL DIFFERENTIAL MULTIPLEXER

FEATURES

- **1.0-MHz Sample Rate, Zero Latency at Full Speed**
- **16-Bit Resolution**
- **Supports Pseudo-Bipolar Differential Input Range: -4 V to +4 V with 2-V Common-Mode**
- **Built-In Four Channel, Differential Ended Multiplexer; with Channel Count Selection and Auto/Manual Mode**
- **On-Board Differential ADC Driver (OPA)**
- **Buffered Reference Output to Level Shift Bipolar ±4-V Input with External Resistance Divider**
- **Reference/2 Output to Set Common-Mode for External Signal Conditioner**
- **16-/8-Bit Parallel Interface**
- **SNR: 95.4dB Typ at 2-kHz I/P**
- **THD: –118dB Typ at 2-kHz I/P**
- **Power Dissipation: 331.25 mW at 1 MSPS**
- **Internal Reference**
- **Internal Reference Buffer**
- **64-Pin QFN Package**

APPLICATIONS

- **Medical Imaging/CT Scanners**
- **Automated Test Equipment**
- **High-Speed Data Acquisition Systems**
- **High-Speed Closed-Loop Systems**

DESCRIPTION

The ADS8254 is a high-performance analog system-on-chip (SoC) device with an 16-bit, 1-MSPS A/D converter, 4-V internal reference, an on-chip ADC driver (OPA), and a 4-channel differential multiplexer. The channel count of the multiplexer and auto/manual scan modes of the device are user selectable.

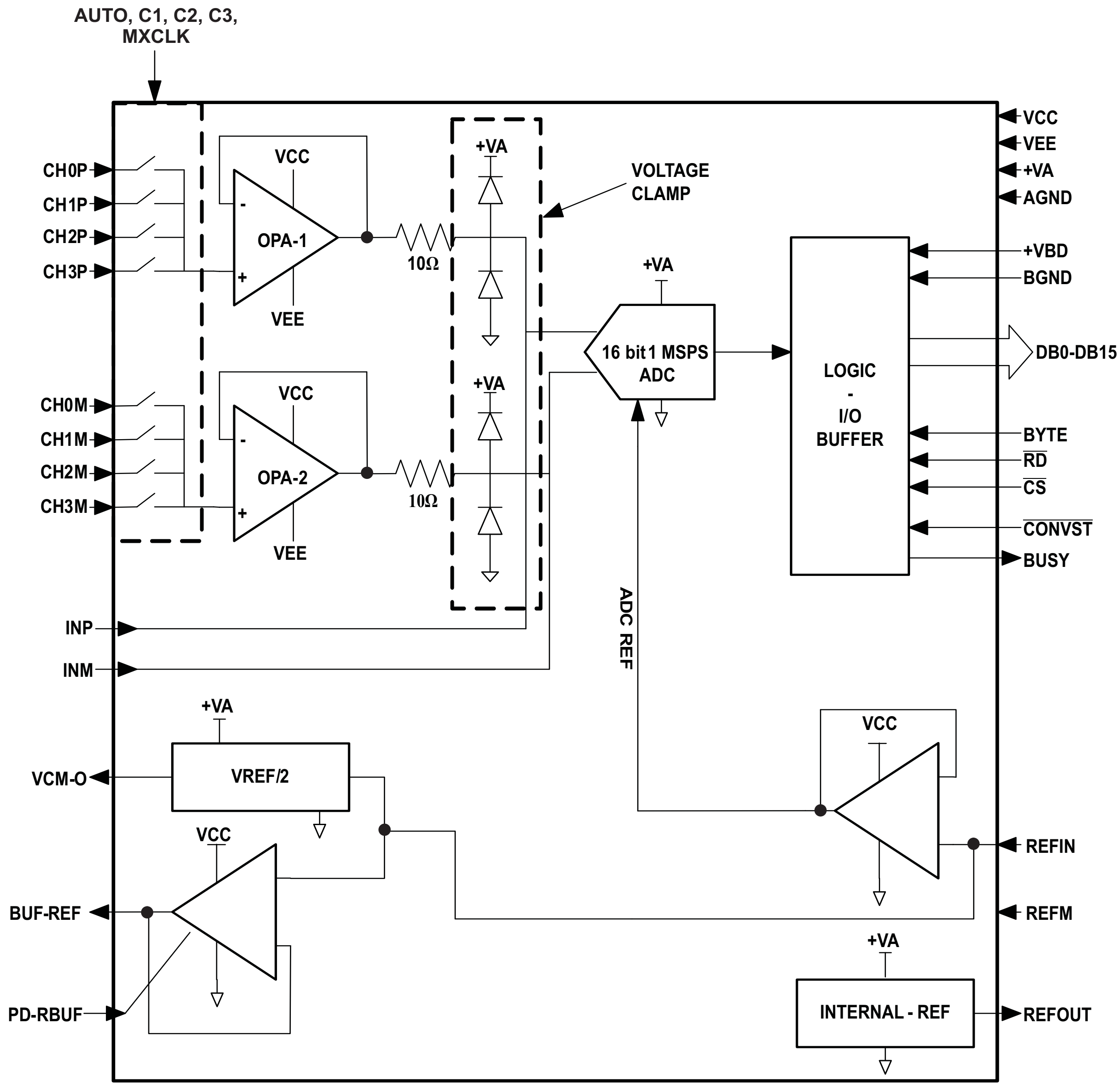
The ADC driver is designed to leverage the very high noise performance of the differential ADC at optimum power usage levels.

The ADS8254 outputs a buffered reference signal for level shifting of a ±4-V bipolar signal with an external resistance divider. A $V_{ref}/2$ output signal is available to set the common-mode of a signal conditioning circuit. The device also includes an 16-/8-bit parallel interface.

The ADS8254 is available in a 9 mm x 9 mm, 64-pin QFN package and is characterized from -40°C to 85°C.

HIGH-SPEED SAR CONVERTER FAMILY

TYPE/SPEED	500 kHz	~600 kHz	750 kHz	1 MHz	1.25 MHz	2 MHz	3 MHz	4MHz
18-Bit Pseudo-Diff	ADS8383	ADS8381		ADS8481				
		ADS8380 (s)						
18-Bit Pseudo-Bipolar, Fully Diff		ADS8382 (s)		ADS8284	ADS8484			
				ADS8482				
16-Bit Pseudo-Diff	ADS8327	ADS8370 (s)	ADS8371	ADS8471	ADS8401	ADS8411		
	ADS8328				ADS8405	ADS8410 (s)		
	ADS8319							
16-Bit Pseudo-Bipolar, Fully Diff	ADS8318	ADS8372 (s)		ADS8472	ADS8402	ADS8412		ADS8422
				ADS8254	ADS8406	ADS8413 (s)		
14-Bit Pseudo-Diff					ADS7890 (s)		ADS7891	
12-Bit Pseudo-Diff				ADS7886		ADS7883		ADS7881


AUTO, C1, C2, C3,
MXCLK
CH0P
CH1P
CH2P
CH3P
CH0M
CH1M
CH2M
CH3M
VCC
VEE
OPA-1
OPA-2
10Ω
10Ω
+VA
VOLTAGE
CLAMP
16 bit 1 MSPS
ADC
LOGIC
-
I/O
BUFFER
VCC
VEE
+VA
AGND
+VBD
BGND
DB0-DB15
BYTE
RD
CS
CONVST
BUSY
INP
INM
ADC REF
VREF/2
VCM-O
BUF-REF
PD-RBUF
REFIN
REFM
INTERNAL - REF
REFOUT

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8254IB	±0.75	±0.5	16	64-pin QFN	RGC	–40°C to 85°C	ADS8254IBRGCT	250
							ADS8254IBRGCR	2000
ADS8254I	±1.5	±0.5	16				ADS8254IRGCT	250
							ADS8254IRGCR	2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, refer to the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
CH(i) to AGND (both P and M inputs)		VEE–0.3 to VCC + 0.3	V
VCC to VEE		-0.3 to 18	V
+VA to AGND		–0.3 to 7	V
+VBD to BDGND		–0.3 to 7	V
ADC control digital input voltage to GND		–0.3 to (+VBD + 0.3)	V
ADC control digital output to GND		–0.3 to (+VBD + 0.3)	V
Multiplexer control digital input voltage to GND		–0.3 to (+VA + 0.3)	V
Power control digital input voltage to GND		–0.3 to (+VCC + 0.3)	V
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C
Junction temperature ($T_J$max)		150	°C
QFN package	Power dissipation	(T_J Max–T_A)/ θJA	
	θJA Thermal impedance	86	°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215	°C
	Infrared (15 sec)	220	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

T_A = –40°C to 85°C, VCC = 5 V, VEE =–5 V, +VA = 5 V, +VBD = 5 V or 3.3 V, V_{ref} = 4 V, f_{SAMPLE} = 1 MSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
Full-scale input voltage at multiplexer input[(1)]		CH(i)P–CH(i)M	$-V_{ref}$		V_{ref}	V
Absolute input range at multiplexer input		CH (i)	–0.2		V_{ref} + 0.2	V
Input common-mode voltage		[CH(i)P + CH(i)M] /2	$(V_{ref})/2 - 0.2$	$(V_{ref})/2$	$(V_{ref})/2 + 0.2$	V
SYSTEM PERFORMANCE						
Resolution				16		Bits
No missing codes	ADS8254IB		16			Bits
	ADS8254I		16			
Integral linearity [(2)]	ADS8254IB		–0.75	±0.4	0.75	LSB [(3)]
	ADS8254I		–1.5	±0.4	1.5	
Differential linearity	ADS8254IB	At 18-bit level	–0.5	±0.32	0.5	LSB[(3)]
	ADS8254I		–0.5	±0.32	0.5	
Offset error[(4)]	ADS8254IB		–0.5	±0.05	0.5	mV
	ADS8254I		–0.5	±0.05	0.5	
Gain error[(4)]	ADS8254IB	External reference	–0.1	±0.025	0.1	%FS
	ADS8254I		–0.1	±0.025	0.1	
DC Power supply rejection ratio		At $3FFF0_H$ output code. For +VA or VCC, VEE variation of 0.5V individually		80		dB
SAMPLING DYNAMICS						
Conversion time		+VBD = 5 V		625	650	ns
		+VDB = 3 V		625	650	ns
Acquisition time		+VBD = 5 V	320	350		ns
		+VDB = 3 V	320	350		
Maximum throughput rate					1.0	MHz
Aperture delay				4		ns
Aperture jitter				5		ps
Settling time to 0.5 LSB		For ADC only		150		ns
		For OPA (OP1, OP2)+ Mux		700		
Over voltage recovery		For ADC only		150		ns
DYNAMIC CHARACTERISTICS						
Total harmonic distortion (THD)[(4)]	ADS8254I	V_{IN} = 4 V_{pp} at 2 kHz		–118		dB
	ADS8254IB			–118		
	ADS8254I	V_{IN} = 4 V_{pp} at 10 kHz		–105		dB
	ADS8254IB			–105		
	ADS8254I	V_{IN} = 4 V_{pp} at 100 kHz, LoPWR = 0		–100		dB
	ADS8254IB			–100		
Signal to noise ratio (SNR)	ADS8254I	V_{IN} = 4 V_{pp} at 2 kHz		95.4		dB
	ADS8254IB		94	95.4		
	ADS8254I	V_{IN} = 4 V_{pp} at 10 kHz		95		dB
	ADS8254IB			95		
	ADS8254I	V_{IN} = 4 V_{pp} at 100 kHz, LoPWR = 0		93		dB
	ADS8254IB			94.5		

(1) Ideal input span, does not include gain or offset error.
(2) Measured relative to acutal measured referenceThis is endpoint INL, not best fit.
(3) LSB means least significant bit
(4) Calculated on the first nine harmonics of the input frequency.

SPECIFICATIONS (continued)

T_A = –40°C to 85°C, VCC = 5 V, VEE =–5 V, +VA = 5 V, +VBD = 5 V or 3.3 V, V_{ref} = 4 V, f_{SAMPLE} = 1 MSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal to noise + distortion (SINAD)	ADS8254I	V_{IN} = 4 V_{pp} at 2 kHz		95.2		dB
	ADS8254IB			95.2		
	ADS8254I	V_{IN} = 4 V_{pp} at 10 kHz		94.5		dB
	ADS8254IB			94.5		
	ADS8254I	V_{IN} = 4 V_{pp} at 100 kHz, LoPWR = 0		92.2		dB
	ADS8254IB			93.4		
Spurious free dynamic range (SFDR)	ADS8254I	V_{IN} = 4 V_{pp} at 2 kHz		120		dB
	ADS8254IB			120		
	ADS8254I	V_{IN} = 4 V_{pp} at 10 kHz		106		dB
	ADS8254IB			106		
	ADS8254I	V_{IN} = 4 V_{pp} at 100 kHz, LoPWR = 0		101		dB
	ADS8254IB			101		
–3dB Small signal bandwidth				8		MHz
VOLTAGE REFERENCE INPUT (REFIN)						
Reference voltage at REFIN, V_{ref}			3.0	4.096	+VA – 0.8	V
Reference input current(5)				1	1	μA
INTERNAL REFERENCE OUTPUT (REFOUT)						
Internal reference start-up time		From 95% (+VA), with 1-μF storage capacitor			120	ms
Reference voltage range, V_{ref}			4.081	4.096	4.111	V
Source current		Static load			10	μA
Line regulation		+VA = 4.75 V ~ 5.25 V		60		μV
Drift		I_O = 0		±6		PPM/°C
BUFFERED REFERENCE OUTPUT (BUF-REF)						
Output current		REFIN = 4V, at 85°C		70		mA
REFERENCE/2 OUTPUT (VCMO)						
Output current		REFIN = 4V, at +85°C		50		μA
ANALOG MULTIPLEXER						
Number of channels					8	
Channel to channel crosstalk		100 kHz i/p		–95		dB
Channel selection		Auto sequencer with selection of channel count OR Manual selection through control lines				
DIGITAL INPUT-OUTPUT						
ADC CONTROL PINS						
Logic Family-CMOS						
Logic level	V_{IH}	I_{IH} = 5 μA	$+V_{BD}$–1		$+V_{BD}$ + 0.3	V
	V_{IL}	I_{IL} = 5 μA	0.3		0.8	V
	V_{OH}	I_{OH} = 2 TTL loads	$+V_{BD}$–6		$+V_{BD}$	V
	V_{OL}	I_{OL} = 2 TTL loads	0		0.4	V
MULTIPLEXER CONTROL PINS						
Logic Family - CMOS						
Logic Level	I_{IH}	I_{IH} = 5 μA	2.3		+VA +0.3	V
	I_{IL}	I_{IL} = 5 μA	–0.3		0.8	V
POWER CONTROL PINS						
Logic Family - CMOS						
Logic Level	V_{IH}	I_{IH} = 5 μA	2.3		+VA +0.3	V
	V_{IL}	I_{IL} = 5 μA	–0.3		0.8	V

(5) Can vary ±20%

SPECIFICATIONS (continued)

T_A = –40°C to 85°C, VCC = 5 V, VEE =–5 V, +VA = 5 V, +VBD = 5 V or 3.3 V, V_{ref} = 4 V, f_{SAMPLE} = 1 MSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY REQUIREMENTS						
Power supply voltage	+VBD		2.7	3.3	5.25	V
	+VA		4.75	5	5.25	V
	VCC		4.75	5	7.5	V
	VEE		–7.5	–5	–3	V
ADC driver positive supply (VCC) current (for OP1 and OP2 together)		VCC = +5, VEE = -5V, CH0 - CH3 p and m inputs shorted to each other and connected to 2V		11.65		mA
ADC driver negative supply (VEE) current (for OP1 and OP2 together)		VCC = +5, CH0 - CH3 p and m inputs shorted to each other and connected to 2V		9.6		mA
+VA Supply Current, 1MHz Sample Rate				45	50	mA
Reference buffer (BUF-REF) supply current (VCC to GND)		VCC= +5, PD-RBUF = 0, Quiescent current		8		mA
		VCC = 5, PD-RBUF = 1 [6]		10		µA
TEMPERATURE RANGE						
Operating free air			–40		85	°C

(6) PD-RBUF=1 powers down the Reference buffer (BUF-REF), note that it does not 3-state the BUF-REF output.

TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C, +VA =+VBD = 5 V (1) (2) (3)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(CONV)}$	Conversion time			650	ns
$t_{(ACQ)}$	Acquisition time	320			ns
$t_{(HOLD)}$	Sample capacitor hold time			25	ns
t_{pd1}	$\overline{\text{CONVST}}$ low to BUSY high			40	ns
t_{pd2}	Propagation delay time, end of conversion to BUSY low			15	ns
t_{pd3}	Propagation delay time, start of convert state to rising edge of BUSY			15	ns
t_{w1}	Pulse duration, $\overline{\text{CONVST}}$ low	40			ns
t_{su1}	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	20			ns
t_{w2}	Pulse duration, $\overline{\text{CONVST}}$ high	20			ns
	$\overline{\text{CONVST}}$ falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	$t_{(ACQ)}$min			ns
t_{w4}	Pulse duration, BUSY signal high			650	ns
t_{h1}	Hold time, first data bus transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE or BUS18/$\overline{16}$ input changes) after $\overline{\text{CONVST}}$ low	40			ns
t_{d1}	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low	0			ns
t_{su2}	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t_{w5}	Pulse duration, $\overline{\text{RD}}$ low	50			ns
t_{en}	Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid			20	ns
t_{d2}	Delay time, data hold from $\overline{\text{RD}}$ high	5			ns
t_{d3}	Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid	10		20	ns
t_{w6}	Pulse duration, $\overline{\text{RD}}$ high	20			ns
t_{w7}	Pulse duration, $\overline{\text{CS}}$ high	20			ns
t_{h2}	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	50			ns
t_{pd4}	Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge	0			ns
t_{d4}	Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew	0			ns
t_{su3}	Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{\text{RD}}$ falling edge	10			ns
t_{h3}	Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{\text{RD}}$ falling edge	10			ns
t_{dis}	Disable time, $\overline{\text{RD}}$ high ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus			20	ns
t_{d5}	Delay time, BUSY low to MSB data valid delay			0	ns
t_{d6}	Delay time, $\overline{\text{CS}}$ rising edge to BUSY falling edge	50			ns
t_{d7}	Delay time, BUSY falling edge to $\overline{\text{CS}}$ rising edge	50			ns
t_{su5}	BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition setup time, from BUS18/$\overline{16}$ to next BUS18/$\overline{16}$.	50			ns
$t_{su(ABORT)}$	Setup time from the falling edge of $\overline{\text{CONVST}}$ (used to start the valid conversion) to the next falling edge of $\overline{\text{CONVST}}$ (when CS = 0 and $\overline{\text{CONVST}}$ are used to abort) or to the next falling edge of $\overline{\text{CS}}$ (when $\overline{\text{CS}}$ is used to abort).	60		550	ns

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C, +VA = 5 V +VBD = 3 V (1) (2) (3)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(CONV)}$	Conversion time			650	ns
$t_{(ACQ)}$	Acquisition time	310			ns
$t_{(HOLD)}$	Sample capacitor hold time			25	ns
t_{pd1}	CONVST low to BUSY high			40	ns
t_{pd2}	Propagation delay time, end of conversion to BUSY low			25	ns
t_{pd3}	Propagation delay time, start of convert state to rising edge of BUSY			25	ns
t_{w1}	Pulse duration, CONVST low	40			ns
t_{su1}	Setup time, CS low to CONVST low	20			ns
t_{w2}	Pulse duration, CONVST high	20			ns
	CONVST falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	$t_{(ACQ)}$min			ns
t_{w4}	Pulse duration, BUSY signal high			650	ns
t_{h1}	Hold time, first data bus transition (RD low, or CS low for read cycle, or BYTE or BUS18/16 input changes) after CONVST low	40			ns
t_{d1}	Delay time, CS low to RD low	0			ns
t_{su2}	Setup time, RD high to CS high	0			ns
t_{w5}	Pulse duration, RD low	50			ns
t_{en}	Enable time, RD low (or CS low for read cycle) to data valid			30	ns
t_{d2}	Delay time, data hold from RD high	5			ns
t_{d3}	Delay time, BUS18/16 or BYTE rising edge or falling edge to data valid	10		30	ns
t_{w6}	Pulse duration, RD high	20			ns
t_{w7}	Pulse duration, CS high	20			ns
t_{h2}	Hold time, last RD (or CS for read cycle) rising edge to CONVST falling edge	50			ns
t_{pd4}	Propagation delay time, BUSY falling edge to next RD (or CS for read cycle) falling edge	0			ns
t_{d4}	Delay time, BYTE edge to BUS18/16 edge skew	0			ns
t_{su3}	Setup time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t_{h3}	Hold time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t_{dis}	Disable time, RD high (CS high for read cycle) to 3-stated data bus			30	ns
t_{d5}	Delay time, BUSY low to MSB data valid delay			0	ns
t_{d6}	Delay time, CS rising edge to BUSY falling edge	50			ns
t_{d7}	Delay time, BUSY falling edge to CS rising edge	50			ns
t_{su5}	BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/16 transition setup time, from BUS18/16 to next BUS18/16.	50			ns
$t_{su(ABORT)}$	Setup time from the falling edge of CONVST (used to start the valid conversion) to the next falling edge of CONVST (when CS = 0 and CONVST are used to abort) or to the next falling edge of CS (when CS is used to abort).	70		550	ns

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

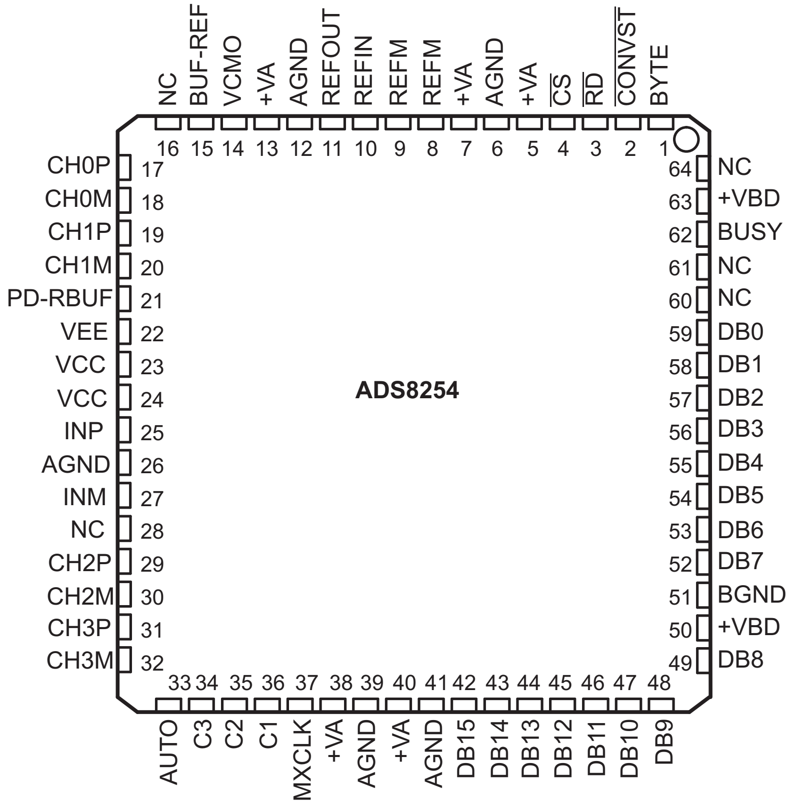
MULTIPLEXER TIMING REQUIREMENTS

VCC = 4.75 V to 7.5 V, VEE = -3 V to -7.5 V

		MIN	TYP	MAX	UNIT
t_{su6}	Setup time C1, C2 or C3 to MXCLK rising edge			600	ns
t_{d8}	Multiplexer and driver settle time (from MXCLK rising edge to CONVST falling edge)	600			ns

PIN ASSIGNMENTS

QFN PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO	NAME		
MULTIPLEXER INPUT PINS			
17	CH0P	I	Non-inverting analog input for differential multiplexer channel number 0. Device performance is optimized for 50 ohm source impedance at this input.
18	CH0M	I	Inverting analog input for differential multiplexer channel number 0. Device performance is optimized for 50 ohm source impedance at this input.
19	CH1P	I	Non-inverting analog input for differential multiplexer channel number 1. Device performance is optimized for 50 ohm source impedance at this input.
20	CH1M	I	Inverting analog input for differential multiplexer channel number 1. Device performance is optimized for 50 ohm source impedance at this input.
29	CH2P	I	Non-inverting analog input for differential multiplexer channel number 2. Device performance is optimized for 50 ohm source impedance at this input.
30	CH2M	I	Inverting analog input for differential multiplexer channel number 2. Device performance is optimized for 50 ohm source impedance at this input.
31	CH3P	I	Non-inverting analog input for differential multiplexer channel number 3. Device performance is optimized for 50 ohm source impedance at this input.
32	CH3M	I	Inverting analog input for differential multiplexer channel number 3. Device performance is optimized for 50 ohm source impedance at this input.
ADC INPUT PINS			
25	INP	I	ADC Non inverting input., connect 1nF cap across INP and INM
27	INM	I	ADC Inverting input, connect 1nF cap across INP and INM
REFERENCE INPUT/ OUTPUT PINS			
8, 9	REFM	I	Reference ground.
10	REFIN	I	Reference Input. Add 0.1-µF decoupling capacitor between REFIN and REFM.
11	REFOUT	O	Reference Output. Add 1-µF capacitor between the REFOUT pin and REFM pin when internal reference is used.

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION		
NO	NAME				
14	VCMO	O	This pin outputs Refin/2 and can be used to set common-mode voltage of differential analog inputs.		
15	BUF-REF	O	Buffered reference output. Useful to level shift bipolar signals using external resistors.		
POWER CONTROL PINS					
21	PD-RBUF	I	High on this pin powers down the reference buffer (BUF-REF).		
MULTIPLEXER CONTROL PINS					
33	AUTO	I	High level on this pin selects ‘Auto’ mode for multiplexer scanning. Low level selects manual mode of multiplexer scanning		
34	C3	I	In auto mode (AUTO=1) multiplexer channel selection is reset to CH0 on rising edge of MXCLK while C3=1. The pin is 'do not care' in manual mode.		
35	C2	I	Acts as multiplexer address bit when AUTO=0 (Manual mode). In auto mode (AUTO=1) C2 and C1 select the last multiplexer channel (channel count) in the auto scan sequence.		
36	C1	I	Acts as multiplexer address LSB when AUTO=0 (Manual mode). In auto mode (AUTO=1) C2 and C1 select the last multiplexer channel (channel count) in the auto scan sequence.		
37	MXCLK	I	Multiplexer channel is selected on rising edge of MXCLK irrespective of whether it is auto or manual mode. Device BUSY output can be connected to MXCLK so that device selects next channel at the end of every sample.		
ADC DATA BUS					
42-49, 52-59	Data Bus		8-BIT BUS		16-BIT BUS
			BYTE = 0	BYTE = 1	BYTE = 0
42	DB15	O	D15 (MSB)	D7	D15(MSB)
43	DB14	O	D14	D6	D14
44	DB13	O	D13	D5	D13
45	DB12	O	D12	D4	D12
46	DB11	O	D11	D3	D11
47	DB10	O	D10	D2	D10
48	DB9	O	D9	D1	D9
49	DB8	O	D8	D0	D8
52	DB7	O	D7	All ones	D7
53	DB6	O	D6	All ones	D6
54	DB5	O	D5	All ones	D5
55	DB4	O	D4	All ones	D4
56	DB3	O	D3	All ones	D3
57	DB2	O	D2	All ones	D2
58	DB1	O	D1	All ones	D1
59	DB0	O	D0 (LSB)	All ones	D0 (LSB)
ADC CONTROL PINS					
62	BUSY	O	Status output. This pin is held high when device is converting.		
1	BYTE	I	Byte Select Input. Used for 8-bit bus reading. Refer to the ADC DATA BUS description above.		
2	$\overline{\text{CONVST}}$	I	Convert start. This input is active low and can act independent of the CS\ input.		
3	$\overline{\text{RD}}$	I	Synchronization pulse for the parallel output.		
4	$\overline{\text{CS}}$	I	Chip Select.		
DEVICE POWER SUPPLIES					
22	VEE		Negative supply for OPA (OP1, OP2)		
23, 24	VCC		Positive supply for OPA (OP1, OP2, BUF-REF)		
5, 7, 13, 38, 40	+VA		Analog power supply.		
6, 12, 26, 39, 41	AGND		Analog ground.		
50, 63	+VBD		Digital Power Supply For ADC Bus.		
51	BGND		Digital ground for ADC bus interface digital supply.		
NOT CONNECTED PINS					
16, 28, 60, 61, 64	NC		No connection.		

DEVICE OPERATION AND TIMING DIAGRAMS

The ADS8254 is analog system-on-chip (SoC) device. The device includes a multiplexer, a single-ended input/differential output ADC driver and differential input high-performance ADC, an additional internal reference, a buffered reference output, and a REF/2 output.

Figure 1 shows the basic operation of the device (including all elements). Subsequent sections describe the detailed timings of the individual blocks of the device (primarily the multiplexer and ADC).

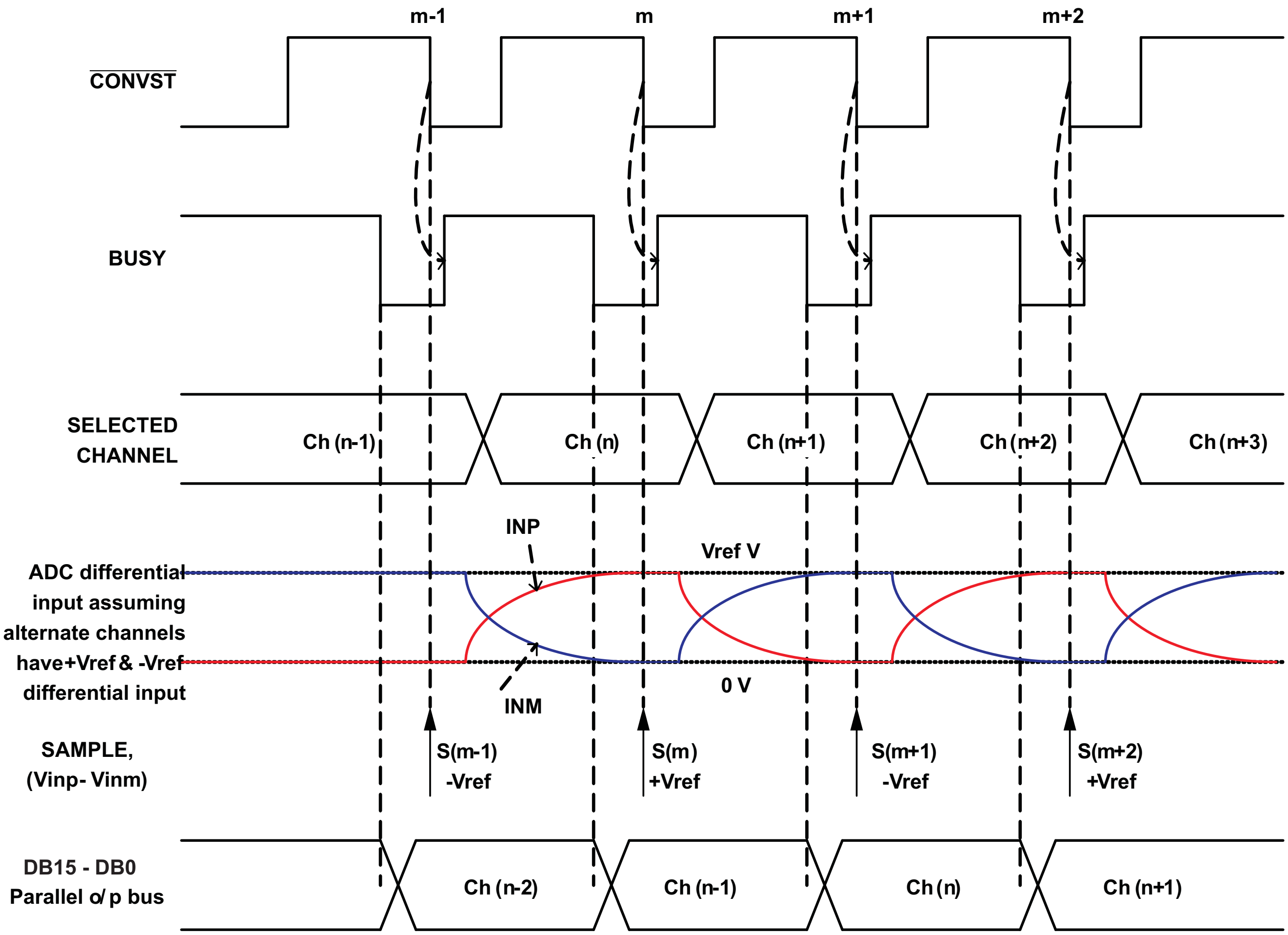
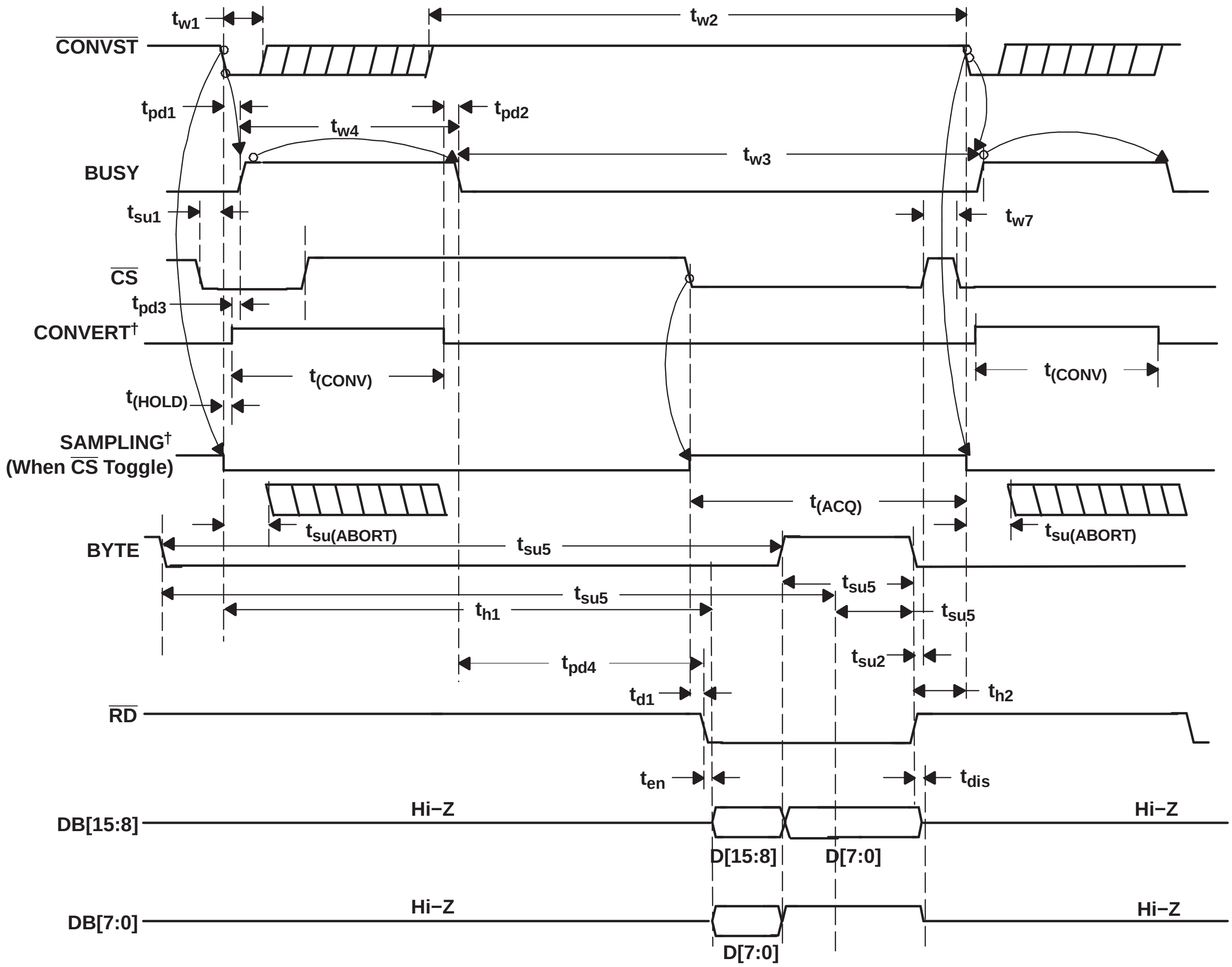


Figure 1. Device Operation

As shown in the diagram, the device can be controlled with only one ($\overline{CONVST}$) digital input. On the falling edge of $\overline{CONVST}$, the BUSY output of the device goes high. A high level on BUSY indicates the device has sampled the signal and it is converting the sample into its digital equivalent. After the conversion is complete, the BUSY output falls to a logic low level and the device output data corresponding to the recently converted sample is available for reading.

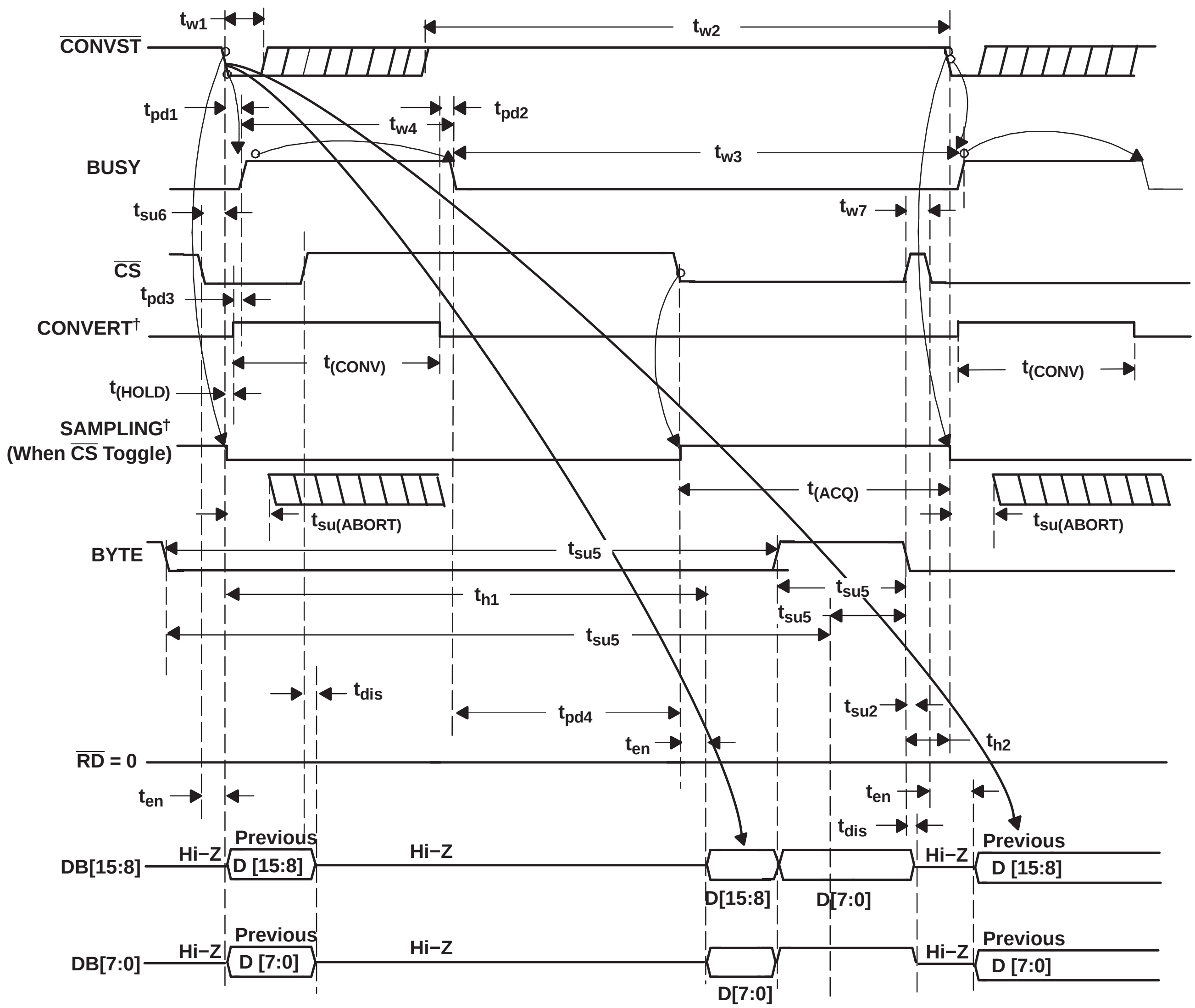
It is recommended (not mandatory) to short the BUSY output of the device to the MXCLK input. The device selects a new channel at every rising edge of MXCLK. The multiplexer is differential. The multiplexer and ADC driver are designed to settle to the 18-bit level before sampling; even at the maximum conversion speed.

ADC Control and Timing: The timing diagrams in the this section describe ADC operation; multiplexer operation is described in a the following sections.



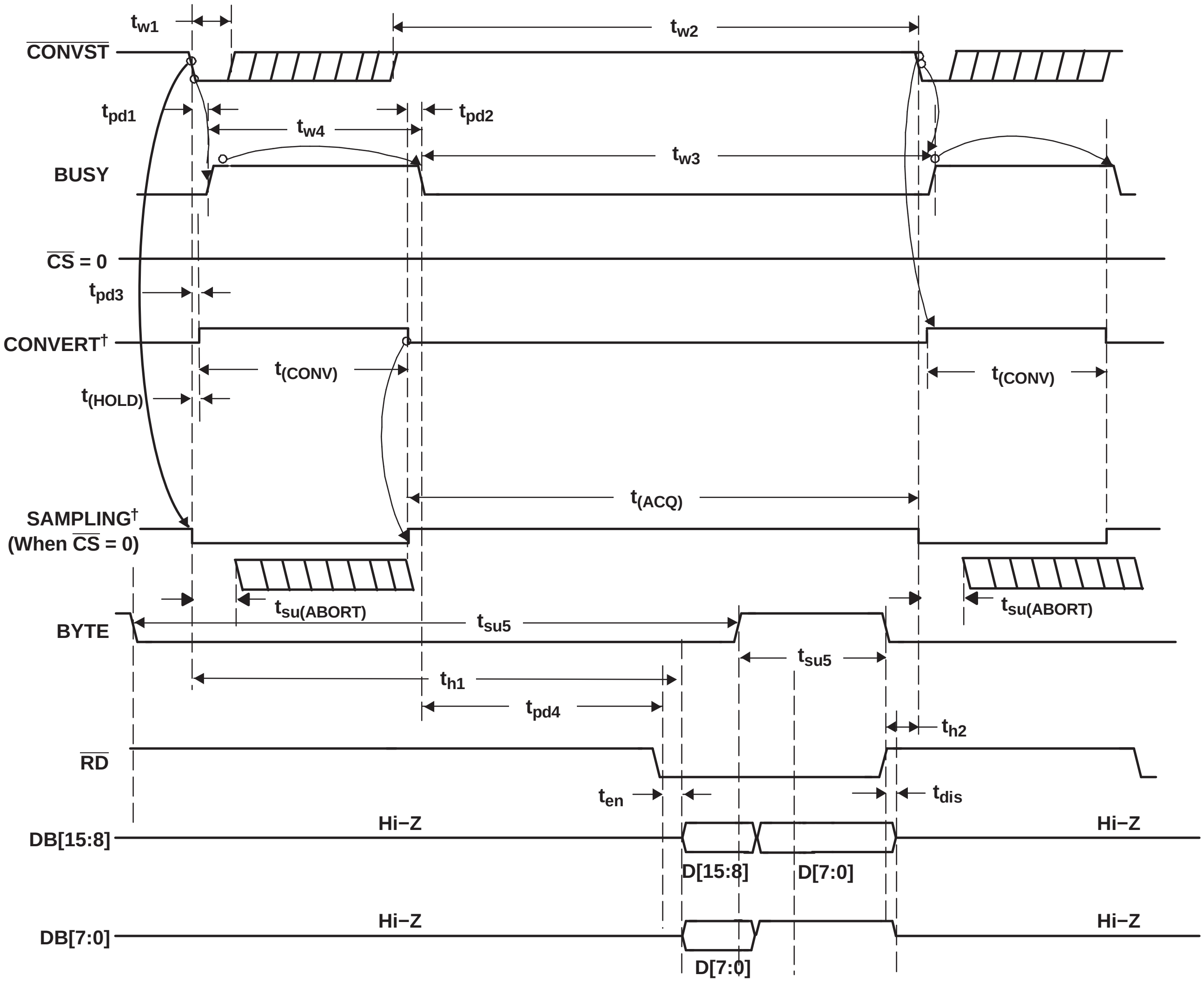
†Signal internal to device

Figure 2. Timing for Conversion and Acquisition Cycles With CS and RD Toggling



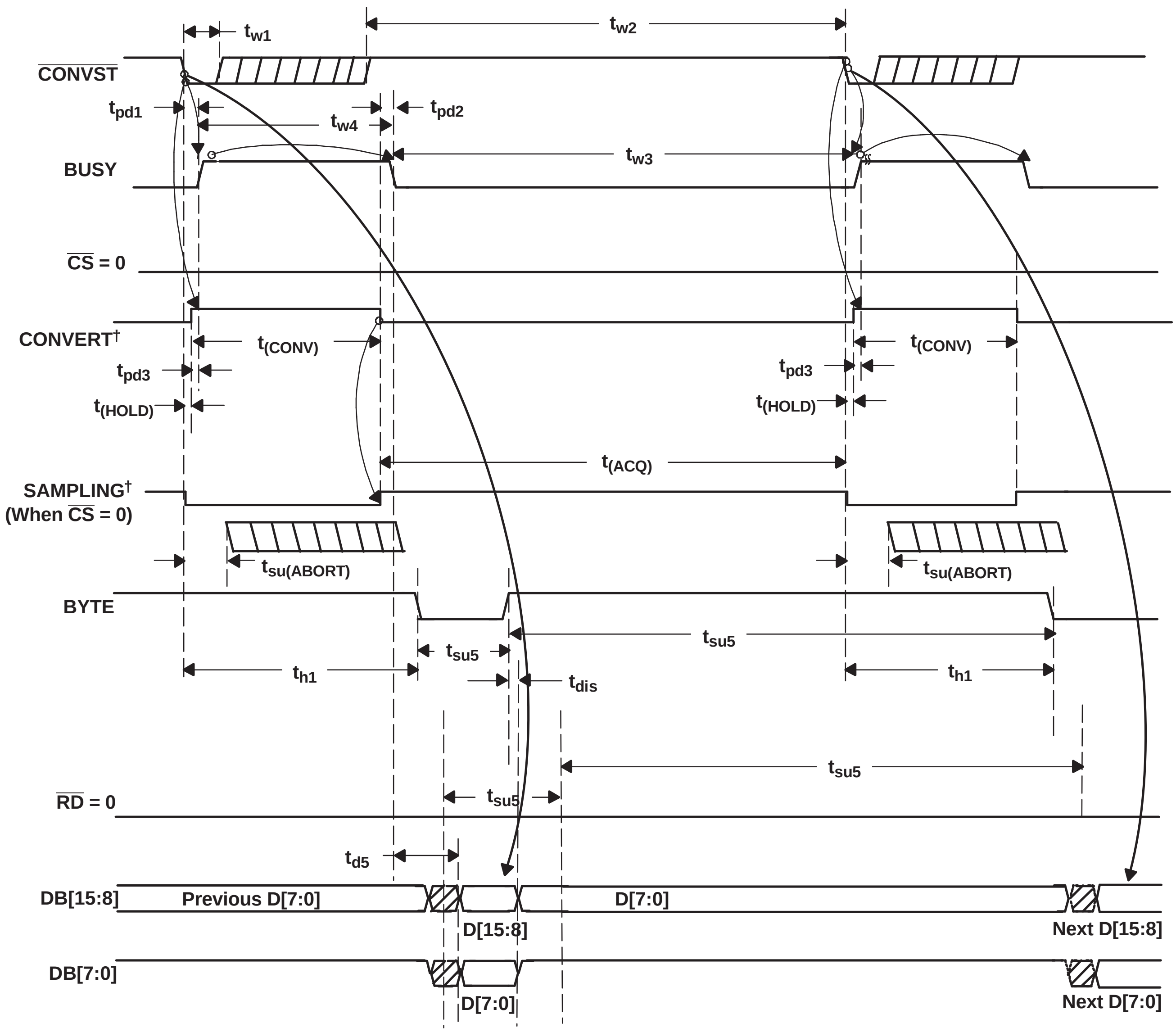
†Signal internal to device

Figure 3. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Toggling, $\overline{RD}$ Tied to BDGND



†Signal internal to device

Figure 4. Timing for Conversion and Acquisition Cycles With CS Tied to BDGND, RD Toggling



†Signal internal to device

Figure 5. Timing for Conversion and Acquisition Cycles With CS and RD Tied to BDGND - Auto Read

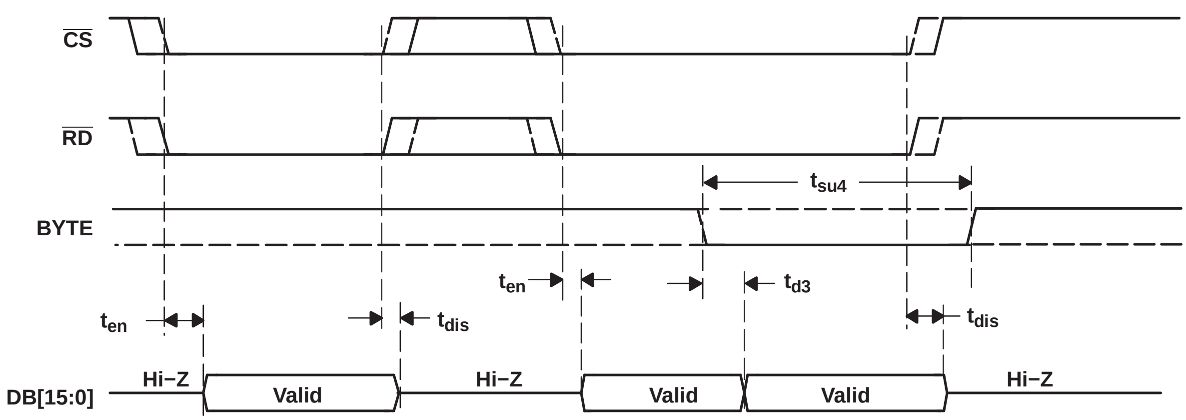


Figure 6. Detailed Timing for Read Cycles

Multiplexer: The multiplexer has two modes of sequencing namely auto sequencing and manual sequencing. Multiplexer mode selection and operation is controlled with the AUTO, C1, C2, C3, and MXCLK pins.

Auto Sequencing: A logic one level on the AUTO pin selects auto sequencing mode. It is possible to select the number of channels to be scanned (always starting from channel zero) in auto sequencing mode. Pins C1 and C2 select the channel count (last channel in the auto sequence).

On every rising edge of MXCLK while C3 is at the logic zero level, the next higher channel (in ascending order) is selected. Channel selection rolls over to channel zero on the rising edge of MXCLK after channel selection reaches the *channel count* (last channel in the auto sequence selected by pins C1and C2).

Any time during the sequence the channel sequence can be reset to channel zero. A rising edge on MXCLK while C3 is at the logic one level resets channel selection to channel zero.

Table 1. Channel Selection in Auto Mode

CHANNEL COUNT PINS			CLOCK PIN	LAST CHANNEL IN SEQUENCE	CHANNEL SEQUENCE
C3	C2	C1	MXCLK		
0	0	0	↑	0	0,0,0,0..
0	0	1	↑	1	0,1,0,1,..
0	1	0	↑	2	0,1,2,0,1,2,0…
0	1	1	↑	3	0,1,2,3,0,1,2,3,0…
1	X	X	↑	X	n → 0 (channel reset to zero)

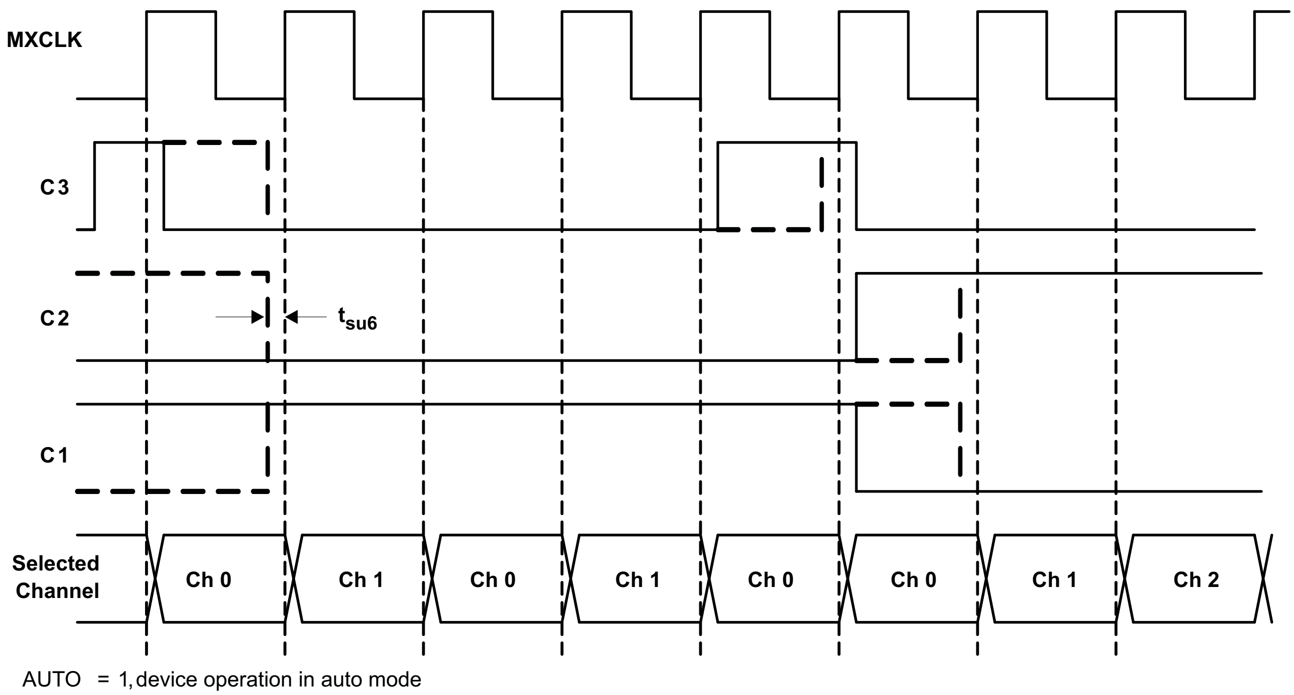


Figure 7. Multiplexer Auto Mode Timing Diagram

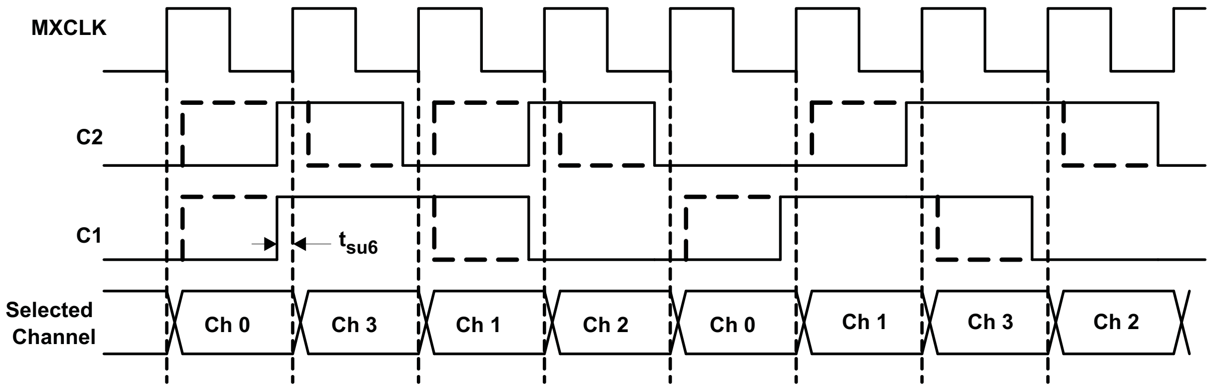
Manual Sequencing: A logic zero level on the AUTO pin selects manual sequencing mode. Pins C1and C2 set the channel address. On the rising edge of MXCLK, the addressed channel is connected to the ADC driver input.

Table 2. Channel Selection in Manual Mode

MODE	CHANNEL ADDRESS PINS			CLOCK PIN	CHANNEL
AUTO	C3	C2	C1	MXCLK	
0	X	0	0	↑	0
0	X	0	1	↑	1

Table 2. Channel Selection in Manual Mode (continued)

MODE	CHANNEL ADDRESS PINS			CLOCK PIN	CHANNEL
AUTO	C3	C2	C1	MXCLK	
0	X	1	0	↑	2
0	X	1	1	↑	3



AUTO = 0, device operation in manual mode

Figure 8. Multiplexer Manual Mode Timing Diagram

TYPICAL CHARACTERISTICS

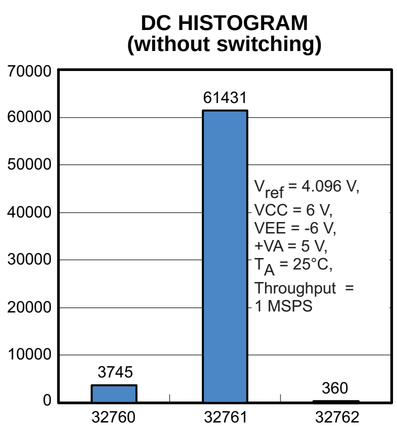


Figure 9.

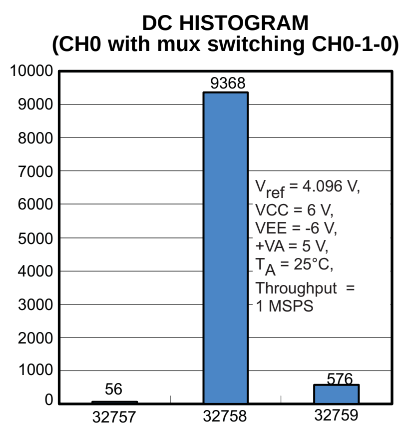


Figure 10.

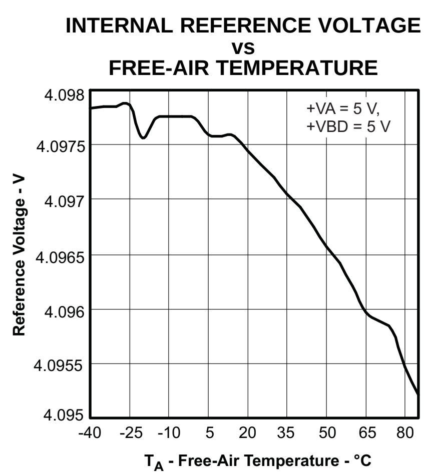


Figure 11.

TYPICAL CHARACTERISTICS (continued)

INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE

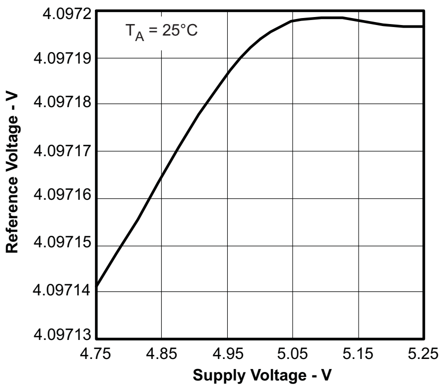


Figure 12.

ANALOG VOLTAGE (+VA) SUPPLY CURRENT (IA) vs FREE-AIR TEMPERATURE

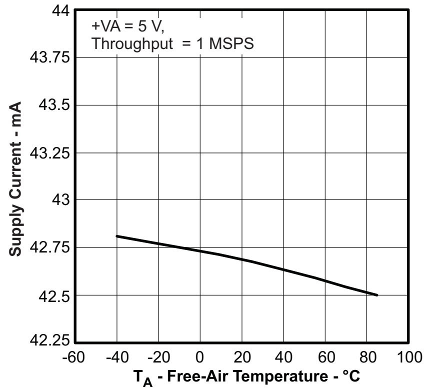


Figure 13.

SUPPLY CURRENT (IA) vs ANALOG VOLTAGE (+VA)

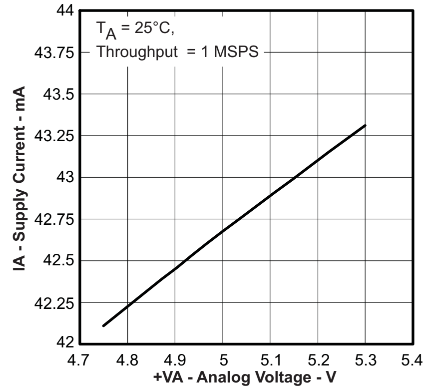


Figure 14.

ANALOG SUPPLY CURRENT vs SAMPLE RATE

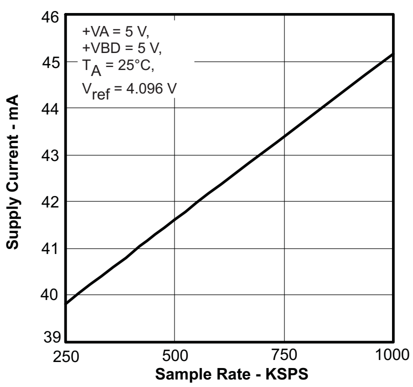


Figure 15.

OPA POSITIVE SUPPLY CURRENT (ICC) vs FREE-AIR TEMPERATURE

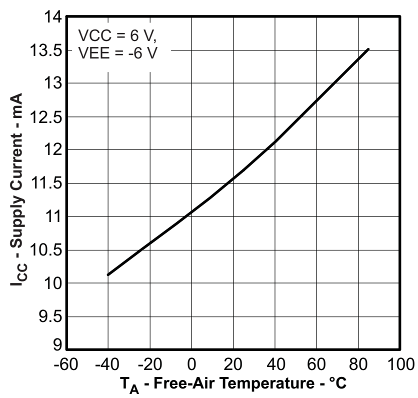


Figure 16.

OPA POSITIVE SUPPLY CURRENT (ICC) vs OPA POSITIVE SUPPLY VOLTAGE (+VCC)

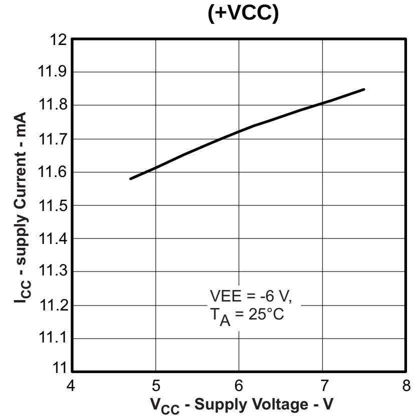


Figure 17.

OPA -VE SUPPLY CURRENT (IEE) vs FREE-AIR TEMPERATURE

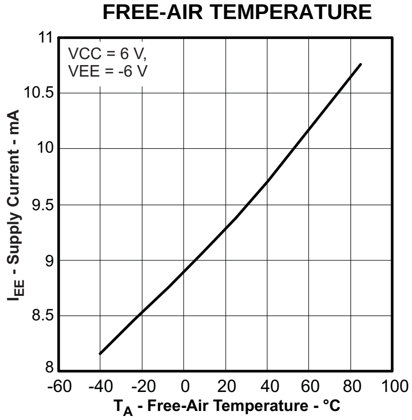


Figure 18.

OPA NEGATIVE SUPPLY CURRENT (IEE) vs OPA NEGATIVE SUPPLY (-VEE)

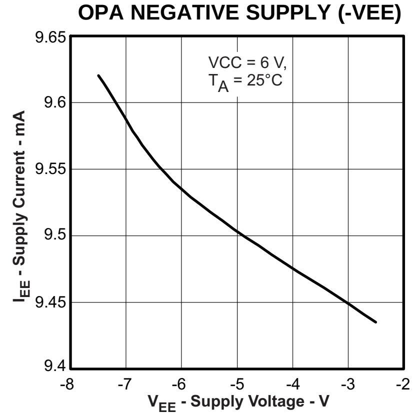


Figure 19.

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

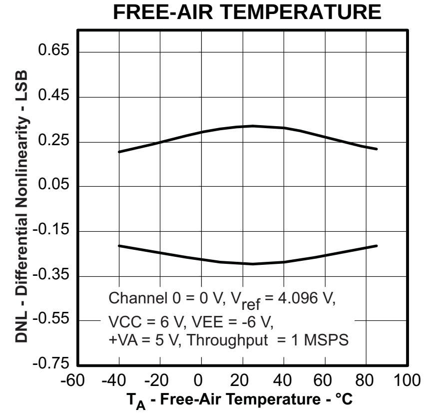


Figure 20.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL NONLINEARITY
vs
ANALOG SUPPLY VOLTAGE (+VA)

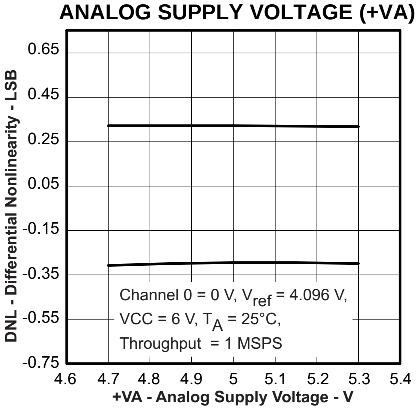


Figure 21.

DIFFERENTIAL NONLINEARITY
vs
REFERENCE VOLTAGE

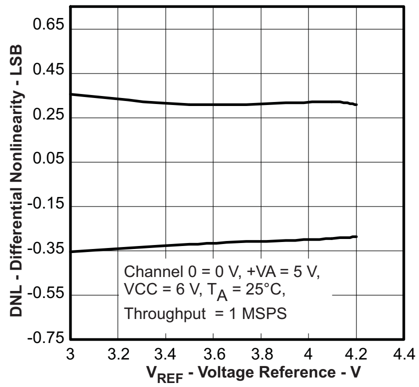


Figure 22.

DIFFERENTIAL NONLINEARITY
vs
OPA SUPPLY VOLTAGE (VCC)

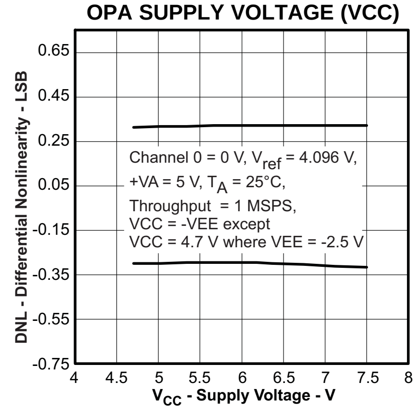


Figure 23.

DIFFERENTIAL NONLINEARITY
vs
MULTIPLEXER CHANNELS

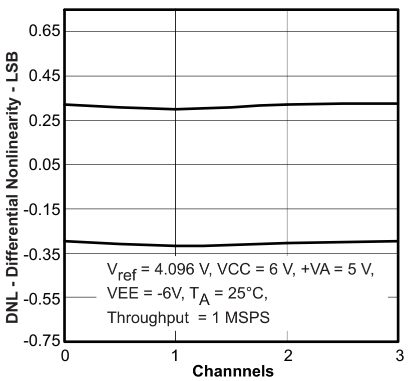


Figure 24.

INTEGRAL NONLINEARITY
vs
FREE-AIR TEMPERATURE

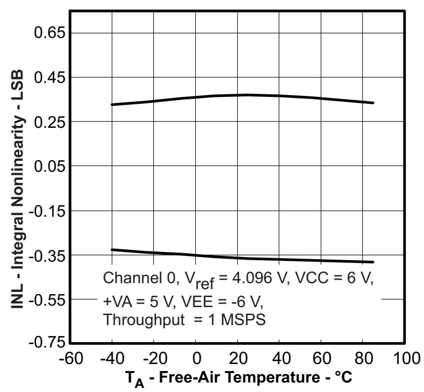


Figure 25.

INTEGRAL NONLINEARITY
vs
ANALOG SUPPLY VOLTAGE (+VA)

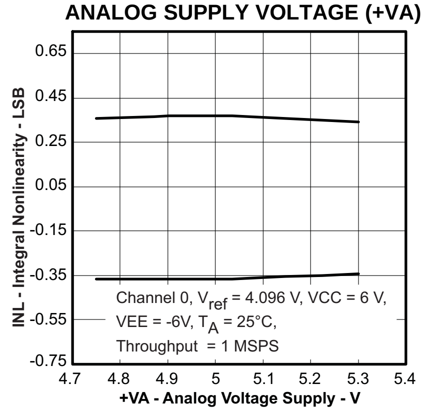


Figure 26.

INTEGRAL NONLINEARITY
vs
REFERENCE VOLTAGE

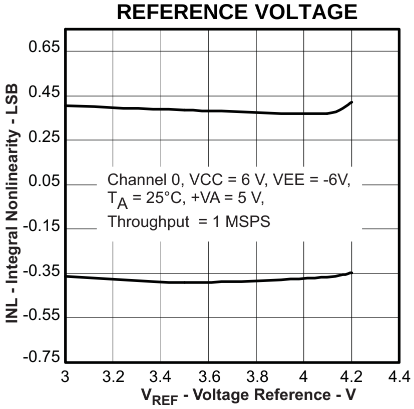


Figure 27.

INTEGRAL NONLINEARITY
vs
OPA SUPPLY VOLTAGE (+VCC)

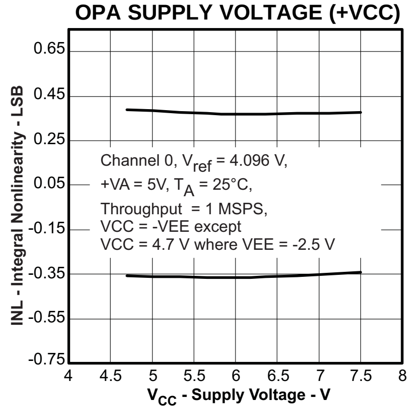


Figure 28.

INTEGRAL NONLINEARITY
vs
MULTIPLEXER CHANNELS

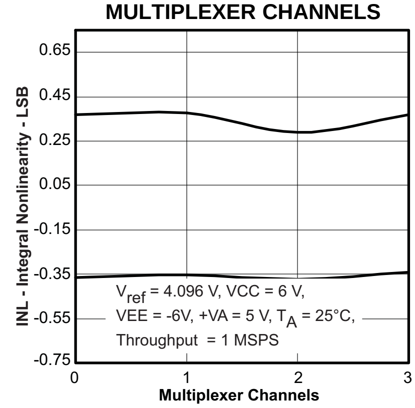


Figure 29.

TYPICAL CHARACTERISTICS (continued)

FULL CHIP OFFSET vs FREE-AIR TEMPERATURE

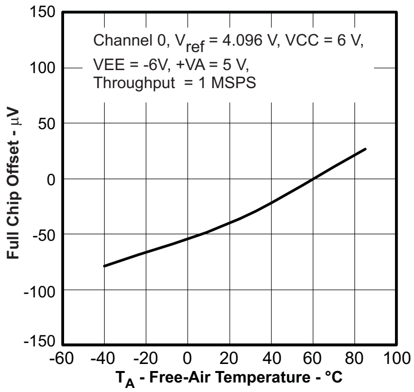


Figure 30.

FULL CHIP OFFSET vs OPA SUPPLY VOLTAGE (VCC)

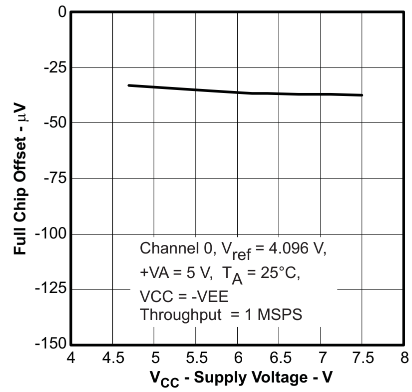


Figure 31.

FULL CHIP OFFSET vs ANALOG SUPPLY VOLTAGE (+VA)

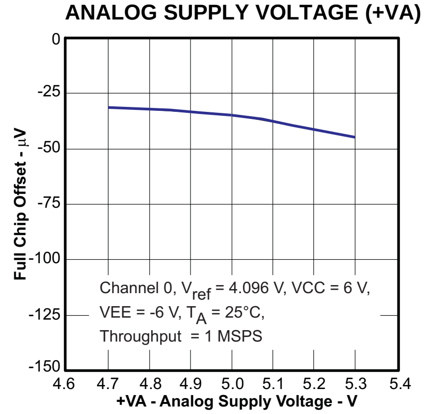


Figure 32.

FULL CHIP OFFSET vs REFERENCE VOLTAGE

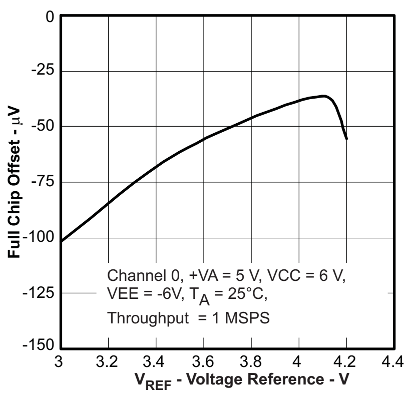


Figure 33.

FULL CHIP OFFSET vs CHANNEL

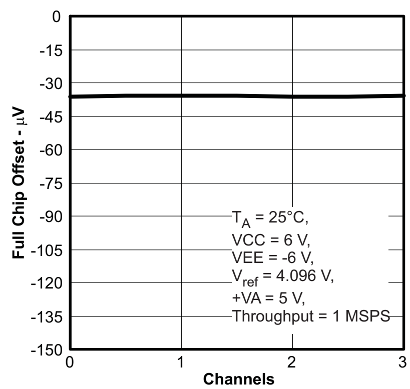


Figure 34.

FULL CHIP GAIN ERROR vs FREE-AIR TEMPERATURE

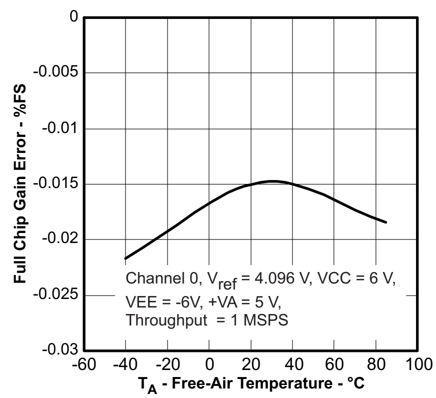


Figure 35.

FULL CHIP GAIN ERROR vs OPA SUPPLY VOLTAGE (VCC)

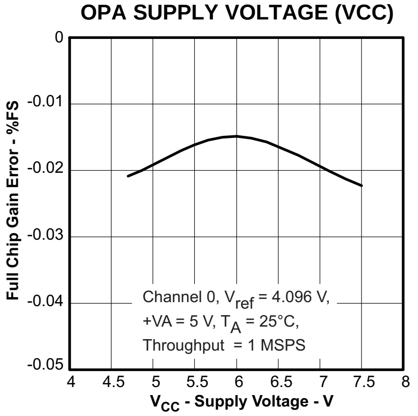


Figure 36.

FULL CHIP GAIN ERROR vs ANALOG SUPPLY VOLTAGE (+VA)

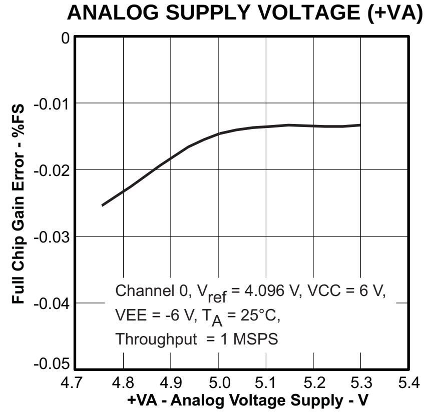


Figure 37.

FULL CHIP GAIN ERROR vs REFERENCE VOLTAGE

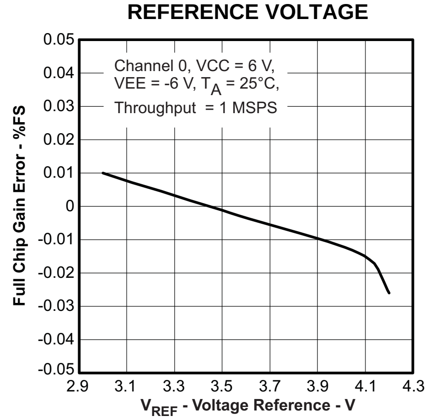


Figure 38.

TYPICAL CHARACTERISTICS (continued)

FULL CHIP GAIN ERROR vs MULTIPLEXER CHANNELS

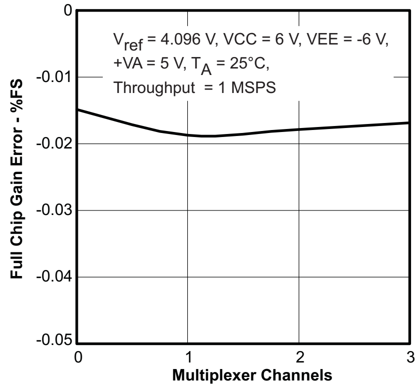


Figure 39.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

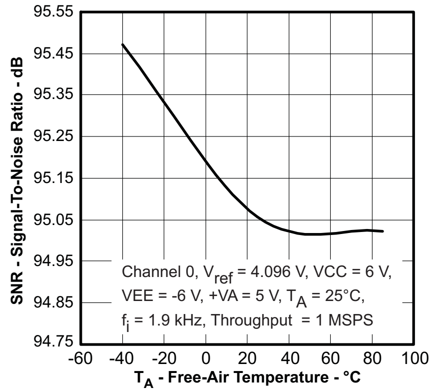


Figure 40.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

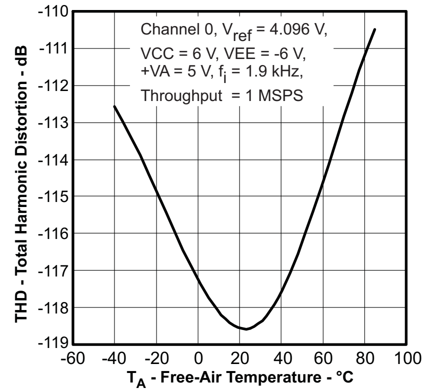


Figure 41.

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

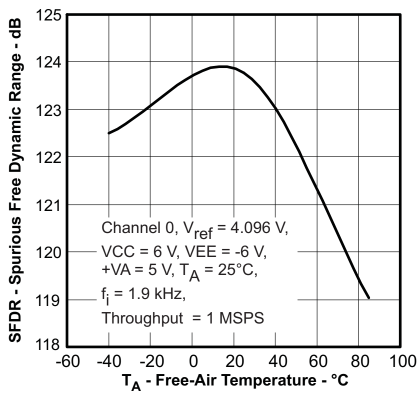


Figure 42.

EFFECTIVE NUMBER OF BITS vs FREE-AIR TEMPERATURE

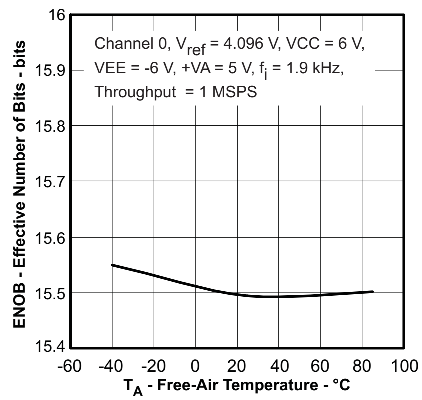


Figure 43.

SIGNAL-TO-NOISE RATIO vs ANALOG SUPPLY VOLTAGE (+VA)

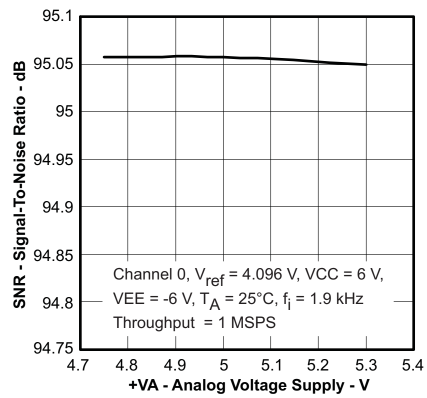


Figure 44.

TOTAL HARMONIC DISTORTION vs ANALOG SUPPLY VOLTAGE (+VA)

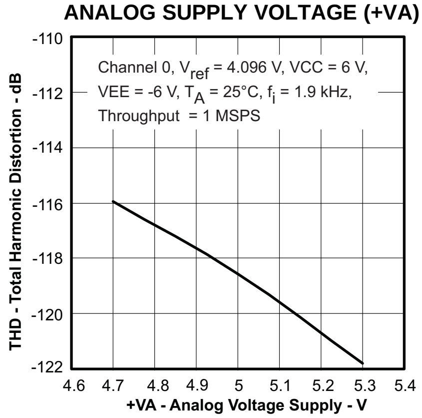


Figure 45.

SPURIOUS FREE DYNAMIC RANGE vs ANALOG SUPPLY VOLTAGE (+VA)

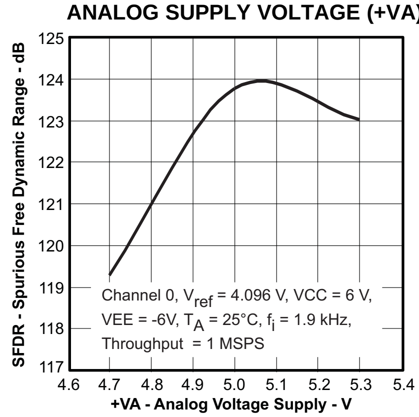


Figure 46.

EFFECTIVE NUMBERR OF BITS vs ANALOG SUPPLY VOLTAGE (+VA)

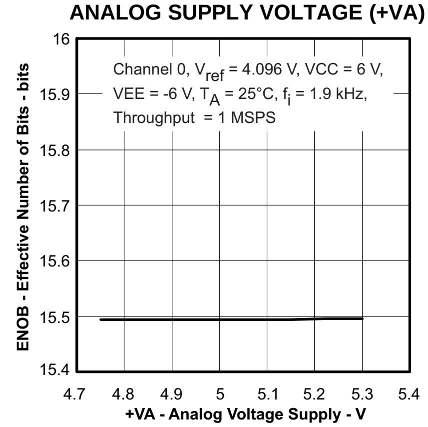


Figure 47.

TYPICAL CHARACTERISTICS (continued)

SIGNAL-TO-NOISE RATIO vs REFERENCE VOLTAGE

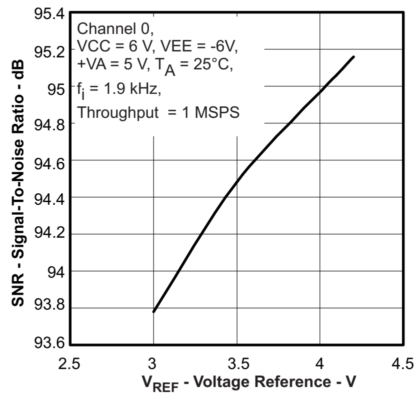


Figure 48.

TOTAL HARMONIC DISTORTION vs REFERENCE VOLTAGE

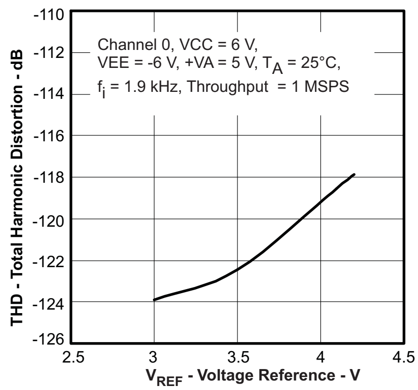


Figure 49.

SPURIOUS FREE DYNAMIC RANGE vs REFERENCE VOLTAGE

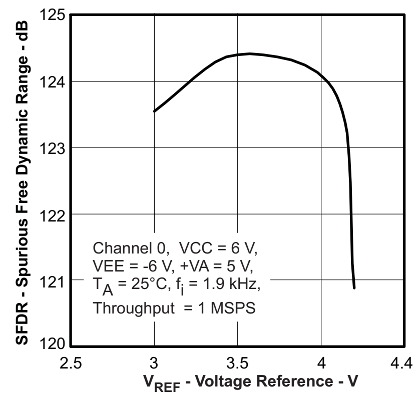


Figure 50.

EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE

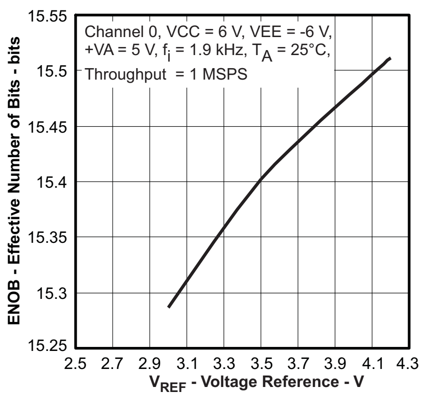


Figure 51.

SIGNAL-TO-NOISE RATIO vs OPA SUPPLY VOLTAGE VCC

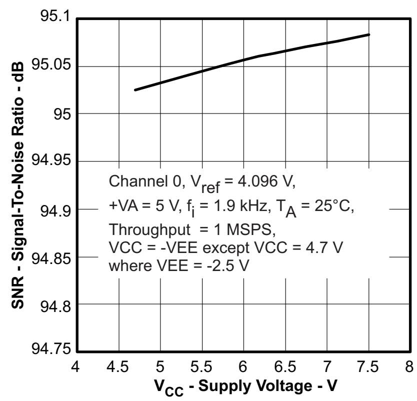


Figure 52.

TOTAL HARMONIC DISTORTION vs OPA SUPPLY VOLTAGE (VCC)

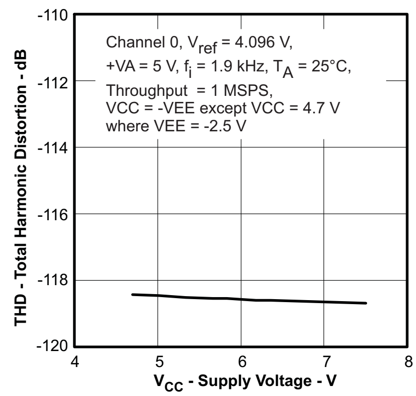


Figure 53.

SPURIOUS FREE DYNAMIC RANGE vs OPA SUPPLY VOLTAGE (VCC)

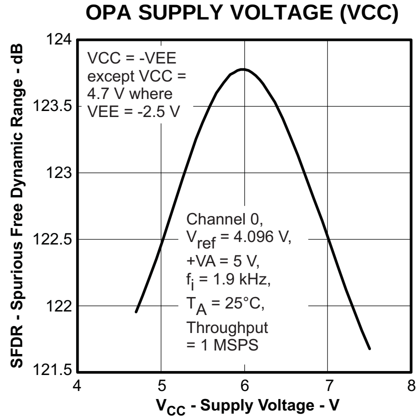


Figure 54.

EFFECTIVE NUMBER OF BITS vs OPA SUPPLY VOLTAGE (VCC)

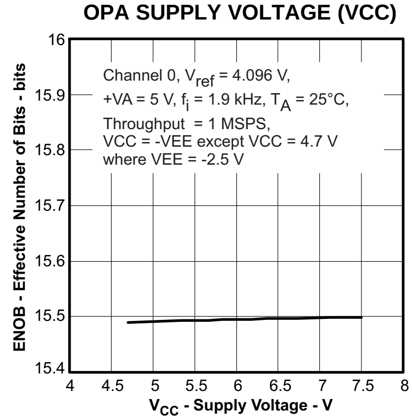


Figure 55.

SIGNAL-TO-NOISE RATIO vs SOURCE RESISTANCE (RIN)

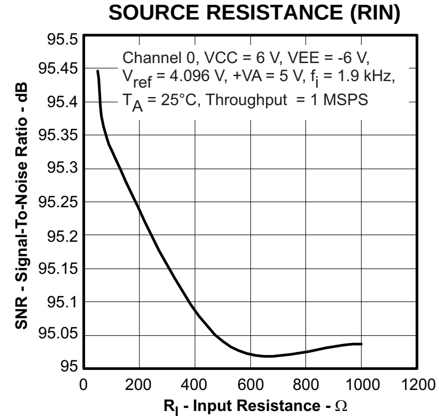


Figure 56.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION vs SOURCE RESISTANCE (RIN)

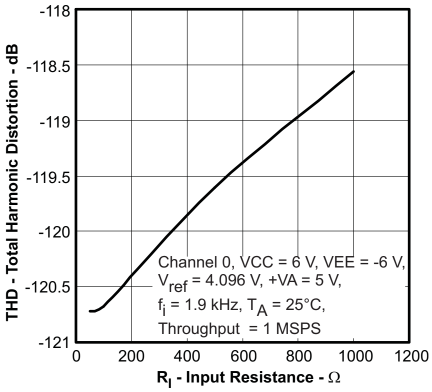


Figure 57.

SPURIOUS FREE DYNAMIC RANGE vs SOURCE RESISTANCE (RIN)

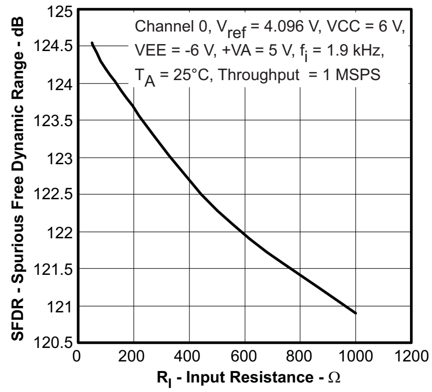


Figure 58.

EFFECTIVE NUMBER OF BITS vs SOURCE RESISTANCE (RIN)

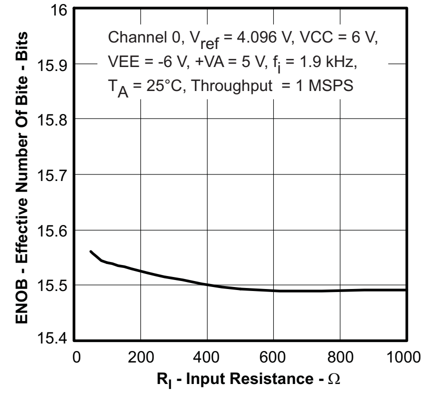


Figure 59.

SIGNAL-TO-NOISE RATIO vs MULTIPLEXER CHANNELS

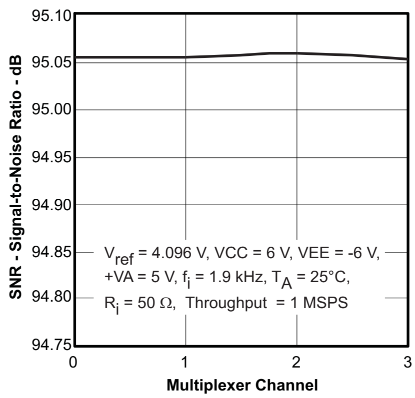


Figure 60.

TOTAL HARMONIC DISTORTION vs MULTIPLEXER CHANNELS

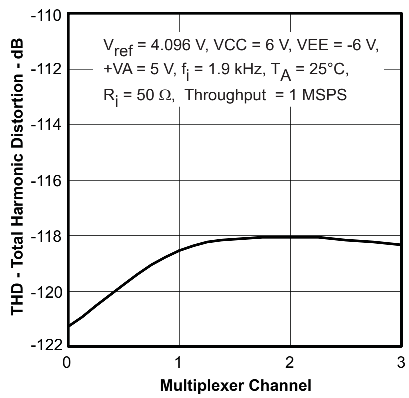


Figure 61.

SPURIOUS FREE DYNAMIC RANGE vs MULTIPLEXER CHANNELS

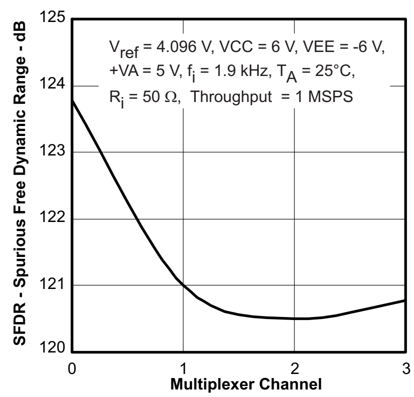


Figure 62.

EFFECTIVE NUMBER OF BITS vs MULTIPLEXER CHANNELS

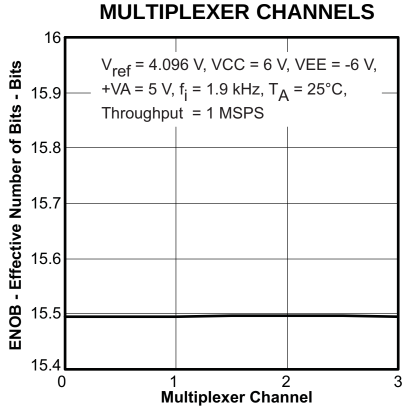


Figure 63.

VCM_O VOLTAGE vs OPA SUPPLY VOLTAGE (VCC)

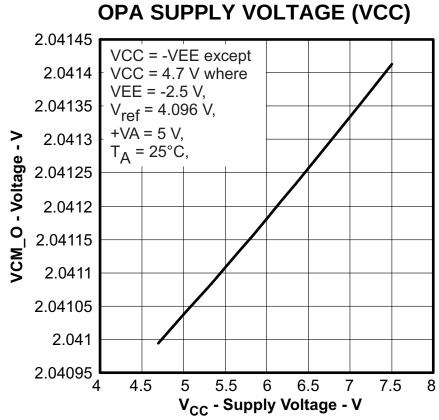


Figure 64.

BUFFER REFERENCE OUTPUT VOLTAGE vs OPA SUPPLY VOLTAGE (VCC)

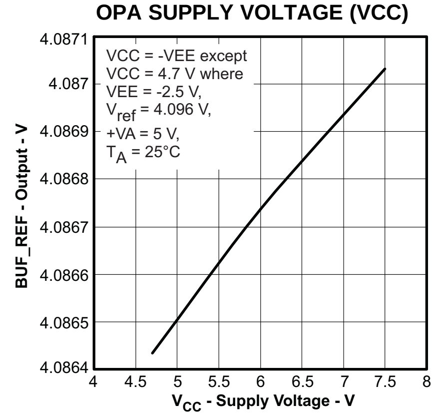


Figure 65.

TYPICAL CHARACTERISTICS (continued)

TYPICAL DNL

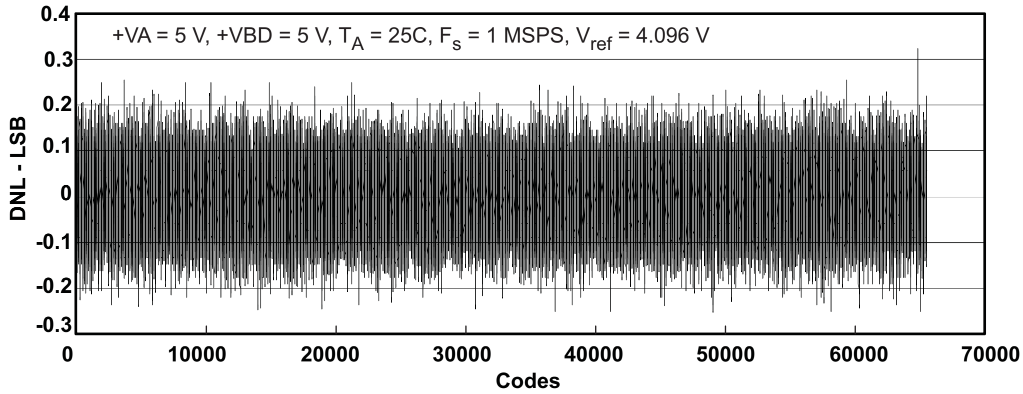


Figure 66.

TYPICAL INL

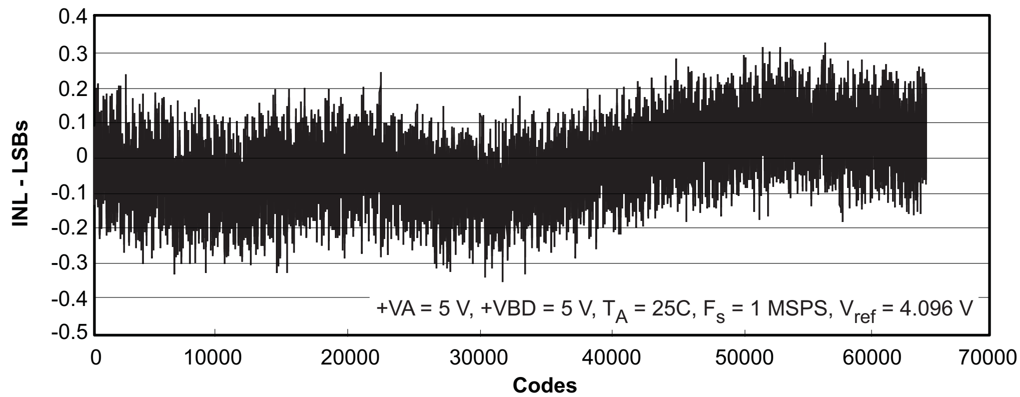


Figure 67.

TYPICAL FFT

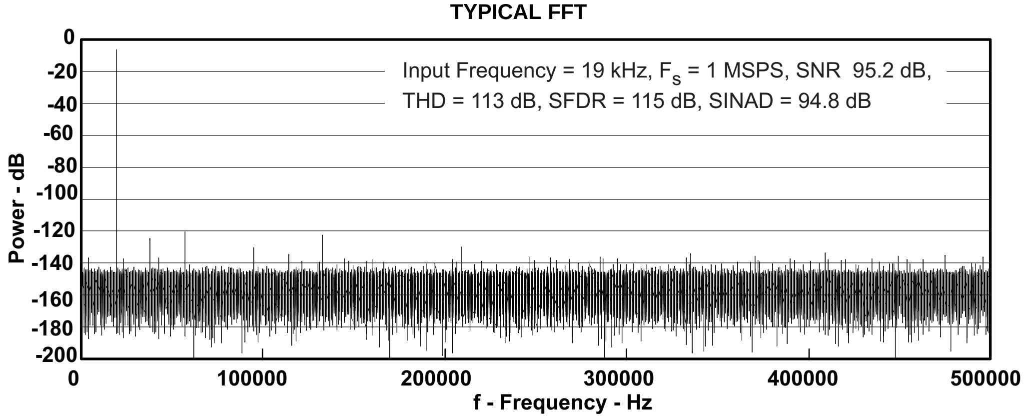


Figure 68.

APPLICATION INFORMATION

As discussed before, the ADS8254 is 16-bit analog SoC that includes various blocks like a multiplexer, ADC driver, internal reference, internal reference buffer, buffered reference output, and Ref/2 output on-board. The following diagram shows the recommended analog and digital interfacing of the ADS8254.

APPLICATION DIAGRAM

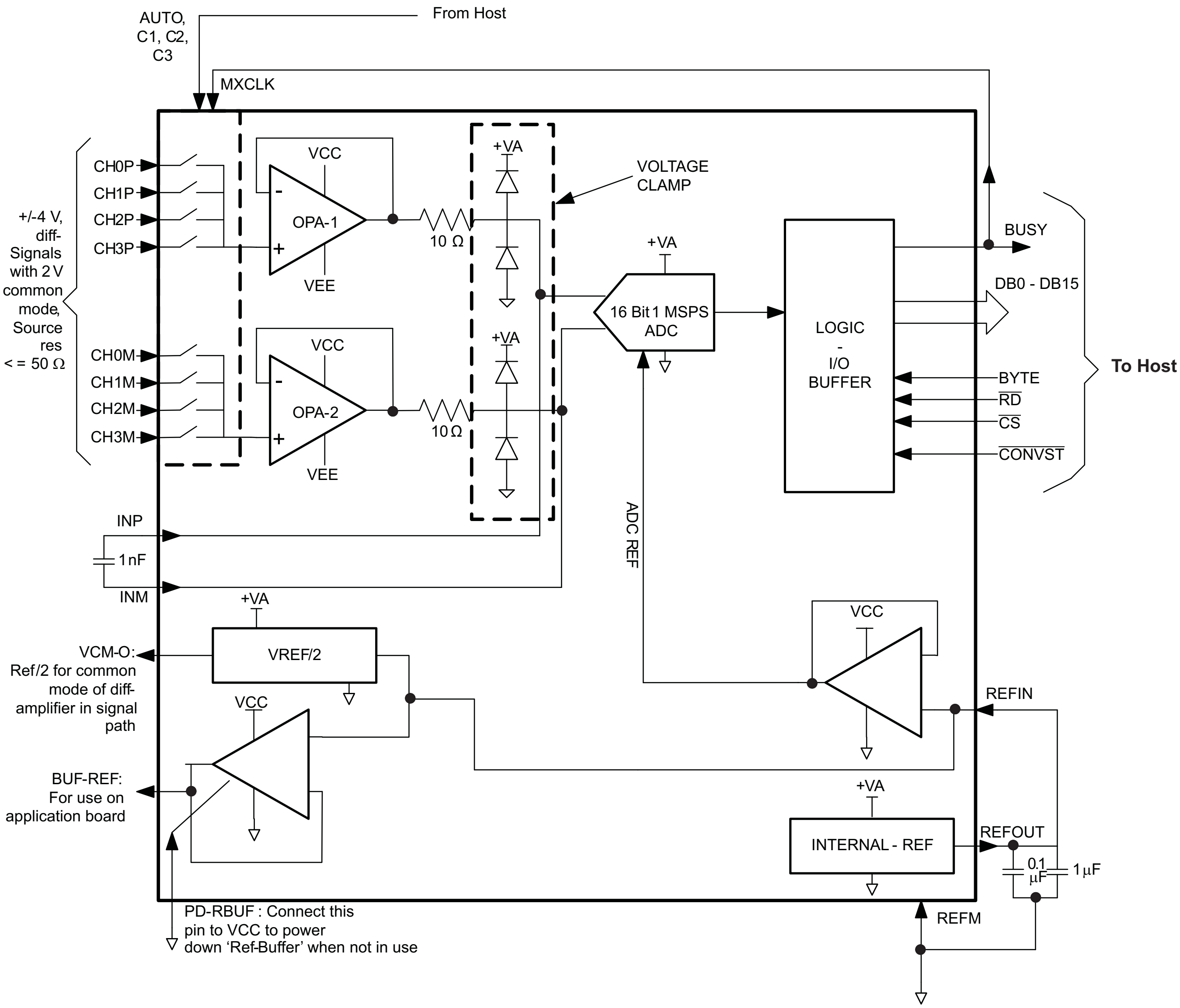


Figure 69. Analog and Digital Interface Diagram

As shown in Figure 69, the ADS8254 accepts unipolar differential analog inputs in the range of $\pm V_{ref}$ with a common-mode voltage of $V_{ref}/2$. An application may require the interfacing of bipolar input signals. The following diagram shows the conversion of bipolar input signals to unipolar differential signals.

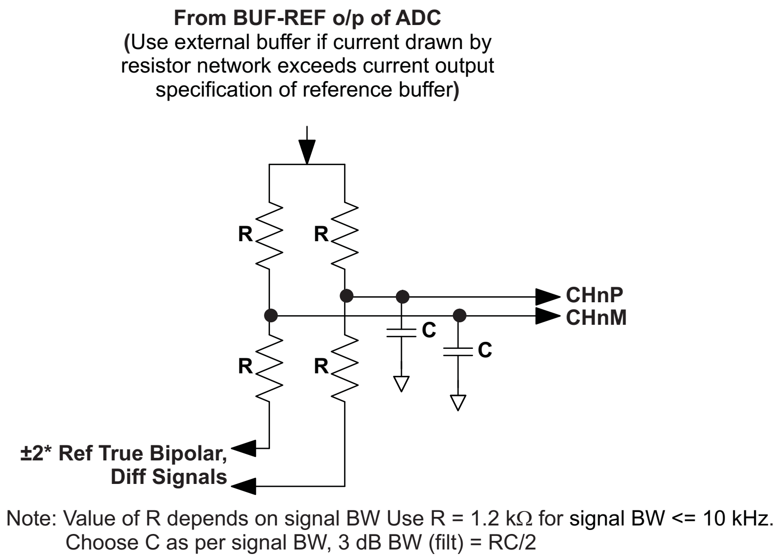


Figure 70. Bipolar Input Signals to Unipolar Differential Signals Conversion

MICROCONTROLLER INTERFACING

ADS8254 to 8-Bit Microcontroller Interface

Figure 71 shows a parallel interface between the ADS8254 and a typical microcontroller using an 8-bit data bus. The BUSY signal is used as a falling edge interrupt to the microcontroller.

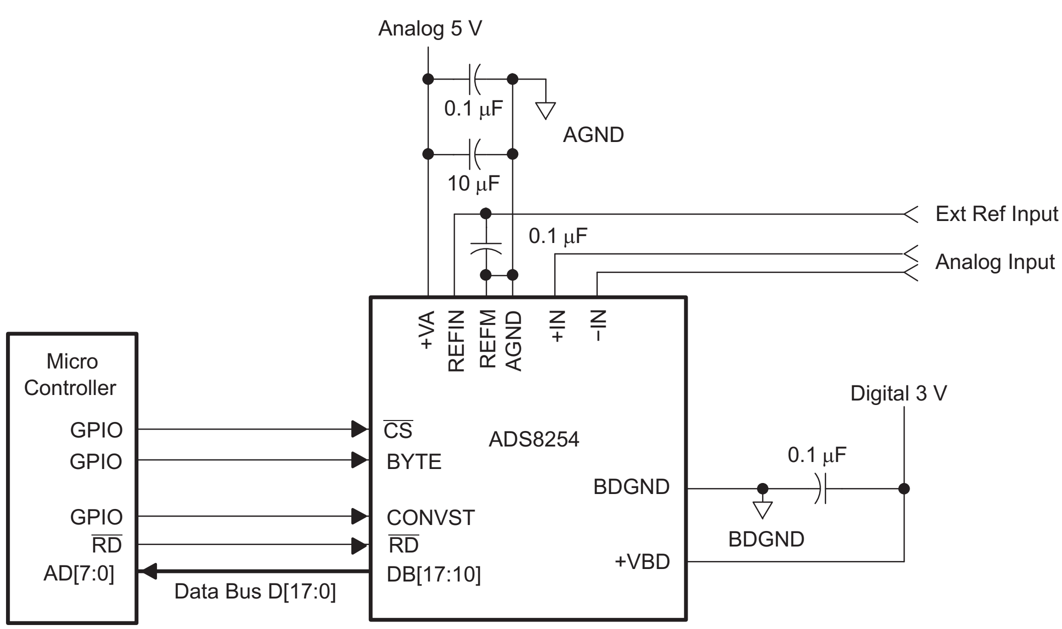


Figure 71. ADS8254 Application Circuitry

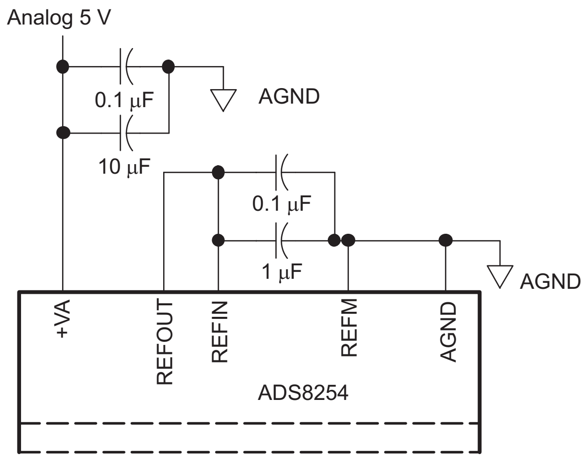


Figure 72. ADS8254 Using Internal Reference

PRINCIPLES OF OPERATION

The ADS8254 features a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 71 for the application circuit for the ADS8254.

The conversion clock is generated internally. The conversion time of 650 ns is capable of sustaining a 1 MHz throughput.

When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8254 can operate with an external reference with a range from 3.0 V to 4.2 V. The reference voltage on the input pin 10 (REFIN) of the converter is internally buffered. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF5040 can be used to drive this pin. A 0.1-µF decoupling capacitor is required between REFIN and REFM pins (pin 10 and pin 9) of the converter. This capacitor should be placed as close as possible to the pins of the device. Designers should strive to minimize the routing length of the traces that connect the terminals of the capacitor to the pins of the converter. An RC network can also be used to filter the reference voltage. A 100-Ω series resistor and a 0.1-µF capacitor, which can also serve as the decoupling capacitor can be used to filter the reference voltage.

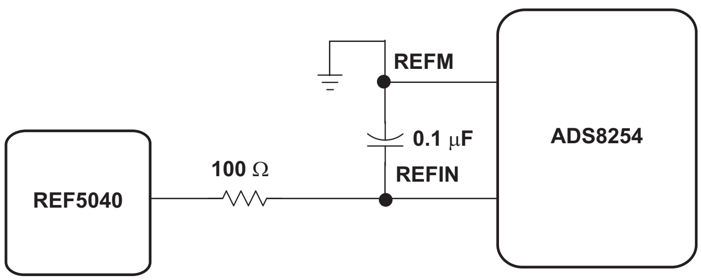


Figure 73. ADS8254 Using External Reference

The ADS8254 also has limited low pass filtering capability built into the converter. The equivalent circuitry on the REFIN input is as shown in Figure 74.

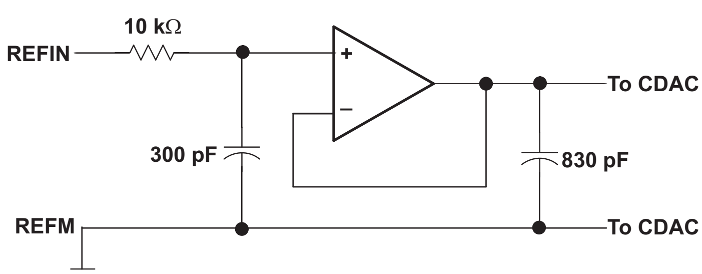


Figure 74. Simplified Reference Input Circuit

The REFM input of the ADS8254 should always be shorted to AGND. A 4.096-V internal reference is included. When the internal reference is used, pin 11 (REFOUT) is connected to pin 10 (REFIN) with an 0.1-µF decoupling capacitor and 1-µF storage capacitor between pin 11 (REFOUT) and pin 9 (REFM) (see Figure 72). The internal reference of the converter is double buffered. If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion. Pin 11 (REFOUT) can be left unconnected (floating) if external reference is used (as shown in Figure 74).

ANALOG INPUT

The ADS8254 features an analog multiplexer, a differential, high-input impedance, unity-gain ADC driver, and a high-performance ADC. Typically it would require alot of care in the selection of the driving circuit components and board layout for high resolution ADC driving. However, an on-board ADC driver simplifies the job for the user. All that is needed is to decouple AINP and AINM with a 1-nF decoupling capacitor across these two terminals as close to the device as possible. The multiplexer inputs tolerate a source impedance of up to 50 Ω for the specified device performance at a 1-MSPS operating speed. This relaxes the constraints on the signal conditioning circuit. In the case of true bipolar input signals, it is possible to condition them with a resister divider as shown in Figure 70. The device permits use of 1.2-kΩ resistors for the divider with an effective source impedance of 600 Ω for signal BW less than 10 kHz. A suitable capacitor value can be used to limit signal BW which limits noise coming from the resistor divider network. Care must be taken about absolute analog voltage at the multiplexer input terminals. This voltage should not exceed VCC and VEE. The clamp at driver OPA limits the voltage applied to the ADC input.

Reading Data

The ADS8254 outputs full parallel data in straight binary format as shown in Table 3. The parallel output is active when $\overline{CS}$ and $\overline{RD}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{CONVST}$. This is 50 ns prior to the falling edge of $\overline{CONVST}$ and 40 ns after the falling edge. No data read should attempted within this zone. Any other combination of $\overline{CS}$ and $\overline{RD}$ sets the parallel output to 3-state. BYTE is used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. Refer to Table 3 for ideal output codes.

Table 3. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
Full scale range	2 × (+V_{ref})		
Least significant bit (LSB)	2 × (+V_{ref})/65536	**BINARY CODE**	**HEX CODE**
+Full scale	(+V_{ref}) – 1 LSB	0111 1111 1111 1111	7FFF
Midscale	0 V	0000 0000 0000 0000	0000
Midscale – 1 LSB	0 V – 1 LSB	1111 1111 1111 1111	FFFF
Zero	–V_{ref}	1000 0000 0000 0000	8000

The output data is a full 16-bit word (D15–D0) on DB15–DB0 pins (MSB–LSB) if BYTE is low.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB15–DB8. In this case two reads are necessary: the first as before, leaving BYTE low and reading the 8 most significant bits on pins DB15–DB8, then bringing BYTE high. When BYTE is high, the low bits (D7–D0) appear on pins DB15–DB8.

This multiword read operation can be performed with multiple active $\overline{RD}$ (toggling) or with $\overline{RD}$ held low for simplicity. This is referred to as the AUTO READ operation.

Table 4. Conversion Data Read Out

BYTE	DATA READ OUT	
	PINS DB15–DB8	**PINS DB7–DB0**
High	D7–D0	All One's
Low	D15–D8	D7–D0

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS8254IBRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8254IBRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8254IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8254IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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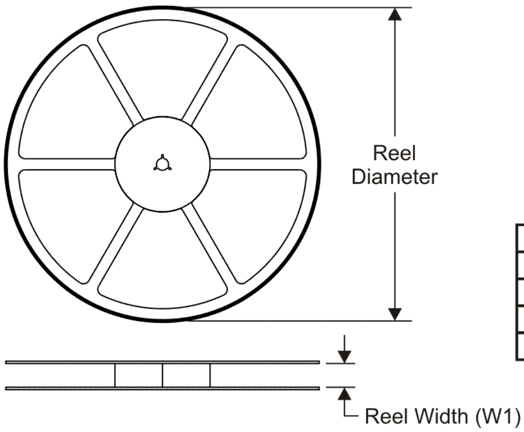
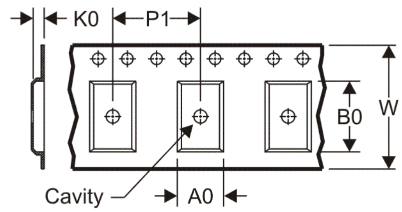
TAPE AND REEL INFORMATION

REEL DIMENSIONS

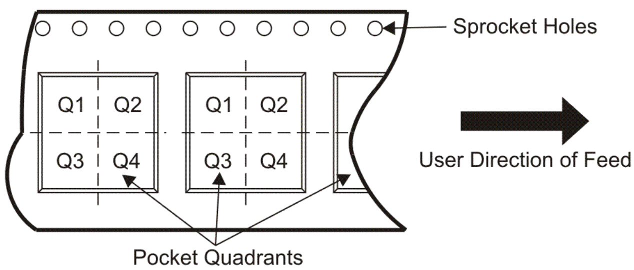


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

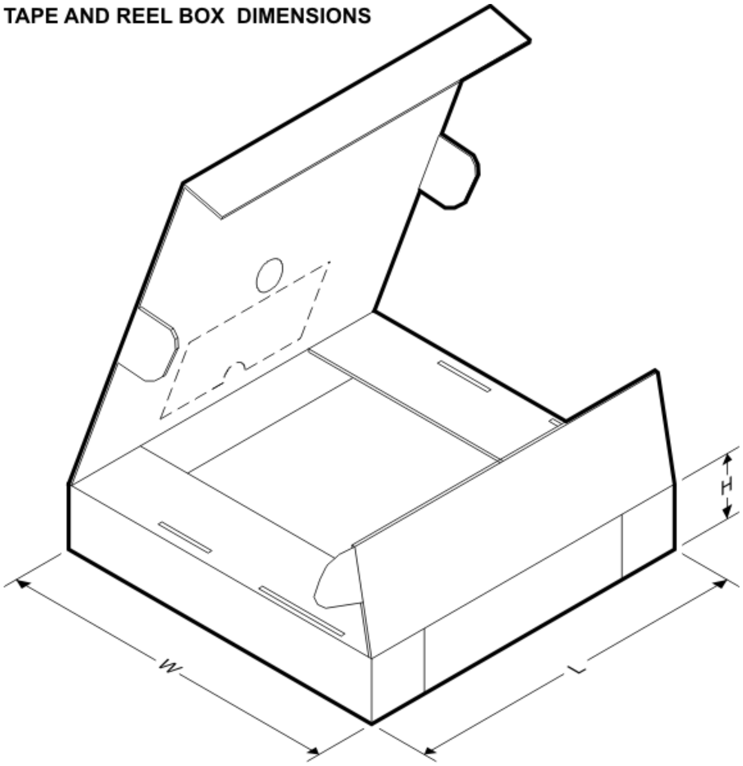
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8254IBRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8254IBRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8254IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8254IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

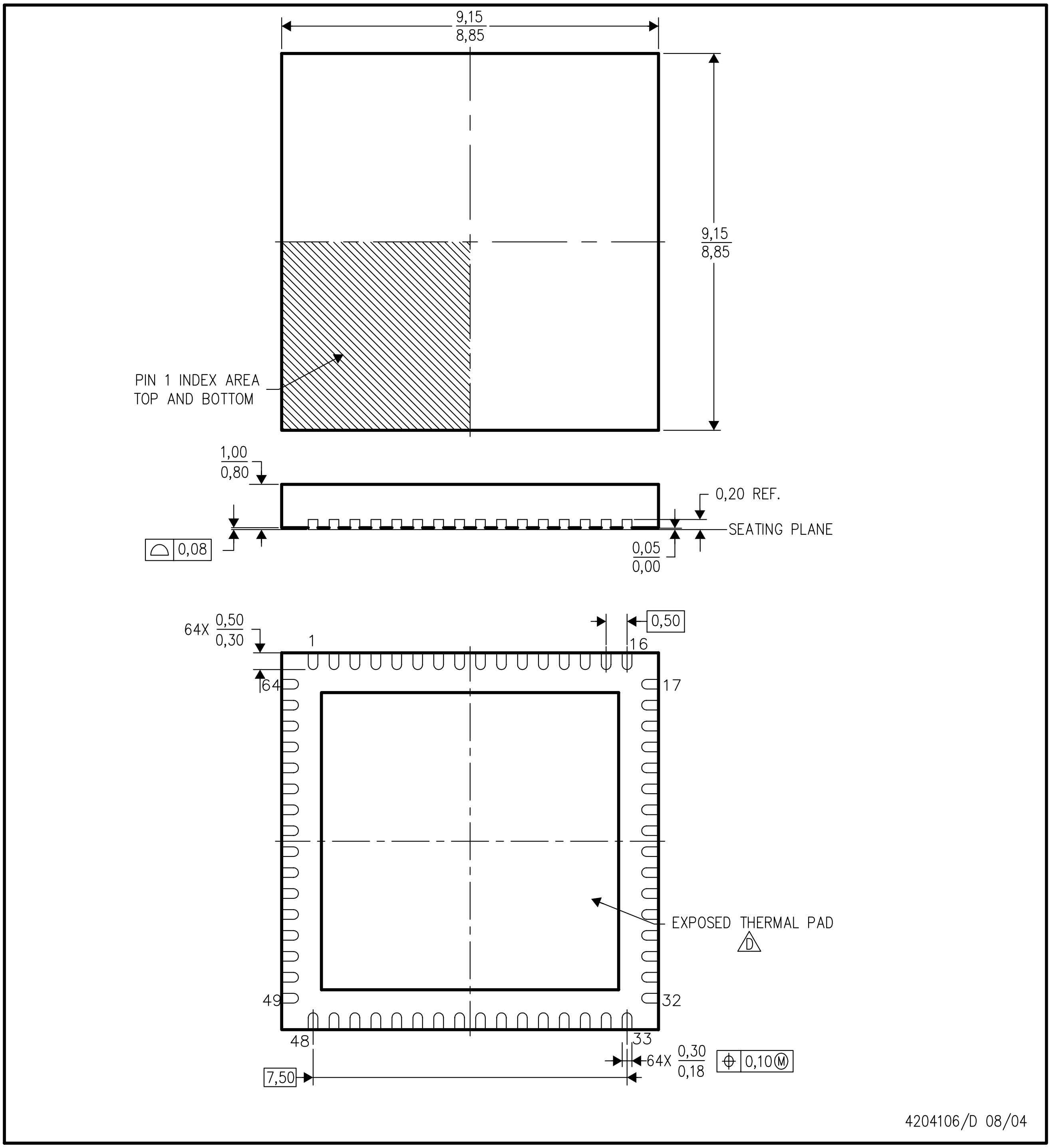
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8254IBRGCR	VQFN	RGC	64	2000	333.2	345.9	28.6
ADS8254IBRGCT	VQFN	RGC	64	250	333.2	345.9	28.6
ADS8254IRGCR	VQFN	RGC	64	2000	333.2	345.9	28.6
ADS8254IRGCT	VQFN	RGC	64	250	333.2	345.9	28.6

RGC (S-PQFP-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK



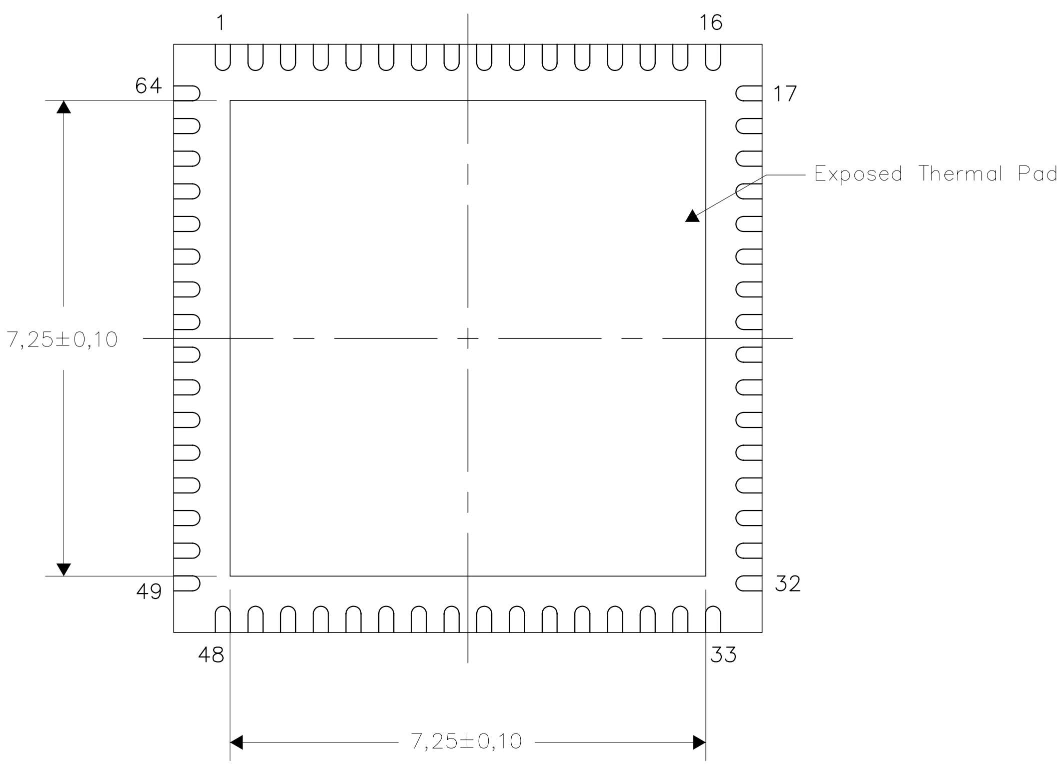
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration .
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

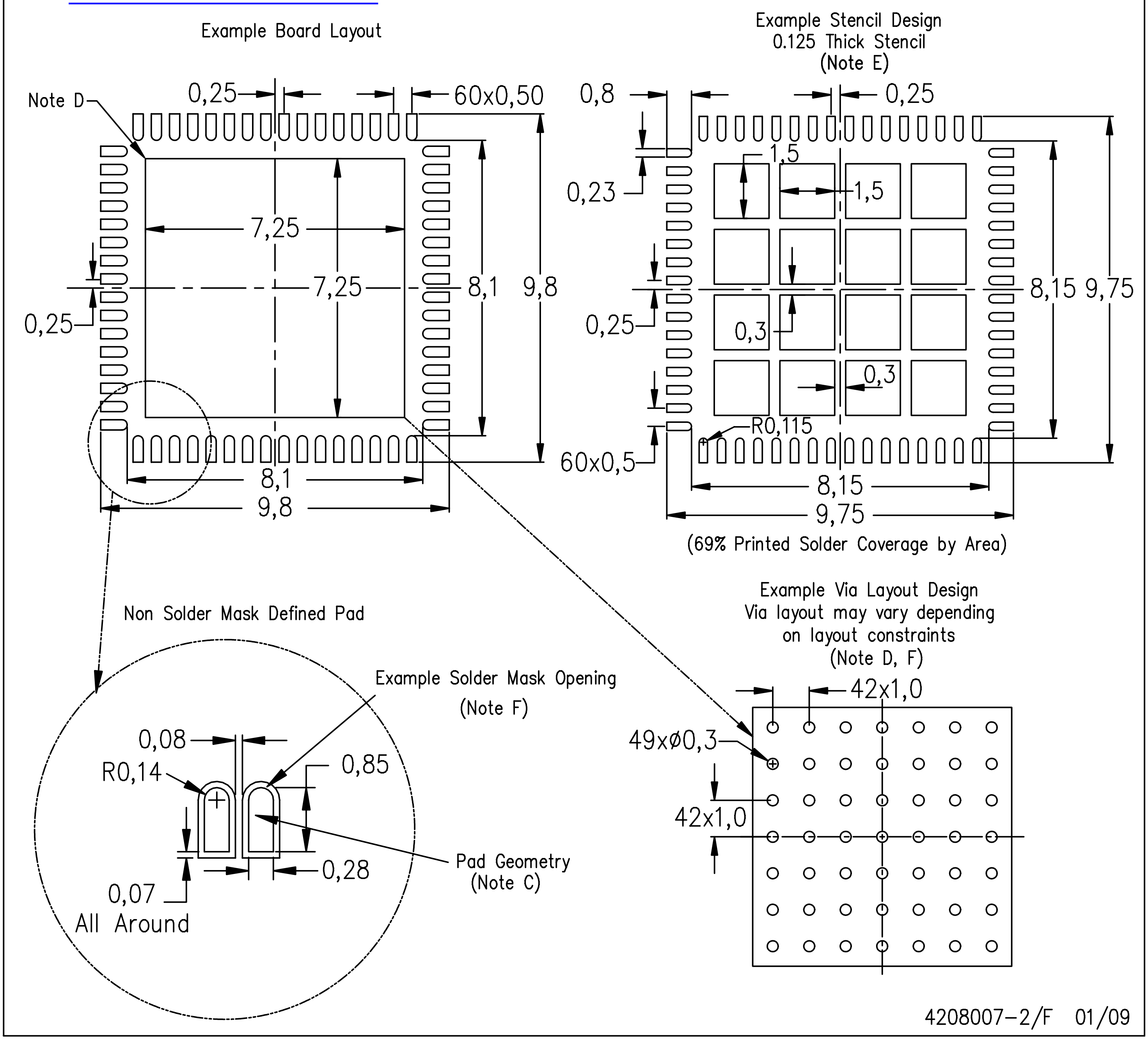


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGC (S–PVQFN–N64)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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