DATA SHEET

NEC



# MOS FIELD EFFECT TRANSISTORS

# 2SK2369/2SK2370

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

The 2SK2369/2SK2370 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

### FEATURES

- Low On-Resistance
  - 2SK2369: $R_{DS(on)}$ = 0.35 Ω ($V_{GS}$ = 10 V, $I_D$ = 10 A)
  - 2SK2370: $R_{DS(on)}$ = 0.4 Ω ($V_{GS}$ = 10 V, $I_D$ = 10 A)
- Low $C_{iss}$   $C_{iss}$ = 2400 pF TYP.
- High Avalanche Capability Ratings

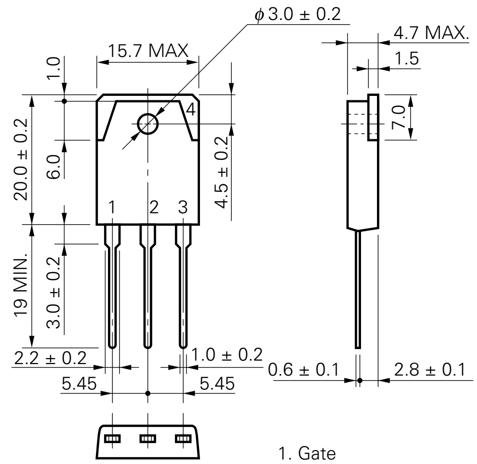
### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 ˚C)

| | | | |
|---|---|---|---|
| Drain to Source Voltage(2SAK2369/2370) | $V_{DSS}$ | 450/500 | V |
| Gate to Source Voltage | $V_{GSS}$ | ±30 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ±20 | A |
| Drain Current (pulse)* | $I_{D(pulse)}$ | ±80 | A |
| Total Power Dissipation ($T_c$ = 25 ˚C) | $P_{T1}$ | 140 | W |
| Total Power Dissipation ($T_A$ = 25 ˚C) | $P_{T2}$ | 3.0 | W |
| Channel Temperature | $T_{ch}$ | 150 | ˚C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | ˚C |
| Single Avalanche Current** | $I_{AS}$ | 20 | A |
| Single Avalanche Energy** | $E_{AS}$ | 285 | mJ |

* PW ≤ 10 $\mu$s, Duty Cycle ≤ 1 %

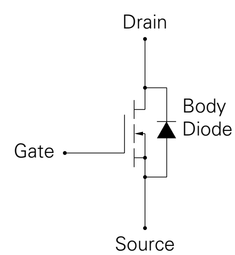
** Starting $T_{ch}$ = 25 ˚C, $R_G$ = 25 Ω, $V_{GS}$ = 20 V → 0

### PACKAGE DIMENSIONS
(in millimeters)




1. Gate
2. Drain
3. Source
4. Fin (Drain)

**MP-88**

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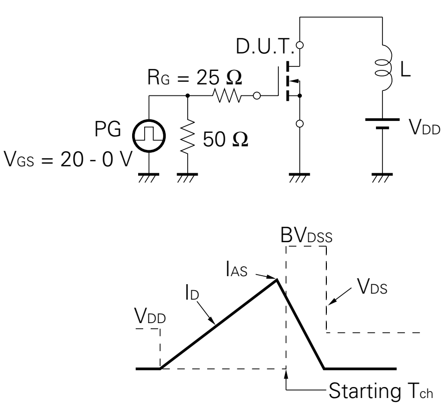
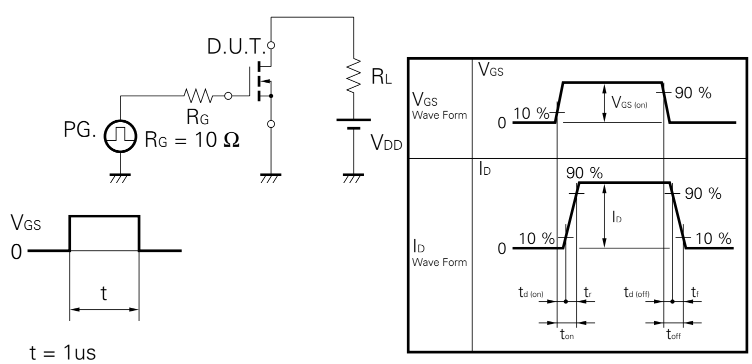
## ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|
| Drain to Source On-State Resistance | $R_{DS(on)}$ | | 0.30 | 0.35 | Ω | $V_{GS}$ = 10 V | 2SK2369 |
| | | | 0.32 | 0.40 | | $I_D$ = 10 V | 2SK2370 |
| Gate to Source Cutoff Voltage | $V_{GS(off)}$ | 2.5 | | 3.5 | V | $V_{DS}$ = 10 V, $I_D$ = 1 mA | |
| Forward Transfer Admittance | $\lvert y_{fs} \rvert$ | 7.5 | | | S | $V_{DS}$ = 10 V, $I_D$ = 10 A | |
| Drain Leakage Current | $I_{DSS}$ | | | 100 | μA | $V_{DS}$ = $V_{DSS}$, $V_{GS}$ = 0 | |
| Gate to Source Leakage Current | $I_{GSS}$ | | | ±100 | nA | $V_{GS}$ = ±30 V, $V_{DS}$ = 0 | |
| Input Capacitance | $C_{iss}$ | | 2400 | | pF | $V_{DS}$ = 10 V | |
| Output Capacitance | $C_{oss}$ | | 500 | | pF | $V_{GS}$ = 0 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 45 | | pF | f = 1 MHz | |
| Turn-On Delay Time | $t_{d(on)}$ | | 35 | | ns | $I_D$ = 10 A | |
| Rise Time | $t_r$ | | 60 | | ns | $V_{GS}$ = 10 V | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 105 | | ns | $V_{DD}$ = 150 V | |
| Fall Time | $t_f$ | | 65 | | ns | $R_G$ = 10 Ω $R_L$ = 15 Ω | |
| Total Gate Charge | $Q_G$ | | 65 | | nC | $I_D$ = 20 A | |
| Gate to Source Charge | $Q_{GS}$ | | 15 | | nC | $V_{DD}$ = 400 V | |
| Gate to Drain Charge | $Q_{GD}$ | | 30 | | nC | $V_{GS}$ = 10 V | |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | | 1.0 | | V | $I_F$ = 20 A, $V_{GS}$ = 0 | |
| Reverse Recovery Time | $t_{rr}$ | | 500 | | ns | $I_F$ = 20 A, $V_{GS}$ = 0 | |
| Reverse Recovery Charge | $Q_{rr}$ | | 3.5 | | μC | di/dt = 50 A/μs | |

**Test Circuit 1 Avalanche Capability**

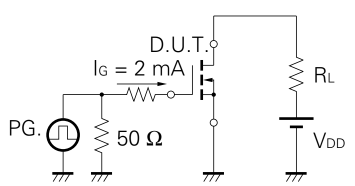



**Test Circuit 2 Switching Time**




t = 1us
Duty Cycle ≤ 1 %

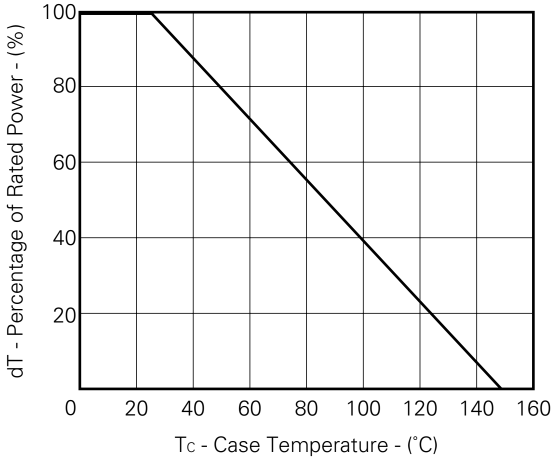
**Test Circuit 3 Gate Charge**



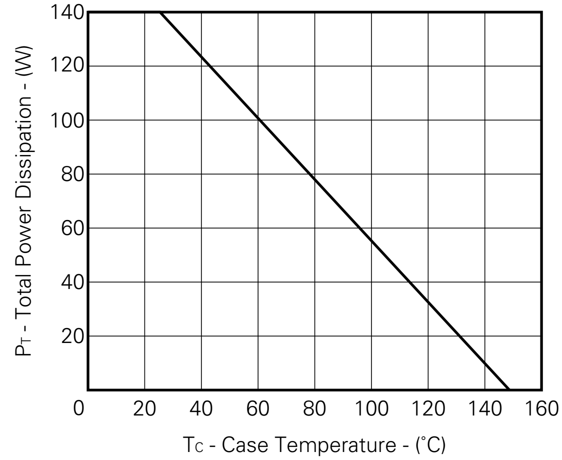

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C)

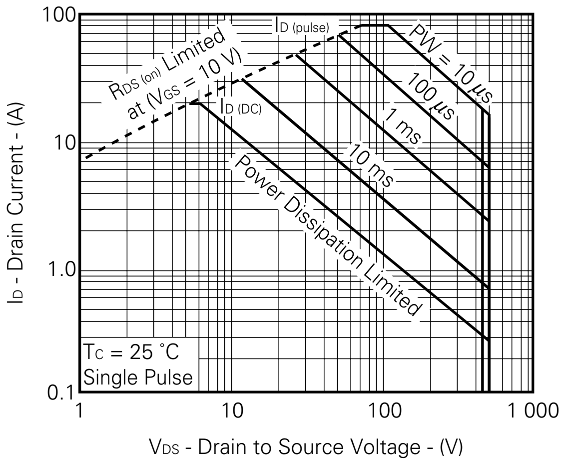
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



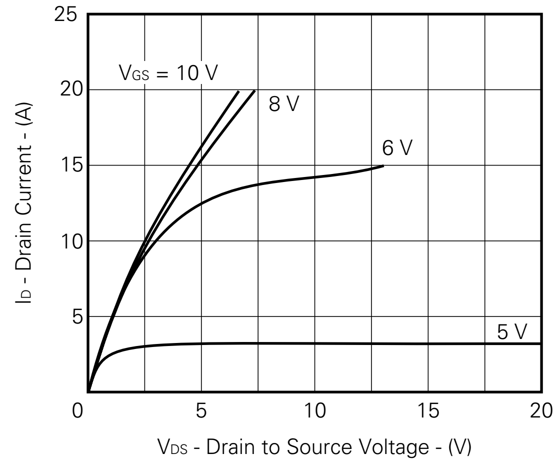

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



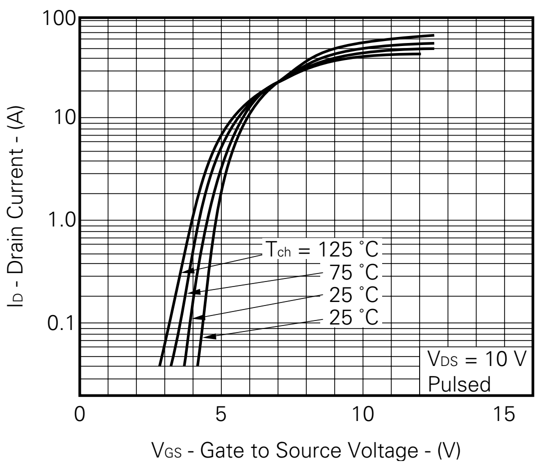

FORWARD BIAS SAFE OPERATING AREA



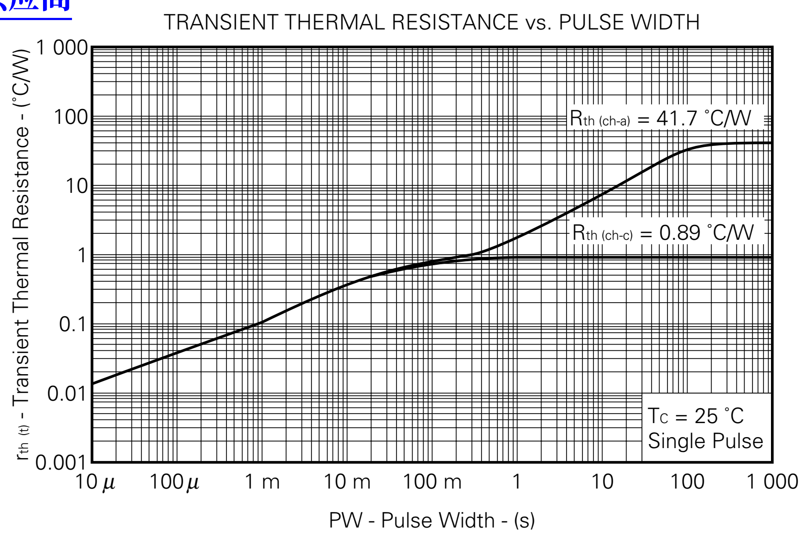

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

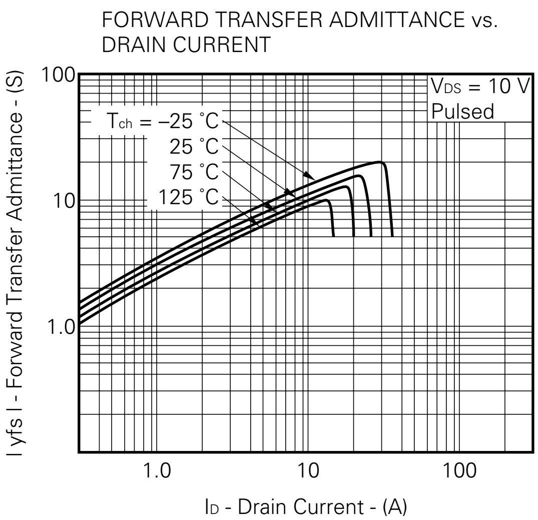


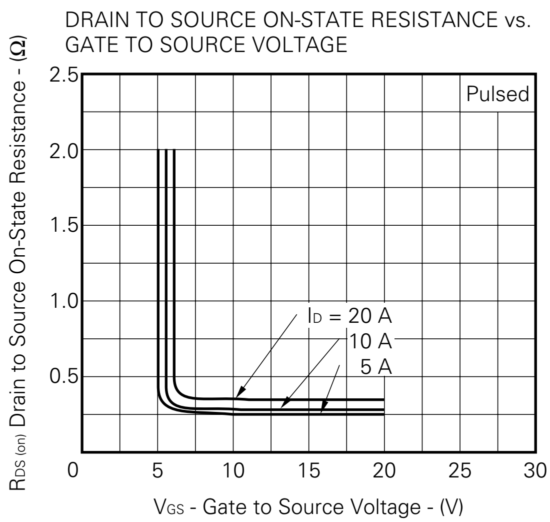

DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE

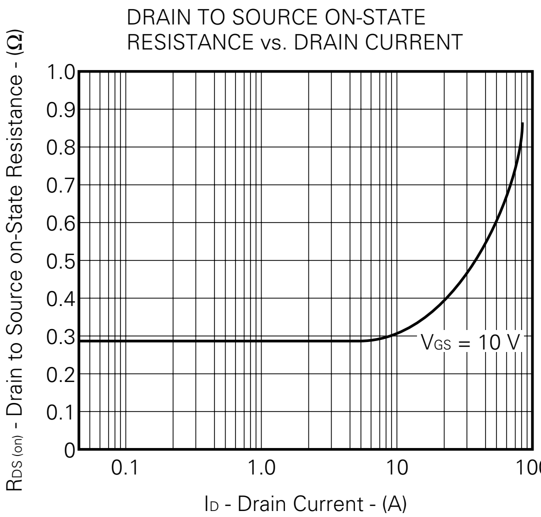


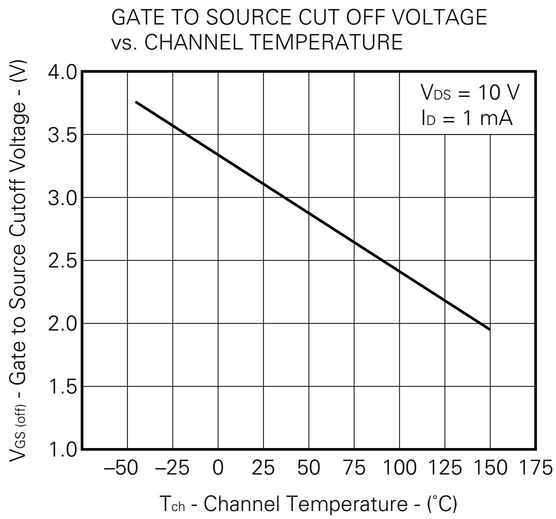
查询"2SK2369"供应商



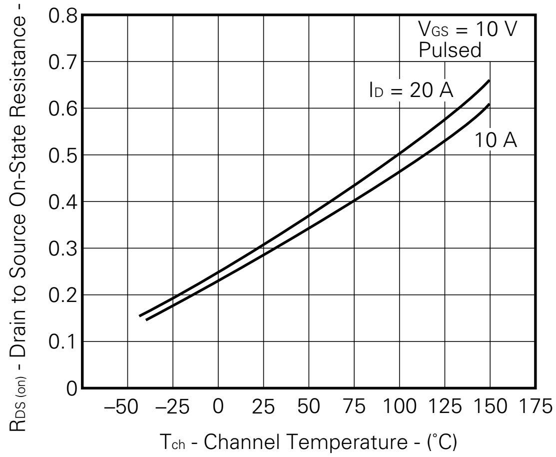



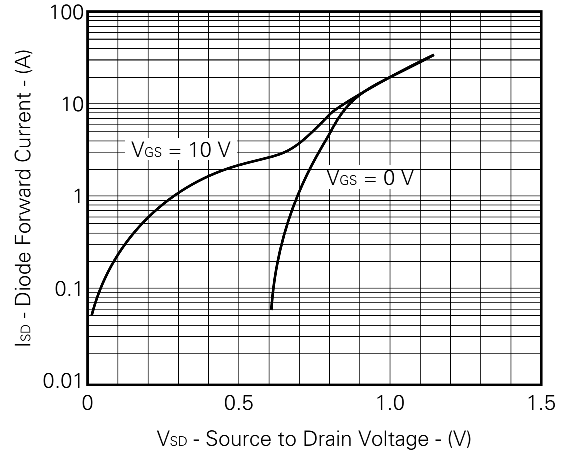



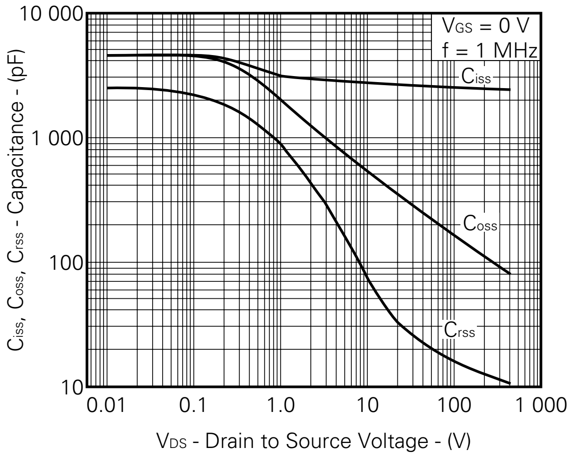
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



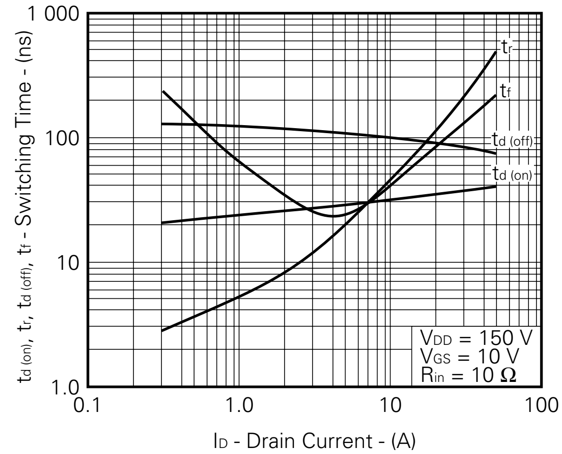

SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



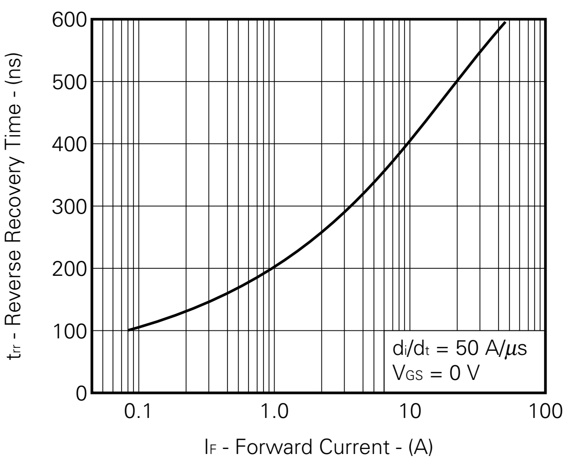

CAPACITANCE vs. DRAIN TO
SOURCE VOLTAGE



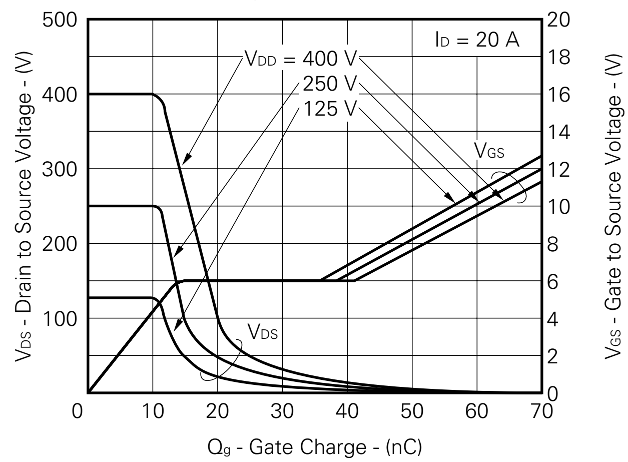

SWITCHING CHARACTERISTICS



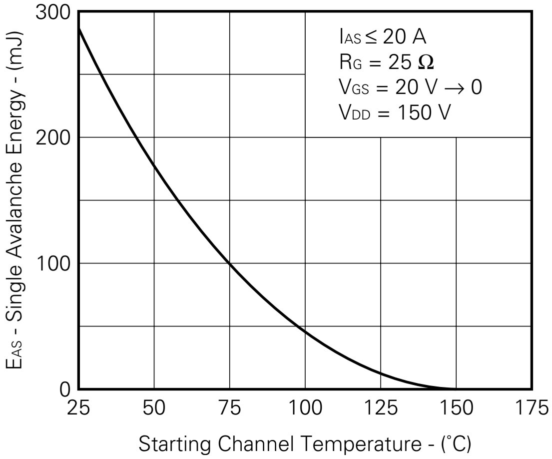

REVERSE RECOVERY TIME vs.
REVERSE DRAIN CURRENT



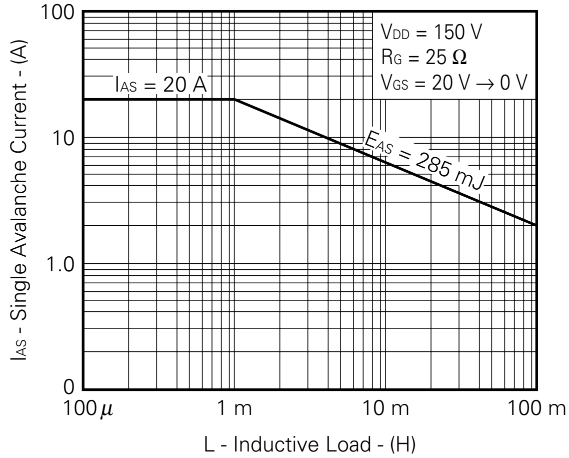

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE




SINGLE AVALANCHE ENERGY vs.
INDUCTIVE LOAD



## REFERENCE

| Document Name | Document No. |
|---|---|
| NEC semiconductor device reliability/quality control system. | TEI-1202 |
| Quality grade on NEC semiconductor devices. | IEI-1209 |
| Semiconductor device mounting technology manual. | IEI-1207 |
| Semiconductor device package manual. | IEI-1213 |
| Guide to quality assurance for semiconductor devices. | MEI-1202 |
| Semiconductor selection guide. | MF-1134 |
| Power MOS FET features and application switching power supply. | TEA-1034 |
| Application circuits using Power MOS FET. | TEA-1035 |
| Safe operating area of Power MOS FET. | TEA-1037 |

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]