

## General Description

The MIC5333 is a tiny dual low quiescent current LDO ideal for applications that are power sensitive. The MIC5333 integrates two high performance, 300mA LDOs, and a POR generator for each LDO into a 2.5mm x 2.5mm Thin MLF® package, which occupies less PC board area than a single SOT-23 package.

The MIC5333 is designed to reject input noise and provide low output noise with fast transient response to respond to any load change quickly even though it is a low quiescent current part. This combination of PSRR, low noise and transient response along with low power consumption makes for a very high performance, yet general purpose product.

The MIC5333 is a  $\mu$ Cap design, operating with very small ceramic output capacitors, which reduces required board space and component cost; and it is available in fixed output voltages in the tiny 10-pin 2.5mm x 2.5mm Thin MLF® leadless package.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

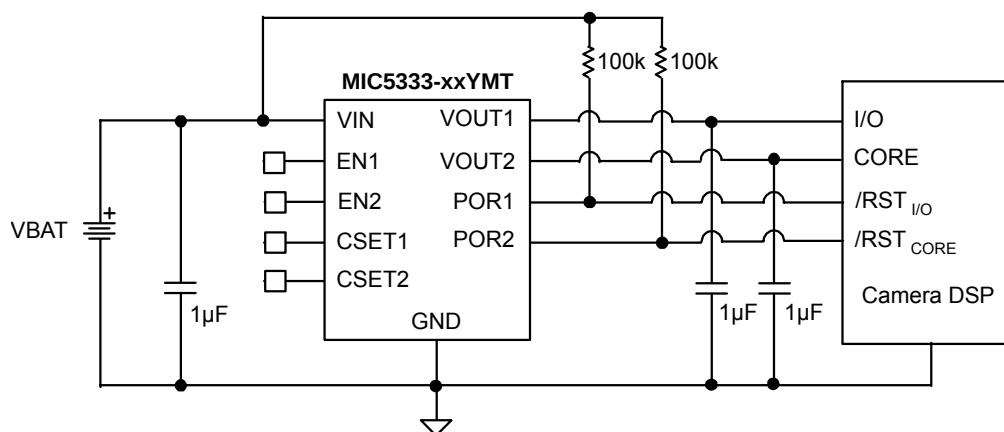
## Features

- 2.3V to 5.5V input voltage range
- 300mA output current per LDO
- Very low quiescent current: 25 $\mu$ A per LDO
- POR output with programmable delay for each LDO
- High PSRR – >65dB on each LDO
- Stable with 1 $\mu$ F ceramic output capacitors
- Tiny 10-pin 2.5mm x 2.5mm Thin MLF® package
- Ultra-low dropout voltage – 120mV @ 300mA
- Low output voltage noise – 50 $\mu$ Vrms
- Thermal shutdown protection
- Current limit protection

## Applications

- Camera phones
- Mobile phones
- PDAs
- GPS receivers
- Portable devices

## Typical Application



**Camera DSP Power Supply Circuit**

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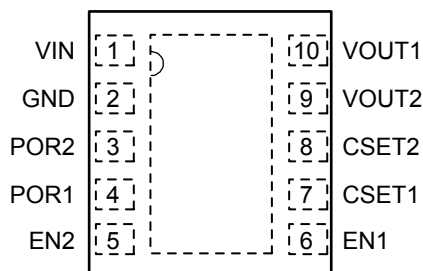
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**Ordering Information**

| Part Number          | Manufacturing Part Number | Marking | Voltage     | Junction Temperature Range | Package                    |
|----------------------|---------------------------|---------|-------------|----------------------------|----------------------------|
| MIC5333-2.5/1.2YMT   | MIC5333-J4YMT             | XJ4     | 2.5V/1.2V   | −40° to +125°C             | 10-Pin 2.5 x 2.5 Thin MLF® |
| MIC5333-2.8/2.8YMT   | MIC5333-MMYMT             | XMM     | 2.8V/2.8V   | −40° to +125°C             | 10-Pin 2.5 x 2.5 Thin MLF® |
| MIC5333-2.8/2.85YMT  | MIC5333-MNYMT             | XMN     | 2.8V/2.85V  | −40° to +125°C             | 10-Pin 2.5 x 2.5 Thin MLF® |
| MIC5333-2.85/2.85YMT | MIC5333-NNYMT             | XNN     | 2.85V/2.85V | −40° to +125°C             | 10-Pin 2.5 x 2.5 Thin MLF® |
| MIC5333-3.0/2.8YMT   | MIC5333-PMYMT             | XPM     | 3.0V/2.8V   | −40° to +125°C             | 10-Pin 2.5 x 2.5 Thin MLF® |
| MIC5333-3.0/2.85YMT  | MIC5333-PNYMT             | XPN     | 3.0V/2.85V  | −40° to +125°C             | 10-Pin 2.5 x 2.5 Thin MLF® |
| MIC5333-3.0/3.0YMT   | MIC5333-PPYMT             | XPP     | 3.0V/3.0V   | −40° to +125°C             | 10-Pin 2.5 x 2.5 Thin MLF® |

**Note:** Other voltage options available. Contact Micrel for details.

## Pin Configuration



**10-Pin 2.5mm x 2.5mm Thin MLF® (MT)**  
**(Top View)**

## Pin Description

| Pin Number | Pin Name | Pin Function                                                                                                                                                                    |
|------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | VIN      | Supply Input.                                                                                                                                                                   |
| 2          | GND      | Ground.                                                                                                                                                                         |
| 3          | POR2     | Power-On Reset Output (Regulator 2): Open-drain output. Active low indicates an output under-voltage condition on regulator 2 when the device is enabled.                       |
| 4          | POR1     | Power-On Reset Output (Regulator 1): Open-drain output. Active low indicates an output under-voltage condition on regulator 1 when the device is enabled.                       |
| 5          | EN2      | Enable Input (Regulator 2): Active High Input. Logic High = On; Logic Low = Off. Do not leave floating.                                                                         |
| 6          | EN1      | Enable Input (Regulator 1): Active High Input. Logic High = On; Logic Low = Off. Do not leave floating.                                                                         |
| 7          | CSET1    | Delay Set Input (Regulator 1): Connect external capacitor to GND to set the internal delay for the POR1 output. When left open, there is no delay. This pin cannot be grounded. |
| 8          | CSET2    | Delay Set Input (Regulator 2): Connect external capacitor to GND to set the internal delay for the POR2 output. When left open, there is no delay. This pin cannot be grounded. |
| 9          | VOUT2    | Regulator Output – LDO2.                                                                                                                                                        |
| 10         | VOUT1    | Regulator Output – LDO1.                                                                                                                                                        |

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|                                                |                                   |
|------------------------------------------------|-----------------------------------|
| Supply Voltage ( $V_{IN}$ )                    | 0V to +6V                         |
| Enable Input Voltage ( $V_{EN1}$ , $V_{EN2}$ ) | 0V to $V_{IN}$                    |
| POR Voltage ( $V_{POR1}$ , $V_{POR2}$ )        | 0V to +6V                         |
| Power Dissipation                              | Internally Limited <sup>(3)</sup> |
| Lead Temperature (soldering, 3sec.)            | 260°C                             |
| Storage Temperature ( $T_s$ )                  | -65°C to +150°C                   |
| ESD Sensitive <sup>(4)</sup>                   |                                   |

**Operating Ratings<sup>(2)</sup>**

|                                                |                 |
|------------------------------------------------|-----------------|
| Supply Voltage ( $V_{IN}$ )                    | +2.3V to +5.5V  |
| Enable Input Voltage ( $V_{EN1}$ , $V_{EN2}$ ) | 0V to $V_{IN}$  |
| POR Voltage ( $V_{POR1}$ , $V_{POR2}$ )        | 0V to +5.5V     |
| Junction Temperature ( $T_J$ )                 | -40°C to +125°C |
| Junction Thermal Resistance                    |                 |
| 2.5mm x 2.5mm Thin MLF-10 ( $\theta_{JA}$ )    | 75°C/W          |

**Electrical Characteristics<sup>(5)</sup>**

$V_{IN} = V_{EN1} = V_{EN2} = V_{OUT} + 1.0V$ , higher of the two regulator outputs;  $I_{OUT1} = I_{OUT2} = 100\mu A$ ;  $C_{OUT1} = C_{OUT2} = 1\mu F$ ;  
 $T_J = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_J \leq +125^\circ C$ ; unless noted.

| Parameter                       | Condition                                                                        | Min         | Typ  | Max         | Units         |
|---------------------------------|----------------------------------------------------------------------------------|-------------|------|-------------|---------------|
| Output Voltage Accuracy         | Variation from nominal $V_{OUT}$                                                 | -1.0        |      | +1.0        | %             |
|                                 | Variation from nominal $V_{OUT}$ ; -40°C to +125°C                               | <b>-2.0</b> |      | <b>+2.0</b> | %             |
| Line Regulation                 | $V_{IN} = V_{OUT} + 1V$ to 5.5V; $I_{OUT} = 100\mu A$                            |             | 0.02 | 0.3         | %/V           |
|                                 |                                                                                  |             |      | <b>0.6</b>  | %/V           |
| Load Regulation                 | $I_{OUT} = 100\mu A$ to 300mA                                                    |             | 0.2  | 0.5         | %             |
| Dropout Voltage                 | $I_{OUT} = 50mA$                                                                 |             | 20   | <b>40</b>   | mV            |
|                                 | $I_{OUT} = 300mA$                                                                |             | 120  | <b>240</b>  | mV            |
| Ground Current                  | $V_{EN1} = \text{High}$ ; $V_{EN2} = \text{Low}$ ; $I_{OUT} = 100\mu A$ to 300mA |             | 25   | <b>50</b>   | $\mu A$       |
|                                 | $V_{EN1} = \text{Low}$ ; $V_{EN2} = \text{High}$ ; $I_{OUT} = 100\mu A$ to 300mA |             | 25   | <b>50</b>   | $\mu A$       |
|                                 | $V_{EN1} = V_{EN2} = \text{High}$ ; $I_{OUT1} = 300mA$ , $I_{OUT2} = 300mA$      |             | 40   | <b>75</b>   | $\mu A$       |
| Ground Current in Shutdown      | $V_{EN1} = V_{EN2} \leq 0.2V$                                                    |             | 0.01 | 1.0         | $\mu A$       |
| Ripple Rejection                | $f = 1kHz$ ; $C_{OUT} = 2.2\mu F$                                                |             | 65   |             | dB            |
|                                 | $f = 20kHz$ ; $C_{OUT} = 2.2\mu F$                                               |             | 45   |             | dB            |
| Current Limit                   | $V_{OUT} = 0V$                                                                   | 350         | 550  | 800         | mA            |
| Output Voltage Noise            | $C_{OUT} = 1\mu F$ ; 10Hz to 100kHz                                              |             | 50   |             | $\mu V_{RMS}$ |
| <b>Enable Inputs (EN1/EN2 )</b> |                                                                                  |             |      |             |               |
| Enable Input Voltage            | Logic Low                                                                        |             |      | <b>0.2</b>  | V             |
|                                 | Logic High                                                                       | <b>1.2</b>  |      |             | V             |
| Enable Input Current            | $V_{IL} \leq 0.2V$                                                               |             | 0.01 | <b>1.0</b>  | $\mu A$       |
|                                 | $V_{IH} \geq 1.2V$                                                               |             | 0.01 | <b>1.0</b>  | $\mu A$       |
| <b>Turn-on Time</b>             |                                                                                  |             |      |             |               |
| Turn-on Time (LDO1 and 2)       | $C_{OUT} = 1\mu F$ (Enable of First LDO)                                         |             | 140  | <b>500</b>  | $\mu s$       |
|                                 | $C_{OUT} = 1\mu F$ (Enable of Second LDO after First Enabled)                    |             | 110  | <b>500</b>  | $\mu s$       |
| <b>POR1/POR2 Output</b>         |                                                                                  |             |      |             |               |
| $V_{TH}$                        | Low Threshold, % of $V_{OUT}$ (POR ON)                                           | 88          |      |             | %             |
|                                 | High Threshold, % of $V_{OUT}$ (POR OFF)                                         |             |      | 98          | %             |
| $V_{OL}$                        | POR Output Logic Low Voltage; $I_L = 250\mu A$                                   |             | 0.02 | <b>0.1</b>  | V             |
| $I_{POR}$                       | POR Leakage Current, POR OFF                                                     | <b>-1.0</b> | 0.01 | <b>+1.0</b> | $\mu A$       |

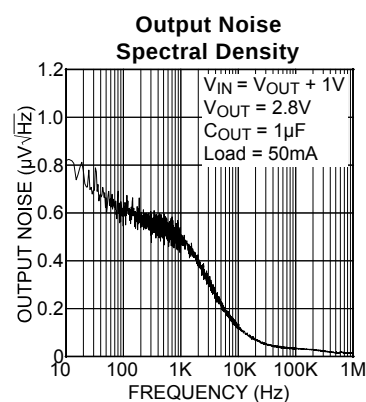
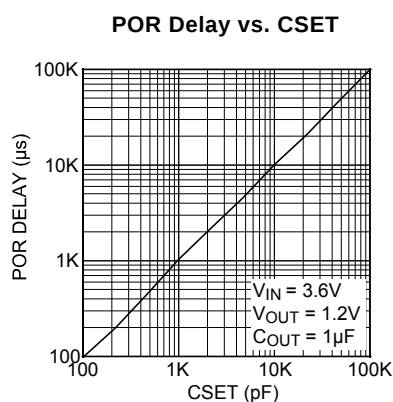
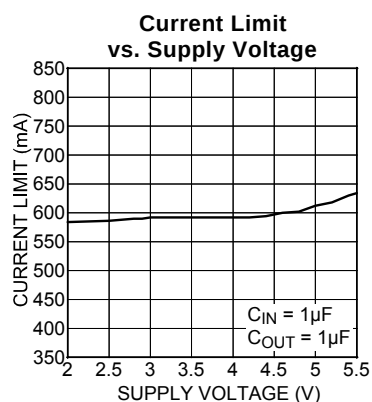
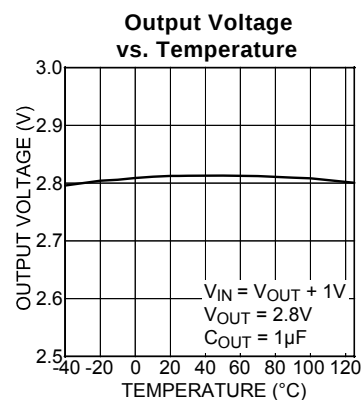
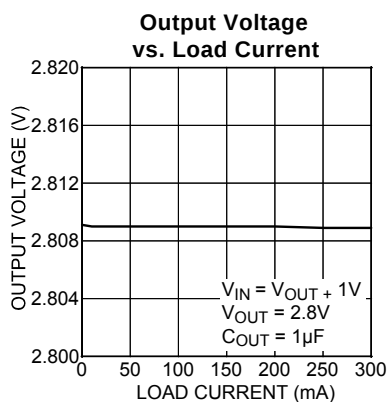
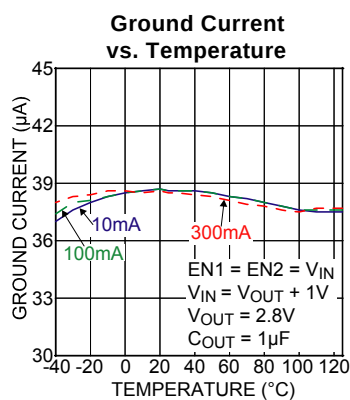
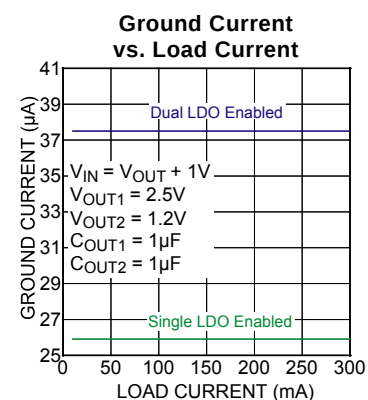
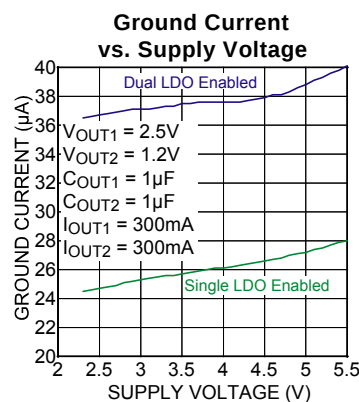
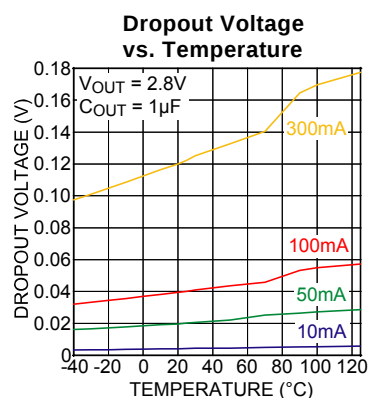
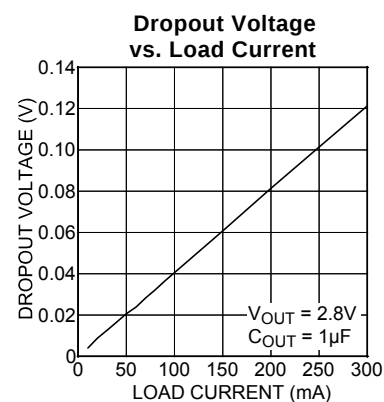
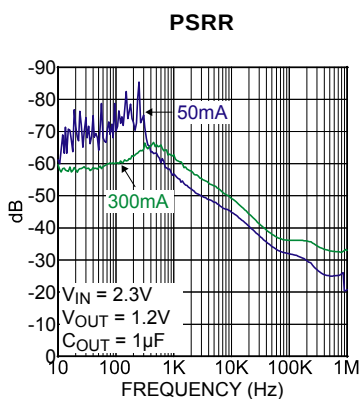
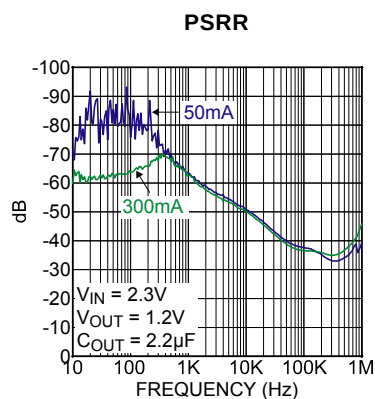
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| Parameter                  | Condition       | Min         | Typ  | Max         | Units   |
|----------------------------|-----------------|-------------|------|-------------|---------|
| <b>CSET1/CSET2 INPUT</b>   |                 |             |      |             |         |
| CSET Pin Current Source    | $V_{CSET} = 0V$ | <b>0.8</b>  | 1.4  | <b>2</b>    | $\mu A$ |
| CSET Pin Threshold Voltage | POR = High      | <b>1.21</b> | 1.25 | <b>1.29</b> | V       |

**Notes:**

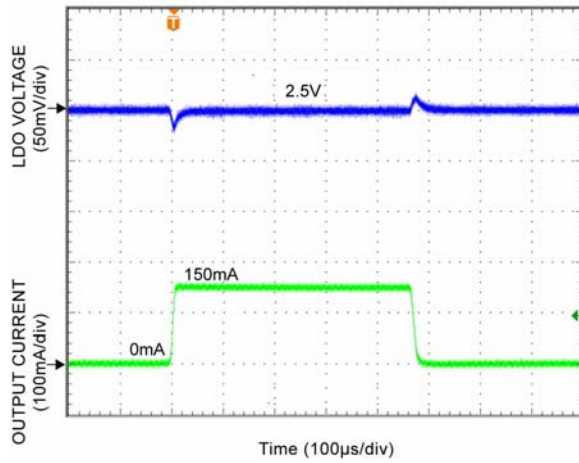
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any  $T_A$  (ambient temperature) is  $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k $\Omega$  in series with 100pF.
5. Specification for packaged product only.

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Typical Characteristics

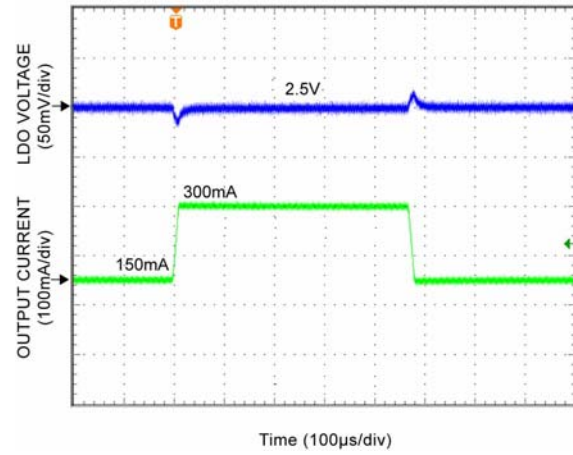


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Functional Characteristics

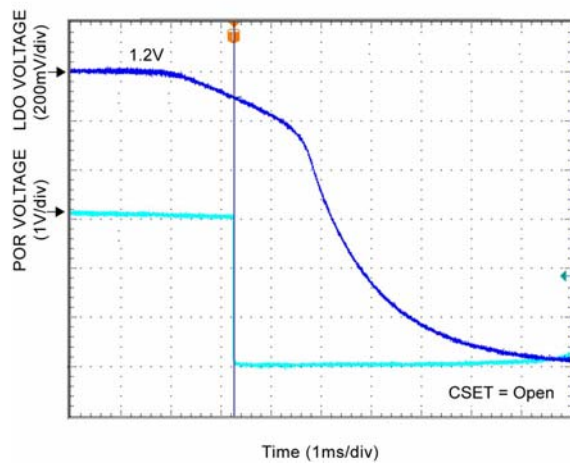
Load Transient (0mA-150mA)



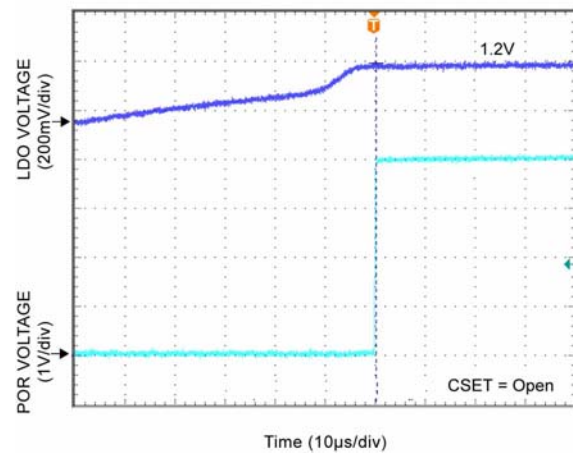
Load Transient (150mA-300mA)



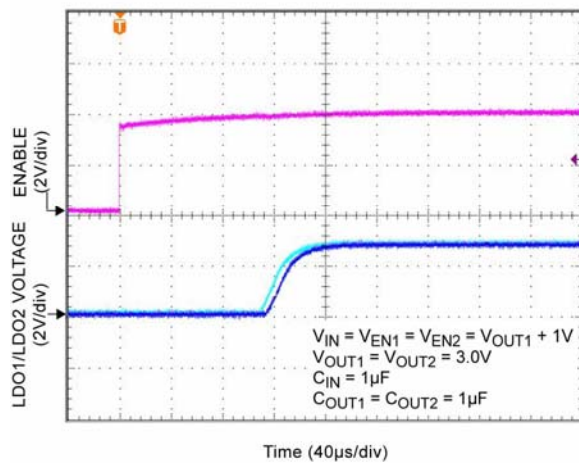
POR Signal (High-Low)



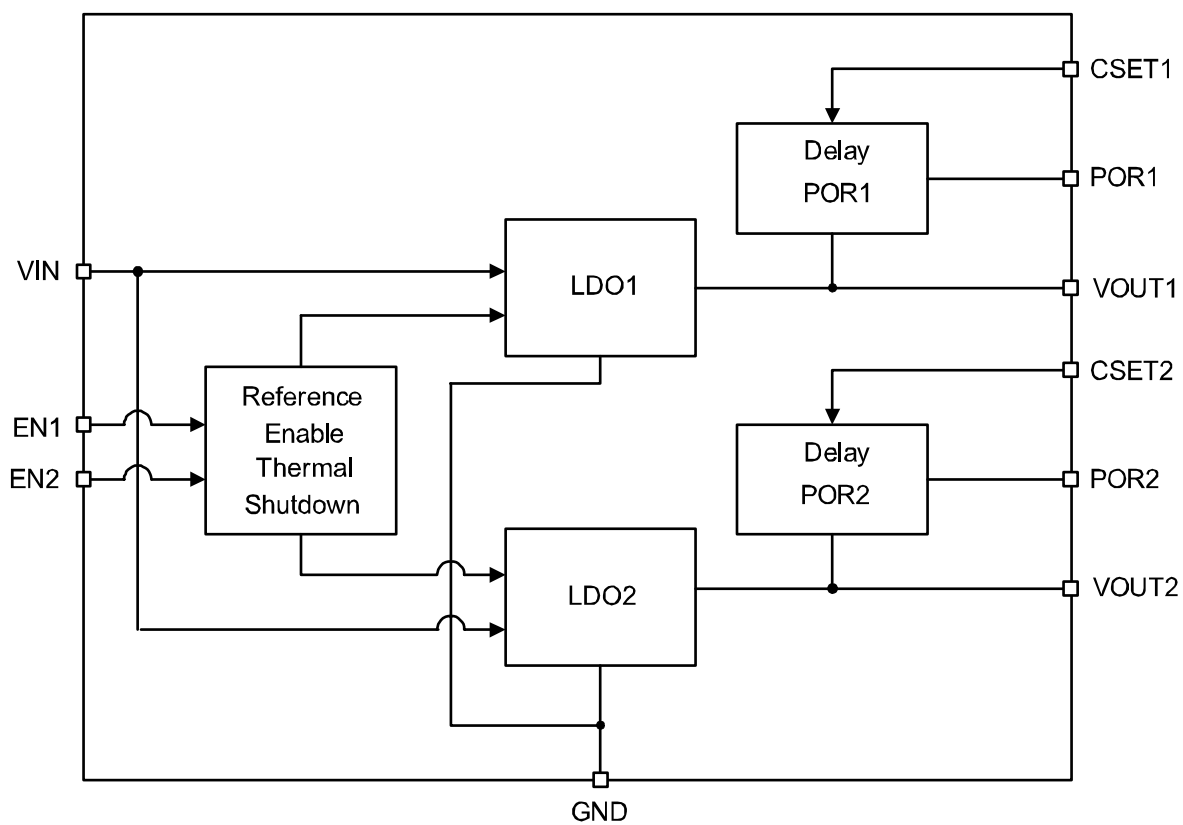
POR Signal (Low-High)



Enable Turn-On



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**Functional Diagram**



**MIC5333 Block Diagram**

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## Application Information

MIC5333 is a dual 300mA LDO, with an integrated Power On Reset (POR) for each of the regulators. The MIC5333 regulator is fully protected from damage due to fault conditions, offering linear current limiting and thermal shutdown.

### Input Capacitor

The MIC5333 is a high-performance, high bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 1 $\mu$ F capacitor is required from the input to ground to provide stability. Low-ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high-frequency capacitors, such as small-valued NPO dielectric-type capacitors, help filter out high-frequency noise and are good practice in any RF-based circuit. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

### Output Capacitor

The MIC5333 requires an output capacitor of 1 $\mu$ F or greater to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 1 $\mu$ F ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

### No-Load Stability

Unlike many other voltage regulators, the MIC5333 will remain stable and in regulation with no load. This is especially important in CMOS RAM keep-alive applications.

### Enable/Shutdown

The MIC5333 comes with dual active-high enable pins that allow each regulator to be disabled independently. Forcing the enable pin low disables the regulator and sends it into a “zero” off-mode-current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage.

The active-high enable pin uses CMOS technology and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

### Power On Reset

Each of the regulator outputs has a Power On Reset status pin (POR1/POR2). This pin is an open drain output. When an LDO is enabled an active low POR indicates an under voltage condition on  $V_{OUT}$ .

Each POR status signal can be programmed for a delay of 1sec/ $\mu$ F by placing a capacitor from its associated CSET pin to ground. Where the CSET1 pin sets the delay for the POR1 output and the CSET2 pin sets the delay for the POR2 output. Zero delay is added by leaving the CSET1/2 pin open circuit.

### Thermal Considerations

The MIC5333 is designed to provide 300mA of continuous current for both outputs in a very small package. Maximum ambient operating temperature can be calculated based on the output current and the voltage drop across the part. For example if the input voltage is 3.6V, the output voltage is 3.0V for  $V_{OUT1}$ , 2.8V for  $V_{OUT2}$  and the output current = 300mA. The actual power dissipation of the regulator circuit can be determined using the equation:

$$P_D = (V_{IN} - V_{OUT1}) I_{OUT1} + (V_{IN} - V_{OUT2}) I_{OUT2} + V_{IN} I_{GND}$$

Because this device is CMOS and the ground current is typically <100 $\mu$ A over the load range, the power dissipation contributed by the ground current is <1% and can be ignored for this calculation.

$$P_D = (3.6V - 3.0V) \times 300mA + (3.6V - 2.8) \times 300mA$$

$$P_D = 0.42W$$

To determine the maximum ambient operating temperature of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

$$P_{D(MAX)} = \left( \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \right)$$

$T_{J(max)} = 125^\circ\text{C}$ , and the maximum junction temperature of the die,  $\theta_{JA}$ , thermal resistance =  $75^\circ\text{C/W}$ .

Substituting  $P_D$  for  $P_{D(max)}$  and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit. The junction-to-ambient thermal resistance for the minimum footprint is  $75^\circ\text{C/W}$ .

The maximum power dissipation must not be exceeded for proper operation.

For example, when operating the MIC5333-PMYMT at an input voltage of 3.6V and 300mA loads at each output with a minimum footprint layout, the maximum ambient operating temperature  $T_A$  can be determined as follows:

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$$0.42\text{W} = (125^{\circ}\text{C} - T_A) / (75^{\circ}\text{C/W})$$

$$T_A = 93.5^{\circ}\text{C}$$

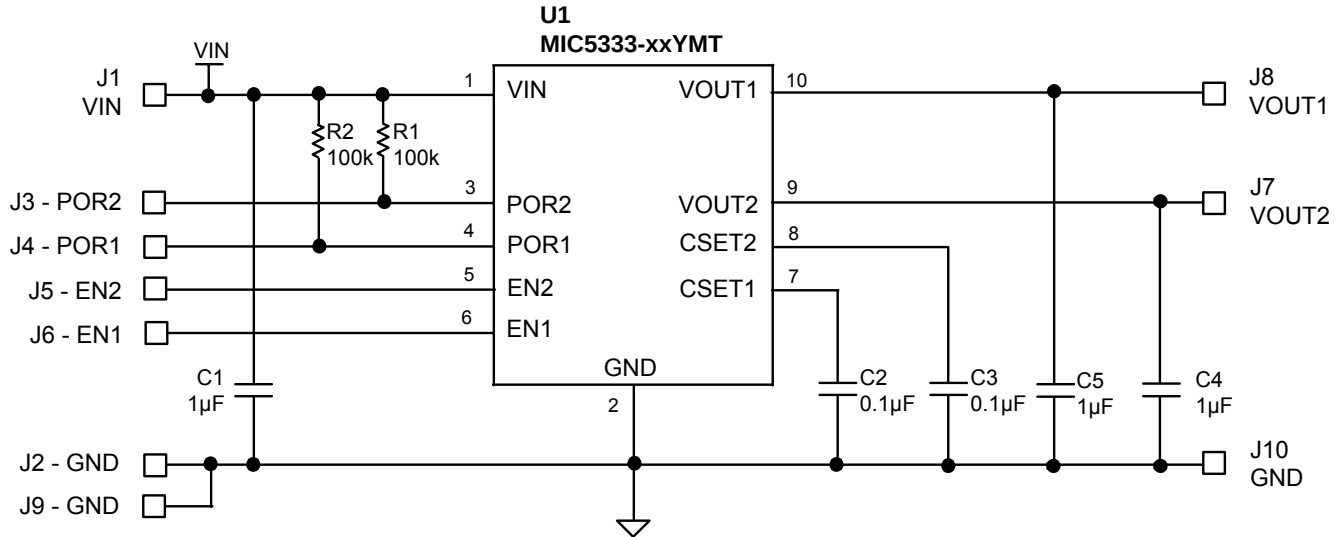
Therefore, a 3.0V/2.8V application with 300mA at each output current can accept an ambient operating temperature of 93.5°C in a 2.5mm x 2.5mm MLF<sup>®</sup> package. For a full discussion of heat sinking and

thermal effects on voltage regulators, refer to the "Regulator Thermals" section of *Micrel's Designing with Low-Dropout Voltage Regulators* handbook. This information can be found on Micrel's website at:

[http://www.micrel.com/\\_PDF/other/LDOBk\\_ds.pdf](http://www.micrel.com/_PDF/other/LDOBk_ds.pdf)

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## MIC5333 Typical Application Circuit



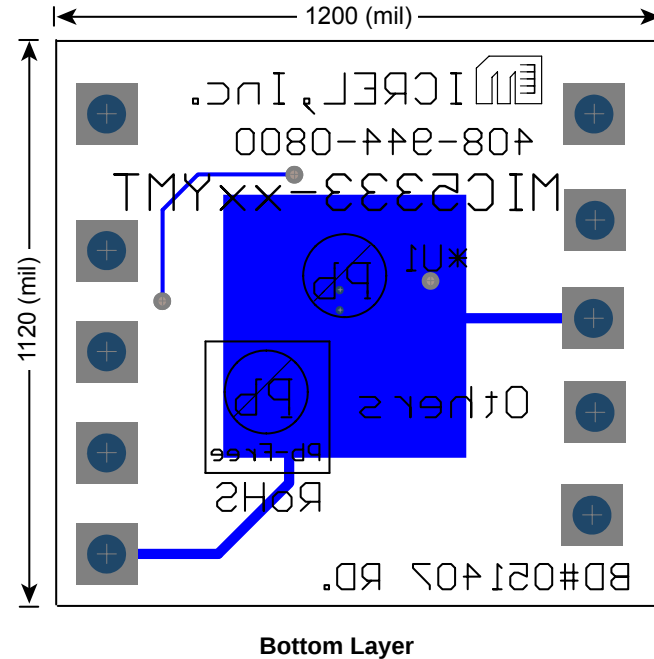
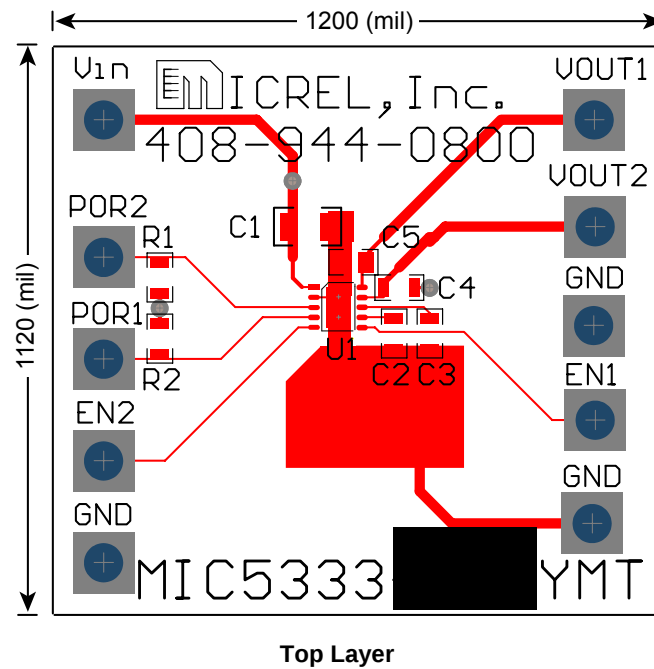
## Bill of Materials

| Item       | Part Number      | Manufacturer          | Description                                                 | Qty |
|------------|------------------|-----------------------|-------------------------------------------------------------|-----|
| C1, C4, C5 | C1608X5R0J105K   | TDK <sup>(1)</sup>    | Capacitor, 1µF Ceramic, 6.3V, X5R, Size 0603                | 3   |
| C2, C3     | VJ0603Y104KXXAT  | Vishay <sup>(2)</sup> | Capacitor, 0.1µF Ceramic, 10V, X7R, Size 0603               | 2   |
| R1, R2     | CRCW06031003FRT1 | Vishay <sup>(2)</sup> | Resistor, 100kΩ, 1%, 1/16W, Size 0603                       | 2   |
| U1         | MIC5333-XXYMT    | Micrel <sup>(3)</sup> | UCAP LDO, Dual 300mA with dual POR, 2.5mm x 2.5mm Thin MLF® | 1   |

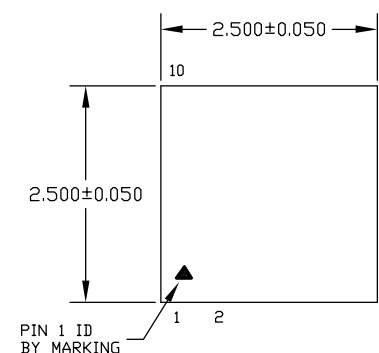
### Notes:

1. TDK: [www.tdk.com](http://www.tdk.com)
2. Vishay: [www.vishay.com](http://www.vishay.com)
3. Micrel, Inc.: [www.micrel.com](http://www.micrel.com)

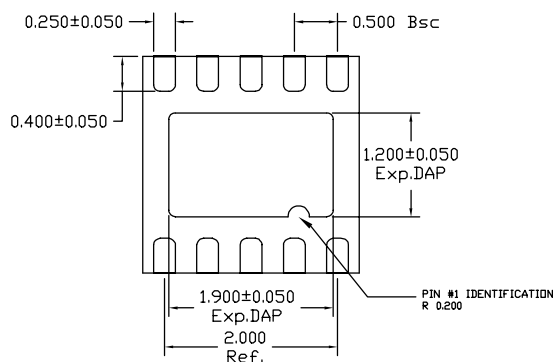
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**PCB Layout Recommendations**



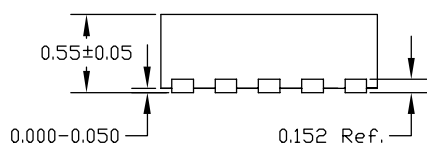
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**Package Information**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

## NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.08 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID WILL BE LASER MARKED.

**10-Pin 2.5mm x 2.5mm Thin MLF<sup>®</sup> (MT)**

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