CMOS programmable electrically erasable logic device

PL22V10-10

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FEATURES

- Advanced CMOS EEPROM technology
- Ultra high performance
  - 10ns, (t_{PD}) commercial version
  - f_{MAX} as fast as 83.3MHz
- Available in Dual In-Line, Small Outline Large, and Plastic Leaded Chip Carrier packages
- Low power consumption
  - 110mA + 0.5mA/MHz max
- EE reprogrammability
  - Low-risk reprogrammable inventory
  - Superior programming and functional yield
  - 100% testable
  - Erases and programs in seconds
  - 100 guaranteed erase cycles
- Development and programming support
  - Third-party software and programmers
  - SLICE development software
- Architectural flexibility
  - 132 product term × 44 input AND array
  - Up to 22 inputs and 10 outputs
  - Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - Independently programmable 4-configuration I/O macrocells
  - Synchronous preset, asynchronous clear
  - Independently programmable output enables
- Application versatility
  - Pin-for-pin and JEDEC-file compatible with the bipolar AmPAL22V10, CMOS PALC22V10 and PEEL22CV10A

DESCRIPTION

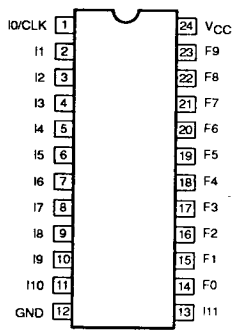
The Philips Semiconductors PL22V10-10 is a CMOS programmable electrically erasable logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to early generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PL22V10 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PL22V10 allows cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function. The PL22V10's flexible architecture offers complete function and JEDEC-file compatibility with the bipolar AmPAL22V10 and the CMOS PALC22V10. Applications for the PL22V10 include: replacement of random SSI/MSI logic circuitry and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PL22V10 is provided by Philips Semiconductors and third-party manufacturers.

PIN LABEL DESCRIPTIONS

I1 – I11	Dedicated Input
NC	Not Connected
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground

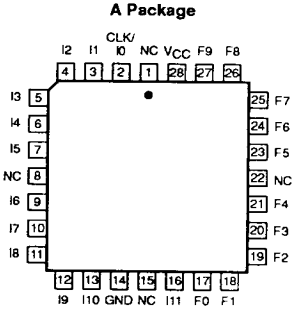
PIN CONFIGURATIONS

D and N Packages



N = Plastic Dual In-Line Package (300mil-wide)
D = Plastic Small Outline Large (300mil-wide) Package

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
24-Pin (300mil-wide) Plastic DIP (Dual-In-Line Package)	PL22V10–10N	0410D
28-Pin (300mil-wide) PLCC (Plastic Leaded Chip Carrier Package)	PL22V10–10A	0401F
24-Pin (300mil-wide) Plastic SOL (Small Outline Large) Package	PL22V10–10D	0173D

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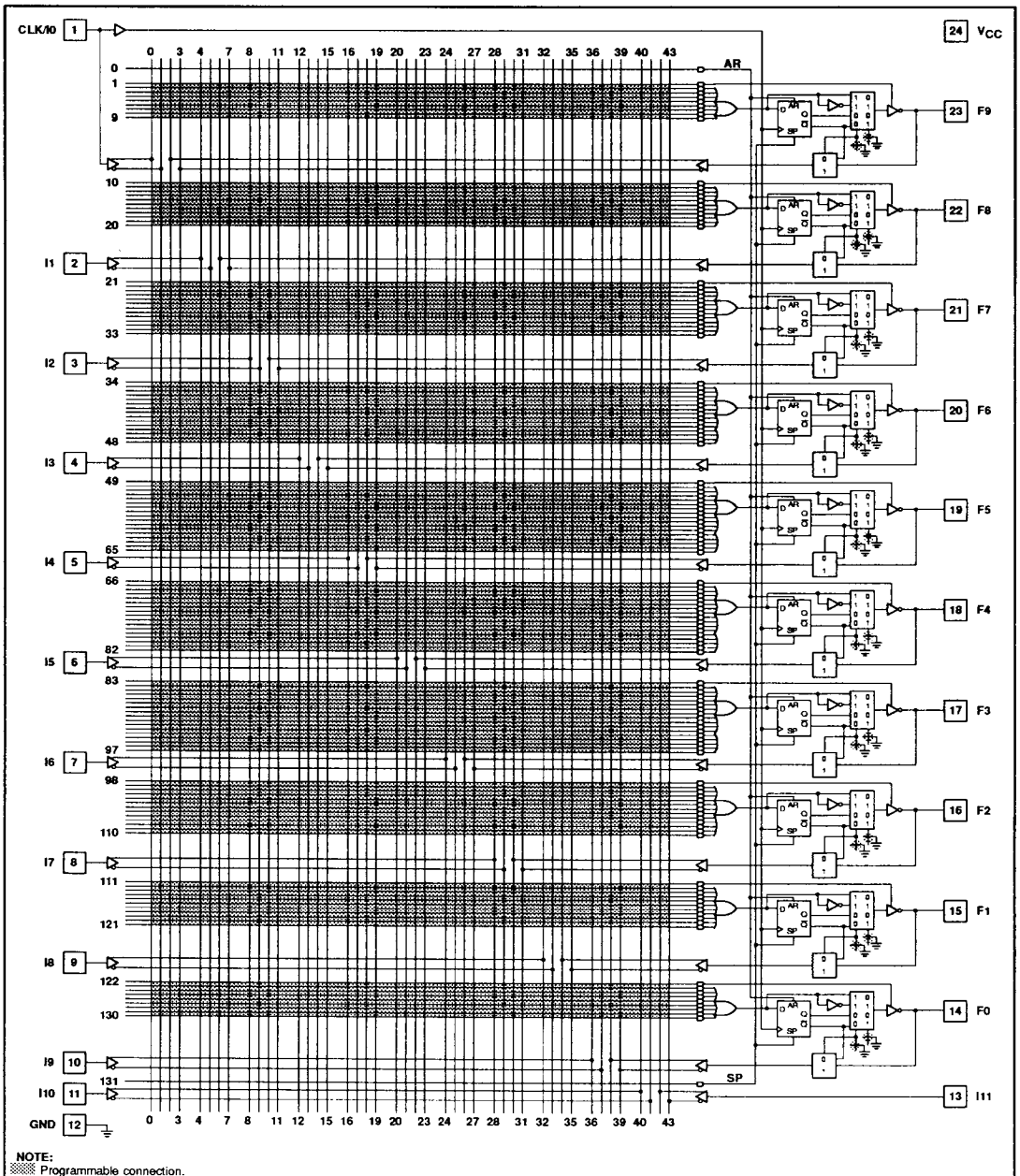
LOGIC DIAGRAM



NOTE:
▒ Programmable connection.

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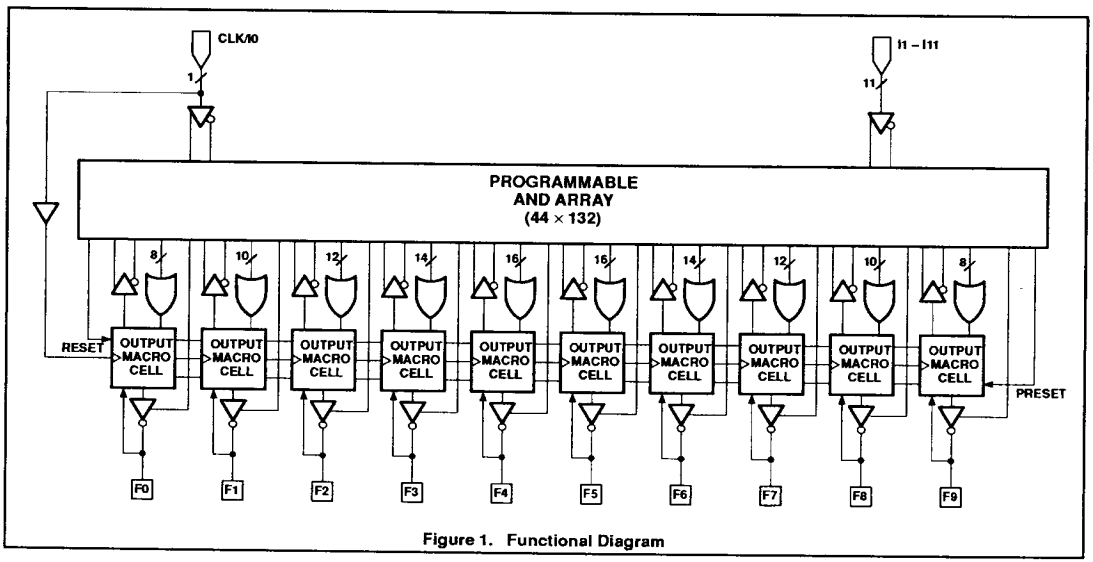

Figure 1. Functional Diagram

FUNCTION DESCRIPTION

The PL22V10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

ARCHITECTURE OVERVIEW

The PL22V10 architecture is illustrated in the Figure 1. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PL22V10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macro cell which can be independently programmed to one of 4 different configurations. The programmable macro cells allow each I/O to create sequential or combinatorial logic functions with either Active-High or Active-Low polarity.

AND/OR LOGIC ARRAY

The programmable AND array of the PL22V10 (shown in the Logic Diagram) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 input lines:

- 24 input lines carry the True and Complement of the signals applied to the 12 input pins
- 20 additional lines carry the True and Complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the True and Complement of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a Don't Care state exists and that term will always be TRUE.

When programming the PL22V10, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND array. (Note that EEPROM device programmers automatically program the connections on unused product terms so that they will have no effect on the output function.)

VARIABLE PRODUCT TERM DISTRIBUTION

The PL22V10 provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Logic Diagram). This distribution allows optimum use of device resources.

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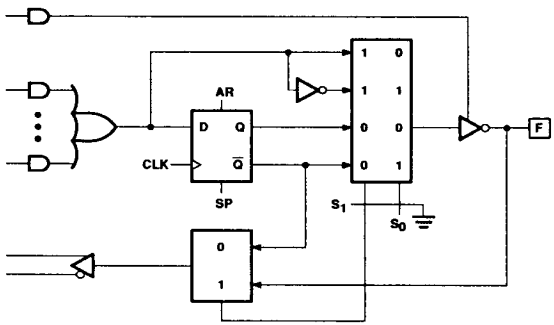
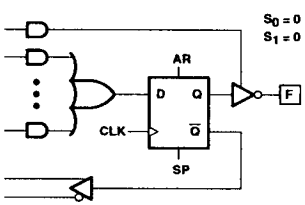


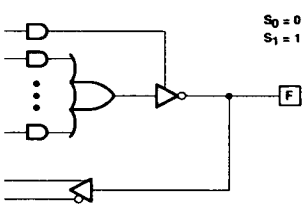
S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed fuse
1 = Programmed fuse

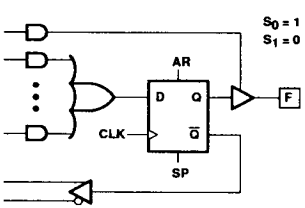
Figure 2. Output Macro Cell Logic Diagram



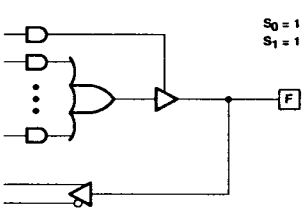
a. Registered/Active-LOW



c. Combinatorial/Active-LOW



b. Registered/Active-HIGH



d. Combinatorial/Active-HIGH

Figure 3.

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PROGRAMMABLE I/O MACROCELL

The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PL22V10 to the precise requirements of their designs.

MACROCELL ARCHITECTURE

Each I/O macrocell, as shown in Figure 2, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell of the PL22V10 is determined by the two EEPROM bits controlling these multiplexers. These bits determine output polarity, and output type (registered or non-registered). Equivalent circuits for the macrocell configurations are illustrated in Figure 3.

OUTPUT TYPE

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

PROGRAM/ERASE CYCLES

The PL22V10 is 100% testable, erases/programs in seconds, and has 100 guaranteed erase cycles.

OUTPUT POLARITY

Each macrocell can be configured to implement Active-High or Active-Low logic. Programmable polarity eliminates the need for external inverters.

OUTPUT ENABLE

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically FALSE and the I/O will function as a dedicated input.

REGISTER FEEDBACK SELECT

When the I/O macrocell is configured to implement a registered function (S1=0) (Figures 3.a or 3.b), the feedback signal to the AND array is taken from the $\overline{Q}$ output.

BI-DIRECTIONAL I/O SELECT

When configuring an I/O macrocell to implement a combinatorial function (S1=1) (Figures 3.c or 3.d), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input, a dedicated output, or a bi-directional I/O.

POWER-ON RESET

To ease system initialization, all flip-flops will power-up to a reset condition and the Q output will be low. The actual output of the PL22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 5µs maximum.

DESIGN SECURITY

The PL22V10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PL22V10 until the entire device has first been erased with the bulk-erase function.

PROGRAM AND ERASE

The PL22V10 can be programmed on standard logic programmers. If a device needs to be reprogrammed, simply place back into the programmer, at which point it will be automatically erased, then repatterned.

Approved programmers are listed in the Philips Semiconductors Programmer Reference Guide.

SOFTWARE SUPPORT

The PL22V10 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors' SNAP design software package. ABEL™, CUPL™, and PALASM® 90 design software packages also support the PL22V10 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PL22V10 logic designs can also be generated using the program table entry format. This program table entry format is supported by SNAP only.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATINGS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage	Relative to GND	–0.5	+7.0	V
V_{IN}, V_{OUT}	Voltage applied to any pin[3]	Relative to GND[2]	–1.2	V_{CC} + 0.5	V_{DC}
I_{OUT}	Output current	Per pin (I_{OL}, I_{OH})	±25		mA
T_{stg}	Storage temperature range		–65	+125	°C
T_{LT}	Lead temperature	Soldering 10 seconds	+300		°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Minimum DC input is –0.5V, however inputs may undershoot to –2.0V for periods less than 20ns.
3. V_{IN} and V_{OUT} are not specified for program/verify operation.

OPERATING RANGES

SYMBOL	PARAMETER	CONDITIONS	RATINGS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage	Commercial[1]	+4.75	+5.25	V_{DC}
		Industrial	+4.5	+5.5	V_{DC}
T_{amb}	Ambient temperature	Commercial[1]	0	+70	°C
		Industrial	–40	+85	°C
t_R	Clock Rise Time	See note 2		250	ns
t_F	Clock Fall Time	See note 2		250	ns
t_{RVCC}	V_{CC} Rise Time	See note 2		250	ms

NOTES:
1. Voltage applied to input or output must not exceed V_{CC} +0.3V.
2. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.

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DC ELECTRICAL CHARACTERISTICS

Commercial = 0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP[4]	MAX	
Input voltage						
V_{IL}	Low		–0.3		0.8	V
V_{IH}	High		2.0		V_{CC} + 0.3	V
Output voltage						
V_{OL}	Low – TTL	V_{CC} = MIN, I_{OL} = 16mA			0.5	V
V_{OLC}	Low – CMOS	V_{CC} = MIN, I_{OL} = 10µA			0.1	V
V_{OH}	High – TTL	V_{CC} = MIN, I_{OH} = –4.0mA	2.4			V
V_{OHC}	High – CMOS	V_{CC} = MIN, I_{OH} = –10µA	V_{CC} – 0.1			V
Input current						
I_{IL}/I_{IH}	Input leakage current	V_{CC} = MAX, GND ≤ V_{IN} ≤ V_{CC}		1	±10	µA
Output current						
I_{OZ}	Output leakage	I/O = Hi-Z, GND ≤ V_O ≤ V_{CC}		2	±10	µA
I_{SC}[5]	Short circuit	V_{CC} = 5V, V_{OUT} = 0.5V[1]	–30		–130	mA
I_{CC}	V_{CC} active current, CMOS (commercial)	V_{IN} = V_{CC} or GND[2, 3]		80 + 0.5mA/MHz	110 + 0.5mA/MHz	mA
	V_{CC} active current, CMOS (industrial)	V_{IN} = V_{CC} or GND[2, 3]		90 + 0.5mA/MHz	120 + 0.5mA/MHz	mA
	V_{CC} active current, TTL (commercial)	V_{IN} = V_{IL} or V_{IH}[2, 3]		90 + 0.5mA/MHz	120 + 0.5mA/MHz	mA
	V_{CC} active current, TTL (industrial)	V_{IN} = V_{IL} or V_{IH}[2, 3]		100 + 0.5mA/MHz	130 + 0.5mA/MHz	mA

NOTES:

1. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second.
2. I/O pins open (no load).
3. I_{CC} for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
4. Typical values are at V_{CC} = 5V. Typical values are guaranteed by design.
5. Room temperature only.

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AC ELECTRICAL CHARACTERISTICS

Commercial = $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$[1, 2]

SYMBOL	PARAMETER	TEST CONDITIONS	PL22V10-10 MIN	PL22V10-10 MAX	UNIT
t_{PD}	Input[3] to non-registered output	50pF		10	ns
t_{EA}	Input[3] to Output Enable[4]	50pF		10	ns
t_{ER}	Input[3] to Output Disable[4]	5pF		10	ns
t_{CO}	Clock to output	50pF		8	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback	50pF		14	ns
t_S	Input[3] or feedback setup to clock	50pF	7		ns
t_{SF}	Internal feedback[6]	50pF	5		ns
t_H	Input[3] hold after clock	50pF	0		ns
t_{WL}, t_{WH}	Clock width – clock low time, clock high time[5]	50pF	6		ns
t_{CP}	MIN clock period External ($t_S + t_{CO}$)	50pF	15		ns
f_{MAX1}	MAX operating frequency; Internal feedback[6] $\left(\frac{1}{t_{SF} + t_{CO}}\right)$	50pF	76.9		MHz
f_{MAX2}	MAX operating frequency; External ($1/t_{CP}$)	50pF	66.6		MHz
f_{MAX3}	MAX clock frequency; No feedback[6] $\left(\frac{1}{t_{WL} + t_{WH}}\right)$	50pF	83.3		MHz
t_{ARW}	Asynchronous Reset pulse width	50pF	10		ns
t_{AR}	Input[3] to Asynchronous Reset	50pF		12	ns
t_{ARR}	Asynchronous Reset recovery time	50pF	8		ns
t_{SPR}	Synchronous Preset recovery time	50pF	10		ns
t_{RESET}	Power-on reset time for registers in clear state[5]	50pF		5	µs
Capacitance[6]					
C_{IN}	Input Capacitance[7]	$T_{amb} = 25°C$, $V_{CC} = 5.0V$		6	pF
C_{OUT}	Output Capacitance[7]	@ f = 1MHz		12	pF

NOTES:

1. Test conditions assume: signal transition times of 2.5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
2. Device test loads are specified at the end of this section.
3. "Input" refers to an Input pin signal.
4. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
5. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
6. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
7. Capacitances are tested on a sample basis.

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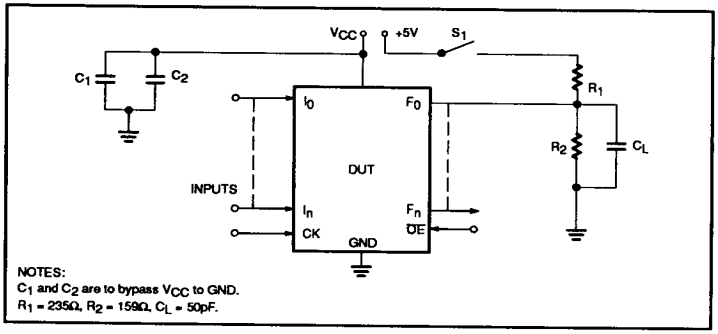
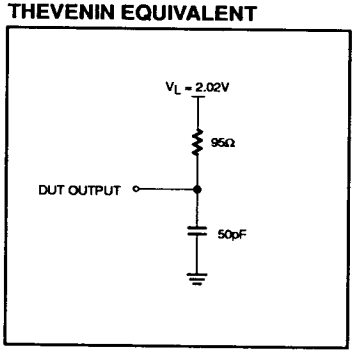
TEST LOAD CIRCUIT

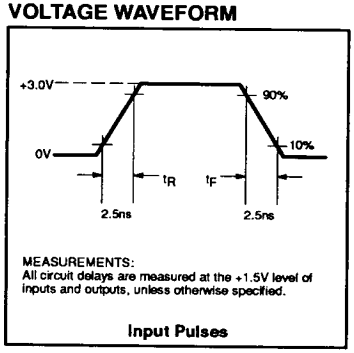


NOTES:
C_1 and C_2 are to bypass V_{CC} to GND.
R_1 = 235Ω, R_2 = 159Ω, C_L = 50pF.

THEVENIN EQUIVALENT



VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

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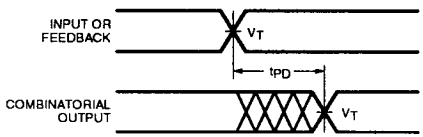
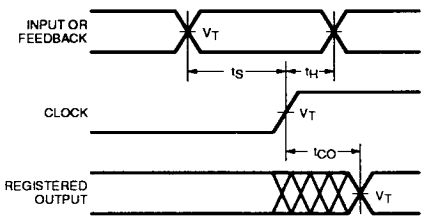
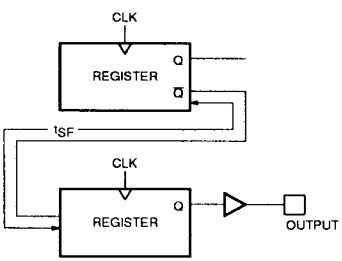
SWITCHING WAVEFORMS



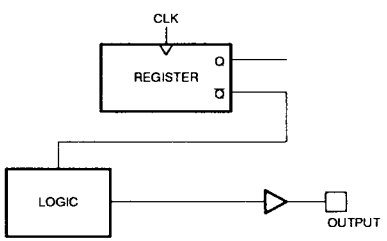
Combinatorial Output



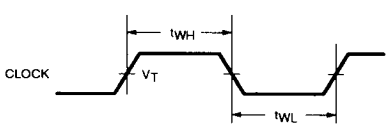
Registered Output



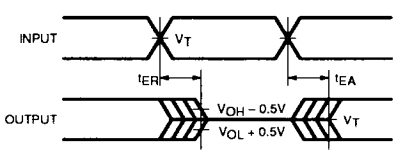
f_{MAX1}; Internal Feedback $\left(\frac{1}{t_{SF} + t_{CO}}\right)$



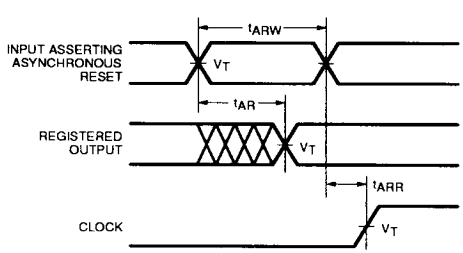
Clock to Combinatorial Output (t_{CO2})



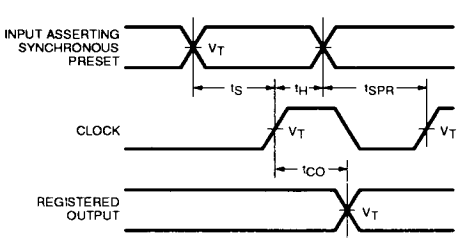
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

NOTES:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 2.5ns max.

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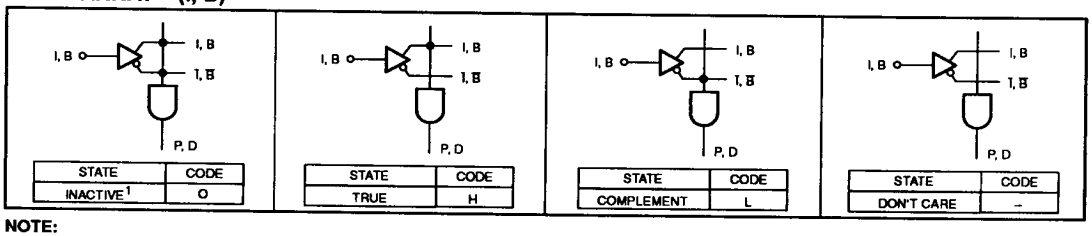
"AND" ARRAY – (I, B)



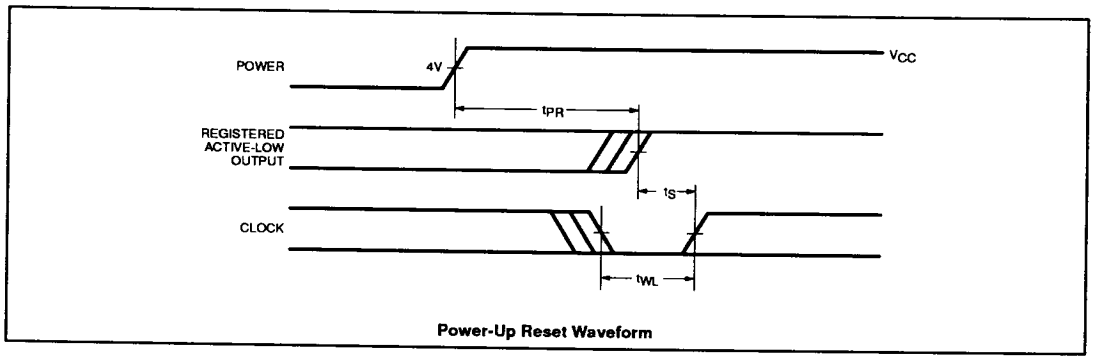
NOTE:
1. This is the initial state.

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{PR}	Power-up Reset Time		1	µs
t_S, t_{SF}	Input or Feedback Setup Time	See AC Electrical Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveform

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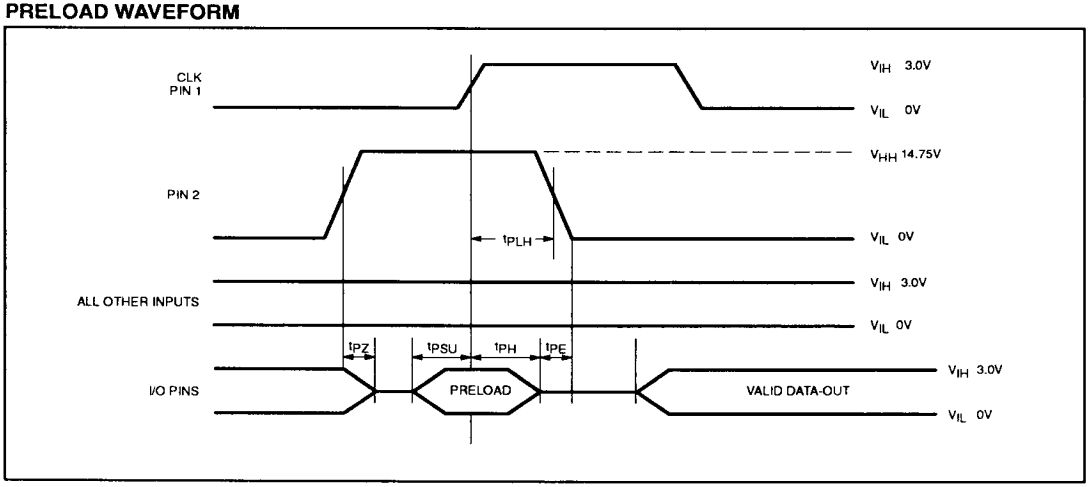
PRELOAD TEST CONDITION

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PE}	Valid data out			100		ns
t_{PZ}	Output 3-State delay time after assertion of Preload (Pin 2 = V_{HH})			100		ns
t_{PH}	Hold time of all preload inputs with respect to Clock rising edge			15		ns
t_{PSU}	Setup time of all preload inputs with respect to Clock rising edge			100		ns
t_{PLH}	Hold time for Preconditioning input			50		ns
V_{HH}	Preload enable voltage		14.50	14.75	15.0	V

PRELOAD WAVEFORM



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CMOS programmable electrically erasable logic device

PL22V10-10

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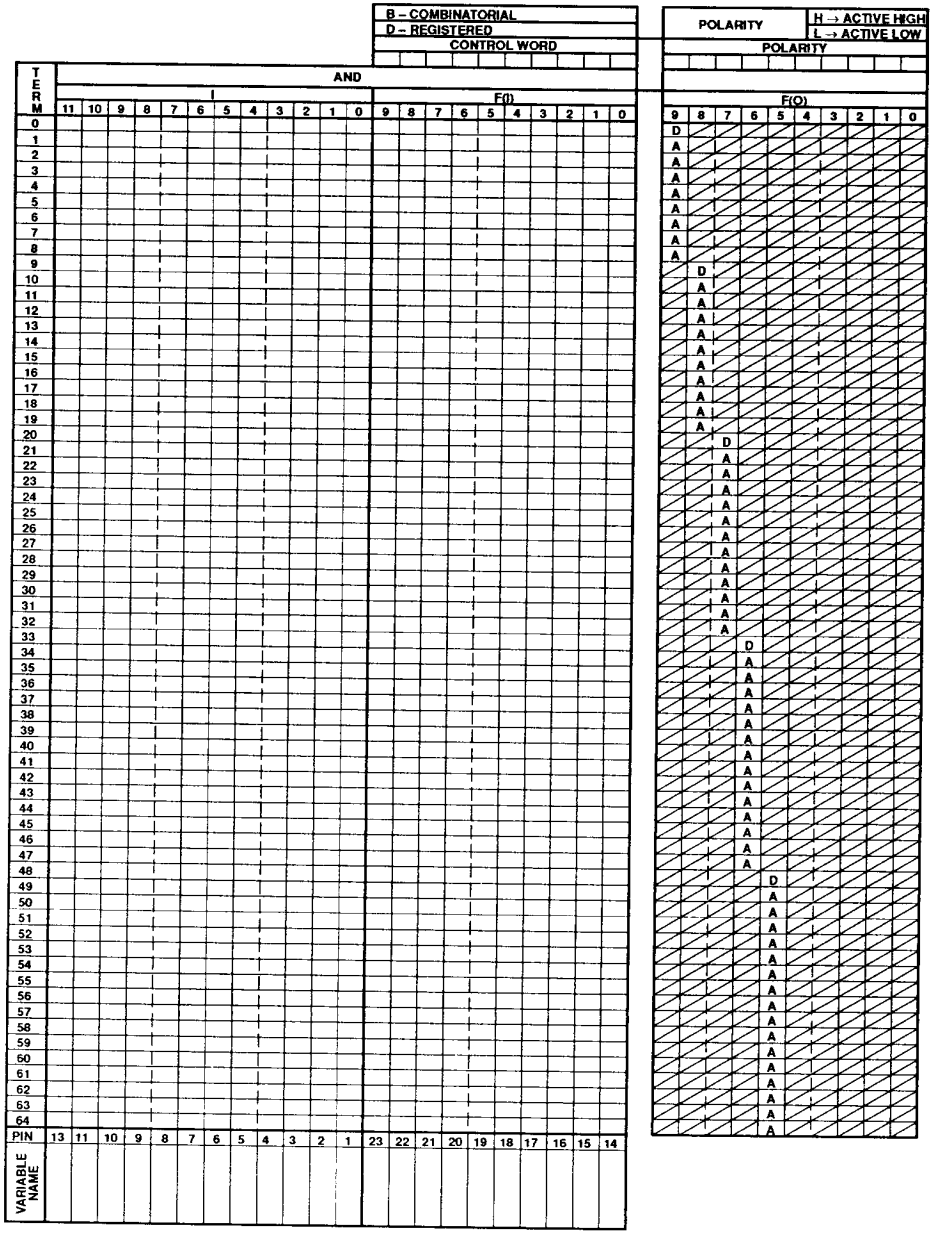
PROGRAM TABLE



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CMOS programmable electrically erasable logic device

PL22V10-10

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PROGRAM TABLE (Continued)

TERM	AND I 11	10	9	8	7	6	5	4	3	2	1	0	F(I) 9	8	7	6	5	4	3	2	1	0	F(O) 9	8	7	6	5	4	3	2	1	0
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128																																A
129																																A
AR																																
SP																																
PIN	13	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	15	14										
VARIABLE NAME																																

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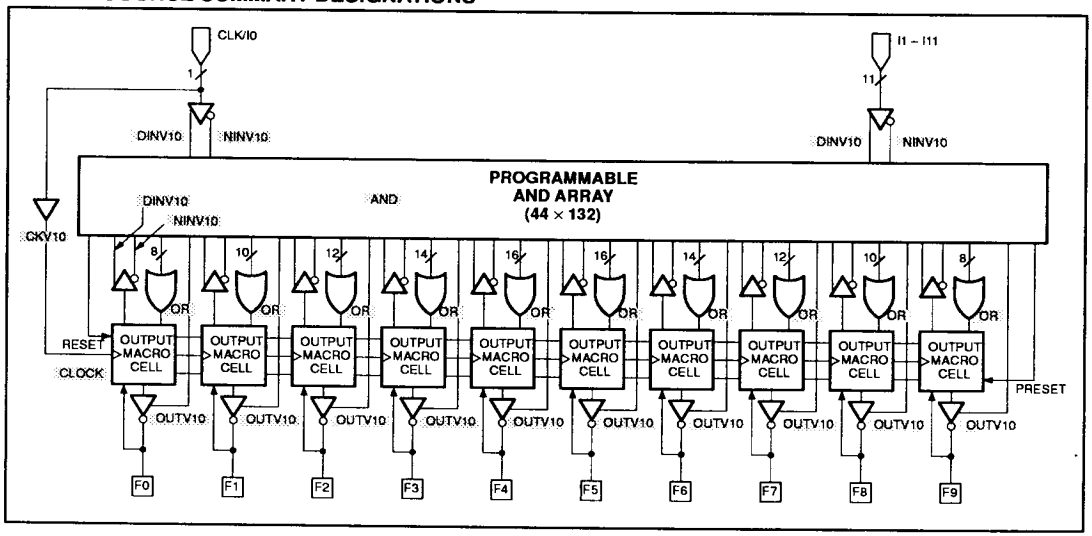
SNAP RESOURCE SUMMARY DESIGNATIONS



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