Freescale Semiconductor, Inc.

"MC145423EVK"

MC145423EVK/D
Rev. 3, 2/2002

Universal Digital Loop Transceiver (UDLT-3) Evaluation Module

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This module was designed to simplify the evaluation and design-in of the MC145423. The MC145423 combines the functionality of the UDLT-1 and UDLT-2—both master and slave.

By configuring this device via the three control pins, FRAME 10/20, MOD TRI/SQ, and MASTER/SLAVE, the following device functions are produced:

- MC145421: UDLT-2 Master
- MC145425: UDLT-2 Slave
- MC145422: UDLT-1 Master
- MC145426: UDLT-1 Slave

In addition, these new features have been added:

- 2.048 MHz: output for clock input to a CODEC
- LI SENS: reduces the sensitivity of the LI input—thus reducing the effects of crosstalk on an open loop
- In UDLT-1 slave mode, the user has the option of selecting the timeslot for Rx.

This document contains the following topics:

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Overview

The M145423EVK module provides a working UDLT communications link that interfaces to synchronous transmit and receive clock configurations. This board has been designed to provide the user with a quick and easy way to evaluate all of the MC145423 functions and features. In addition to making a quantitative evaluation, the handsets (two included) allow the user to also make qualitative evaluations of this complete voice/data system. The use of this module and its features, will help to speed up prototype development—reducing time to market.

In addition to supplying all the clocks required to operate the MC145423 in all of its modes, this board also generates all the clocks necessary to test the device using an HP1645A data error analyzer or similar piece of test equipment. An example test setup is provided later in this data sheet.

This board provides easy access to clocks and other signals in two ways:

1. Through a connector on the edge of the board. The edge connector's pin assignments are shown in Figure 13.

2. Through test points (pins) located throughout the board. While some of these test points are duplicates of those provided via the edge connectors, there are some additional points which are not provided through the edge connector.

CAUTION

The edge connector pins and the test points on the board are connected directly to device pins. Precautions must be taken to prevent electro-static discharge (ESD) damage to the high-impedance pins on the integrated circuits.

To aid the user, two LEDs have been provided on both the master and slave sides of this board. The green LED is connected to the VD (valid data) output of the MC145423. When receiving data, this LED will light, signaling that the data was correctly received and decoded.

The second LED (yellow) is connected to SDO1 of the MC145423. A momentary switch (S1) is connected to SDI1. When the user presses S1, on the slave or master side, the yellow LED on the other master or slave side will light, indicating there is communication between the two UDLT-3s.

The MC145423 is a replacement device for the following ICs.

- MC145421 UDLT-2 Master
- MC145425 UDLT-2 Slave
- MC145422 UDLT-1 Master
- MC145426 UDLT-1 Slave

In the UDLT-1 mode, this device, when operated at +5 V V_{DD}, supports a full duplex 64-kbps data channel and two 8 kbps signaling channels over one 26 AWG and larger wire pair up to 2 km.

In the UDLT-2 mode, this device, when operated at +5 V V_{DD}, is capable of full duplex communication consisting of two 64 kbps data channels, and two 16 kbps signaling channels over one 26 AWG and larger wire pair up to 1 km. This signaling format, known as 2B+2D is compatible with ISDN.

Table 1 is a comparison of the UDLT-1 and UDLT-2 master and slave modes. General differences are listed first, followed by the required state of the control pins to configure the MC145423 into its four different modes. Last, are listed the differences in the functions of the device pins. Any pins not listed retain the same function regardless of the mode of the part.

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Table 1. Comparison of Pin Functions

	Pin No.	UDLT-1 Master	UDLT-2 Master	UDLT-1 Slave	UDLT-2 Slave
General Info					
Data Rate		80 kbps	160 kbps	80 kbps	160 kbps
Data Packets		10 bits (8+1+1)	20 bits (8+8+2+2)	10 bits (8+1+1)	20 bits (8+8+2+2)
Control Pins					
FRAME 10/20	8	0	1	0	1
MOD TRI/SQ	14	0	1	0	1
MASTER/SLAVE	27	0	0	1	1
Multi-Function Pins					
CCI/XTAL$_{in}$	19	2.048 MHz	8.192 MHz	4.096 MHz	8.192 MHz
TDC/RDC XTAL$_{out}$	20	64 kHz to 2.56 MHz	128 kHz to 4.1 MHz	—	—
LI SENS/2.048 MHz	21	LI SENS	LI SENS	2.048 MHz	2.048 MHz
SE/(Mu/A)	12	SE	SE	Mu/A	Mu/A
EN2-TE2/SIE/B1B2	16	SIE	TE2	B1B2	EN2
EN1-TE1	17	TE1	TE1	TE1	EN1
MSI/TONE	18	MSI	MSI	TONE	TONE
RE1/CLKOUT	22	RE1	RE1	RE1	CLKOUT
RE2/BCLK	23	—	RE2	BCLK	BCLK
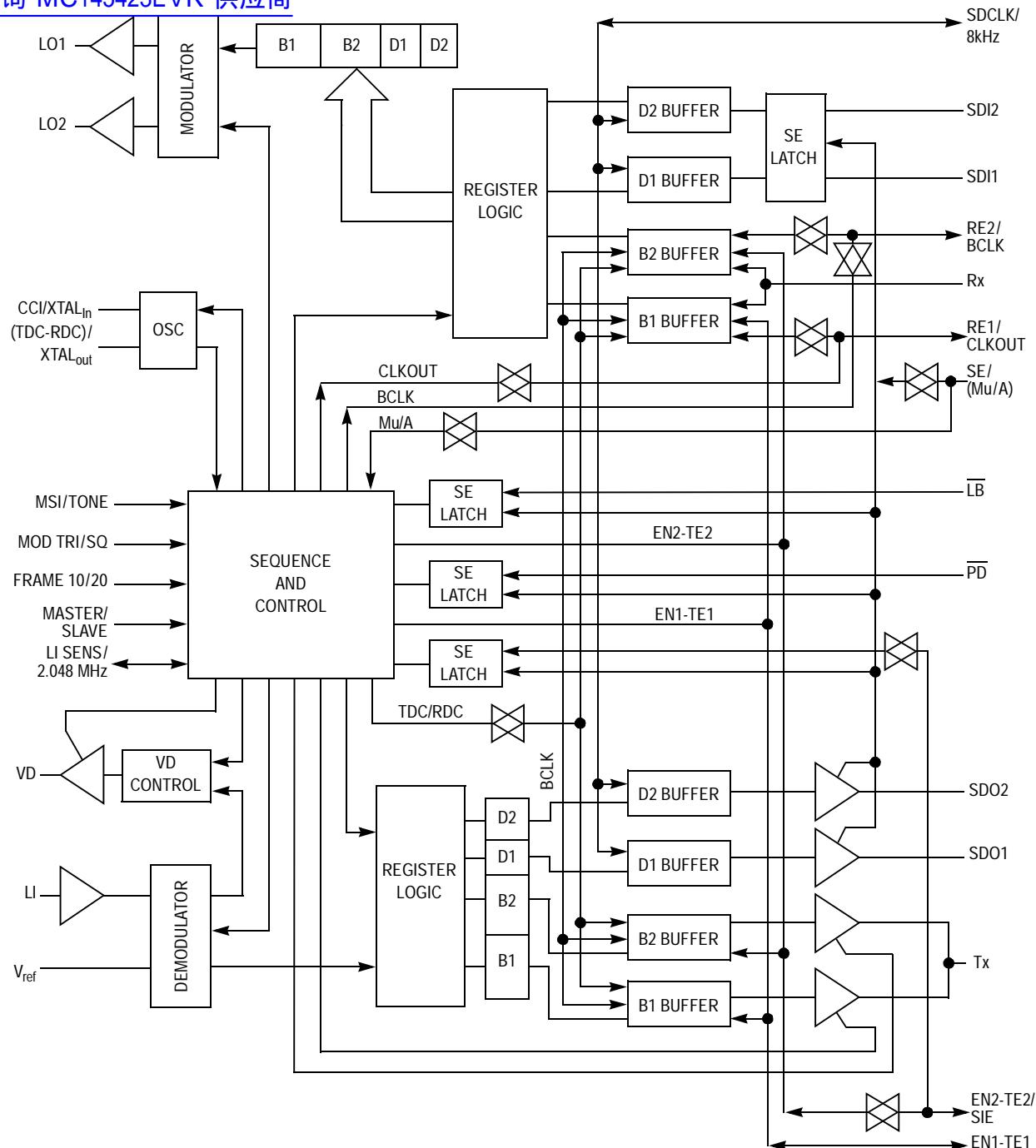
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Figure 1. MC145423 Block Diagram

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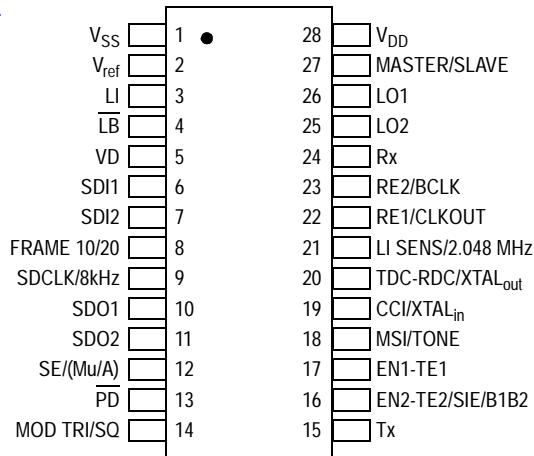
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Figure 2. MC145423 Pinout

The pinout shows pins 1-14 on the left and 28-15 on the right:

Left	Pin		Pin	Right
V_{SS}	1		28	V_{DD}
V_{ref}	2		27	MASTER/SLAVE
$\overline{LI}$	3		26	LO1
$\overline{LB}$	4		25	LO2
VD	5		24	Rx
SDI1	6		23	RE2/BCLK
SDI2	7		22	RE1/CLKOUT
FRAME 10/20	8		21	LI SENS/2.048 MHz
SDCLK/8kHz	9		20	TDC-RDC/$XTAL_{out}$
SDO1	10		19	CCI/$XTAL_{in}$
SDO2	11		18	MSI/TONE
SE/(Mu/A)	12		17	EN1-TE1
$\overline{PD}$	13		16	EN2-TE2/SIE/B1B2
MOD TRI/SQ	14		15	Tx

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Jumpers and Test Points

Table 2. Master—List of Jumpers

Jumper	Function
J10	Enables TDC(L)/RDC(L) to the MC145423
J7	Enables TDC/RDC—removal of this jumper also disables TDC(L)/RDC(L)
J6	Enables SDCLK(L)—removal of this jumper also disables SDCLK
J8	Enables MSI, TE1, RE1
J13	Enables TE2 and RE2 to the MC145423 or V_{DD} or V_{SS}
	Position A selects 8 kHz to RE2/BCLK and EN2/TE2
	Position B selects V_{SS} to RE2/BCLK and EN2/TE2 for BER testing
	Position C selects V_{DD} to RE2/BCLK and EN2/TE2
J3	Enables CCI/XTAL$_{in}$
	Position A selects 8.192 MHz—for UDLT-2 mode
	Position B selects 2.048 MHz—for UDLT-1 mode
J4	Enables SDCLK to the MC145423
J1	Selects the framing for the MC145423
	Position A selects UDLT-1
	Position B selects UDLT-2
J2	Selects the modulation type for the MC145423
	Position A selects square wave
	Position B selects triangle wave
J26	Removal of this jumper allows insertion of a current meter in the V_{SS} line
J12	Selects power-up/-down on the MC145484 CODEC
	Position A selects power-down
	Position B selects power-up
J11	Selects the companding scheme on the MC145484
	Position A selects A law
	Position B selects Mu law
J9	Selects TONE enable in the MC145423 slave mode—left open in master mode
	Position A selects TONE enabled
	Position B selects TONE disabled
J5	Selects LI attenuation in the MC145423 master mode
	Position A selects maximum sensitivity (logic 1)
	Position B selects minimum sensitivity (logic 0)

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Table 3. Master—List of Test Points

Test Point	Function
TP6	TDC/RDC monitor on the MC145423
TP4	Monitors SDCLK on the MC145423
TP1	Monitors V_{ref} on the MC145423
TP23	MC145423 V_{SS} monitor
TP2	Monitors LO1 on the MC145423—can be differential measurement with LO2
TP3	Monitors LO2 on the MC145423—can be differential measurement with LO1
TP24	Monitors $XTAL_{in}$ on the MC145423
TP5	Monitors Tx on the MC145423
TP8	Monitors RO—on the MC145484
TP9	Monitors TI—on the MC145484
TP10	MC145484 V_{SS} monitor
TP7	MC145423 RE1 monitor
TP27	MC145423 LI monitor
TPDT	MC145423 Rx monitor

Table 4. Slave—List of Jumpers

Jumper	Function
J24	Removal of this jumper allows for monitoring V_{SS} current
J14	Selects the framing for the MC145423
	Position A selects UDLT-1
	Position B selects UDLT-2
J15	Selects the modulation type for the MC145423
	Position A selects square wave
	Position B selects triangle wave
J18	Selects power-up/-down on the MC145484 CODEC
	Position A selects power-down
	Position B selects power-up
J17	Selects the companding scheme on the MC145484
	Position A selects A law
	Position B selects Mu law
J16	Selects TONE enable/disable in slave mode
	Position A selects TONE enabled
	Position B selects TONE disabled

Table 4. Slave—List of Jumpers (continued)

Jumper	Function
J20	Selects XTAL$_{in}$ internal or external
	Position A selects external clocking
	Position B selects internal clocking
J21	Selects internal clock frequency
	Position A selects 8.192 MHz for UDLT-1 mode
	Position B selects 4.096 MHz for UDLT-2 mode
J19	Selects Rx timeslot
	Position A selects synchronous Tx/Rx
	Position B selects nonsynchronous Tx/Rx

Table 5. Slave—List of Test Points

Test Point	Function
TP25	Monitors SDCLK on the MC145423
TP11	Monitors V$_{ref}$ on the MC145423
TP22	V$_{SS}$ monitor on the MC145423
TP12	LO1 monitor on the MC145423—can be differential with LO2
TP13	LO2 monitor on the MC145423—can be differential with LO1
TP14	Monitors MC145423 XTAL$_{out}$ in slave mode
TP17	Tx monitor on the MC145423
TP16	MC145423 2.048 MHz output monitor—in slave mode
TP18	RO—monitor on the MC145484
TP19	TI—monitor on the MC145484
TP21	V$_{SS}$ monitor on the MC145484
TP15	MC145423 4.096 MHz output monitor
TP20	MC145423 XTAL$_{in}$ monitor
TP26	MC145423 LI monitor
TPDT	MC145423 Rx monitor

There are two types of jumpers drawn on the schematics. Three-terminal jumpers, shown in Figure 3, are used to select between one of two signals or logic states. Two-terminal jumpers, as shown in Figure 4, are used to simply enable or disable a signal or logic state. All jumpers are designated with a J followed by a number (i.e., J1). On three-terminal jumpers the user choices are labeled A and B.
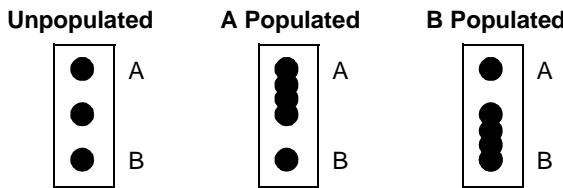
Figure 3. Three-Terminal Jumper
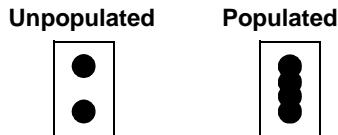
Figure 4. Two-Terminal Jumper

There are numerous test points on the board. They are there to allow the user to easily observe signals and logic states. All test points are identified by a TP followed by a number (i.e., TP1). Test points can be identified by the symbol as shown in Figure 5.

Figure 5. Test Point Symbol

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Configurations

Table 6. UDLT-1 Master Mode Jumper Configurations

Jumper No.	2-Terminal	3-Terminal		Description
		A	B	
10	Populated			Enable—TDC(L)/RDC(L)
7	Populated			Enable—TDC/RDC
6	Populated			Enable—SDCLK(L)
8	Populated			Enable—MSI, TE1, RE1, CLK1(L), CLK1
13		Populated		Enable—TE2, RE2 (8 kHz)
3			Populated	Select—2.048 MHz
4	Populated			Enable—SDCLK
1		Populated		Select—FRAME UDLT-1
2			Populated	Select—MODULATION triangle
26	Populated			Enable—V_{SS}
12			Populated	Select—CODEC power-up
11			Populated	Select—CODEC Mu law
9		Unpopulated		Open—MSI/TONE (do not connect)
5			Populated	Select—Sensitivity max

Table 7. UDLT-2 Master Mode Jumper Configurations

Jumper No.	2-Terminal	3-Terminal		Description
		A	B	
10	Populated			Enable—TDC(L)/RDC(L)
7	Populated			Enable—TDC/RDC
6	Populated			Enable—SDCLK(L)
8	Populated			Enable—MSI, TE1, RE1, CLK1(L), CLK1
13		Populated		Enable—TE2, RE2 (8 kHz)
3		Populated		Select—8.192 MHz
4	Populated			Enable—SDCLK
1			Populated	Select—FRAME UDLT-2
2		Populated		Select—MODULATION square
26	Populated			Enable—V_{SS}
12			Populated	Select—CODEC power-up
11			Populated	Select—CODEC Mu law
9		Unpopulated		Open—MSI/TONE (do not connect)
5			Populated	Select—Sensitivity max

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Figure 6. UDLT-1 Master Mode

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Figure 7. UDLT-2 Master Mode

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## "MC145423EVK"
Connecting to a Line Card

The master side of the M145423EVK board may be connected to a line card—in an existing PBX, for example—for further evaluation by the user. If it is desirable for the MC145423 clocks to be supplied internally, the jumper positions listed earlier may be used. If however, the user wishes to supply the clocks externally the jumper positions listed in Table 8 and Table 9 are to be used.

Table 8. Master In UDLT-1 Mode Connected to Line Card Using External Clocks

Jumper No.	2-Terminal	3-Terminal		Description
		A	B	
10	Unpopulated			Open—TDC(L)/RDC(L)
7	Unpopulated			Open—TDC/RDC
6	Unpopulated			Open—SDCLK(L)
8	Unpopulated			Open—MSI, TE1, RE1, CLK1(L), CLK1
13		Unpopulated		Open—TE2, RE2
3			Populated	Select—2.048 MHz
4	Unpopulated			Open—SDCLK
1		Populated		Select—FRAME UDLT-1
2			Populated	Select—MODULATION triangle
26	Populated			Enable—V_{SS}
12			Populated	Select—CODEC power-up
11			Populated	Select—CODEC law
9		Unpopulated		Open—MSI/TONE (do not connect)
5			Populated	Select—Sensitivity max

Table 9. Master In UDLT-2 Mode Connected to Line Card Using External Clocks

Jumper No.	2-Terminal	3-Terminal		Description
		A	B	
10	Unpopulated			Open—TDC(L)/RDC(L)
7	Unpopulated			Open—TDC/RDC
6	Unpopulated			Open—SDCLK(L)
8	Unpopulated			Open—MSI, TE1, RE1, CLK1(L), CLK1
13		Unpopulated		Open—TE2, RE2
3		Populated		Select—8.192 MHz
4	Unpopulated			Open—SDCLK
1			Populated	Select—FRAME UDLT-2
2		Populated		Select—MODULATION square
26	Populated			Enable—V_{SS}
12			Populated	Select—CODEC power-up
11			Populated	Select—CODEC Mu law
9		Unpopulated		Open—MSI/TONE (do not connect)
5			Populated	Select—Sensitivity max

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Figure 8. UDLT-1 Master Mode Line Card Setup
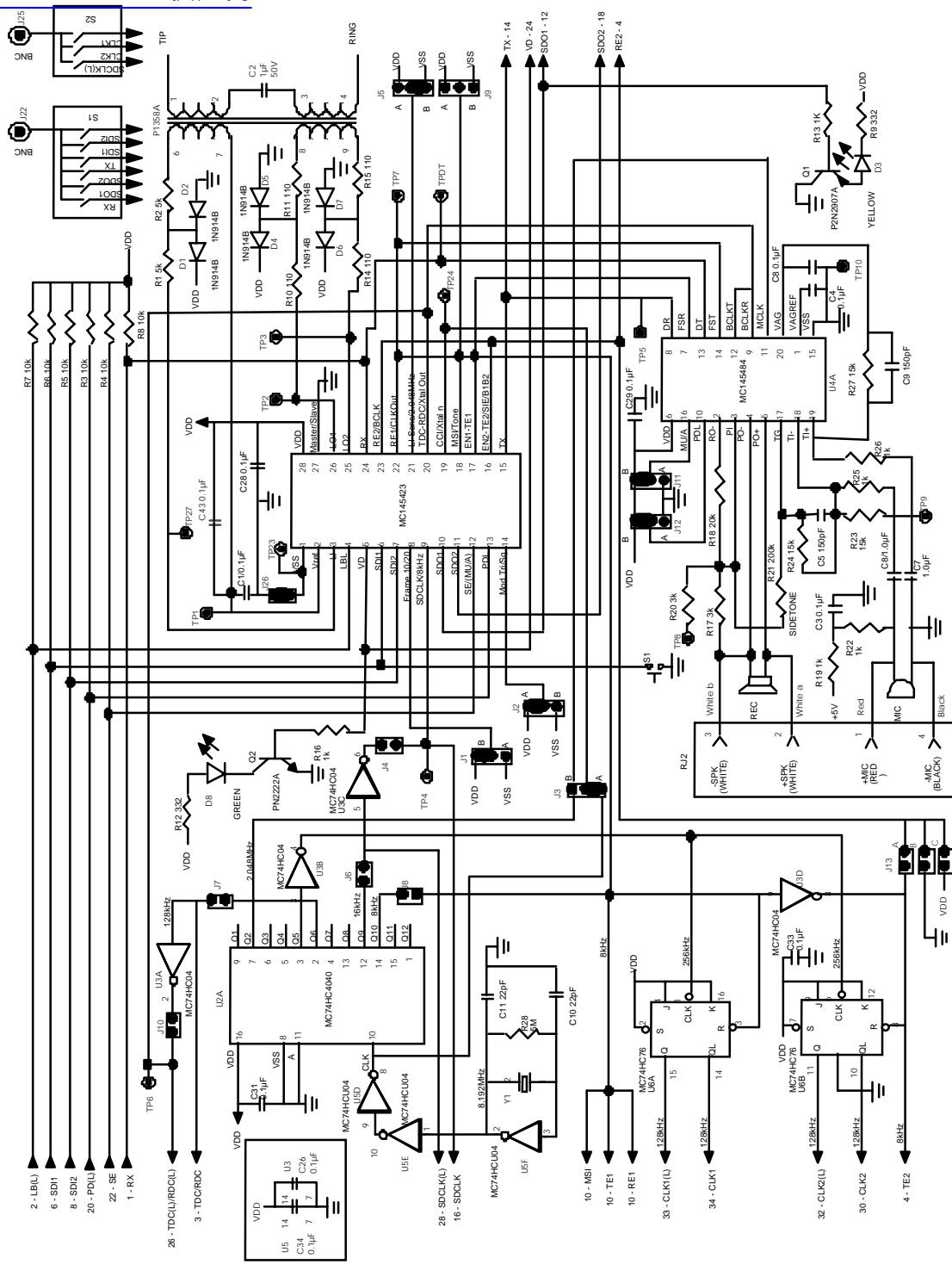
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Figure 9. UDLT-2 Master Mode Line Card Setup

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Table 10. UDLT-1 Slave Mode Setup

Jumper No.	2-Terminal	3-Terminal		Description
		A	B	
24	Populated			Enable—V_{SS}
14		Populated		Select—FRAME UDLT-1
15			Populated	Select—MODULATION triangle
18			Populated	Select—CODEC power-up
17			Populated	Select—Mu law
16			Populated	Select—TONE disabled
20			Populated	Select—Internal clock (on board)
21		Populated		Select—4.096 MHz
19		Populated		Select—Synchronous Rx/Tx (CODEC)
			Populated	Select—Nonsynchronous Rx/Tx (BERT)

Table 11. UDLT-2 Slave Mode Setup

Jumper No.	2-Terminal	3-Terminal		Description
		A	B	
24	Populated			Enable—V_{SS}
14			Populated	Select—FRAME UDLT-2
15		Populated		Select—MODULATION square
18			Populated	Select—CODEC power-up
17			Populated	Select—Mu law
16			Populated	Select—TONE disabled
20			Populated	Select—Internal clock (on board)
21			Populated	Select—8.192 MHz
19		Open	Open	Not applicable (do not connect)

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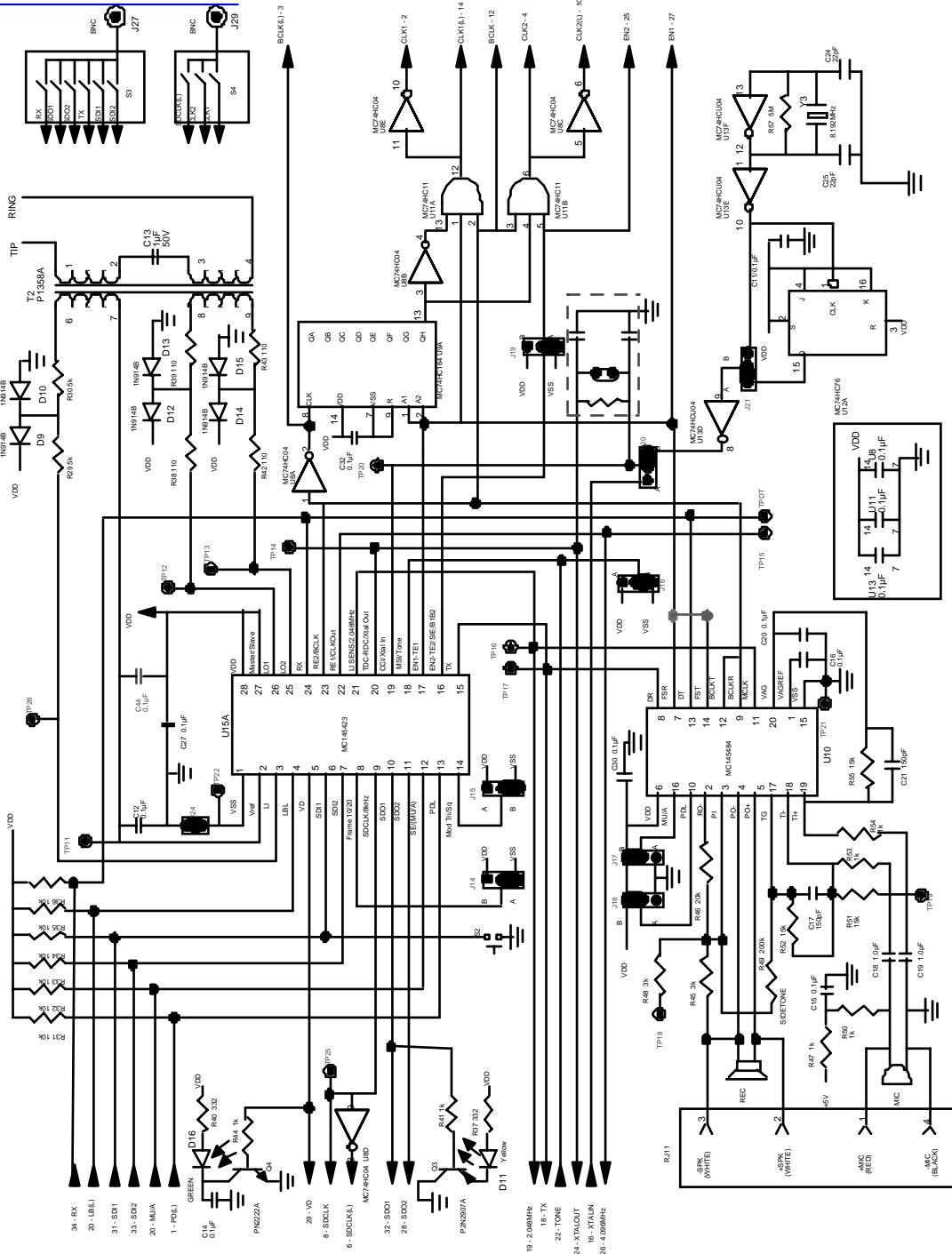
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Figure 10. UDLT-1 Slave Mode—Rx Synchronous with Tx

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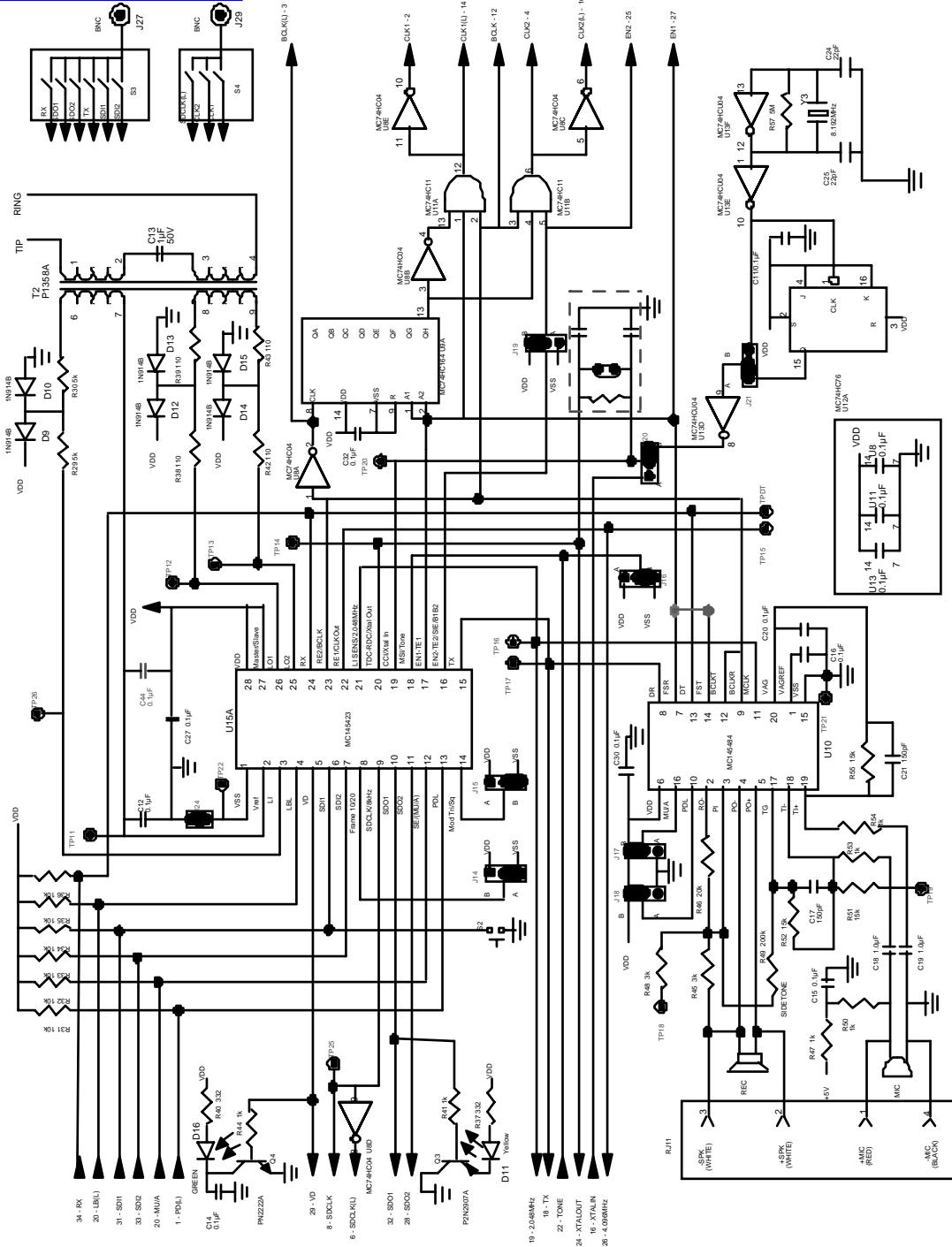
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Figure 11. UDLT-1 Slave Mode—Rx Nonsynchronous with Tx

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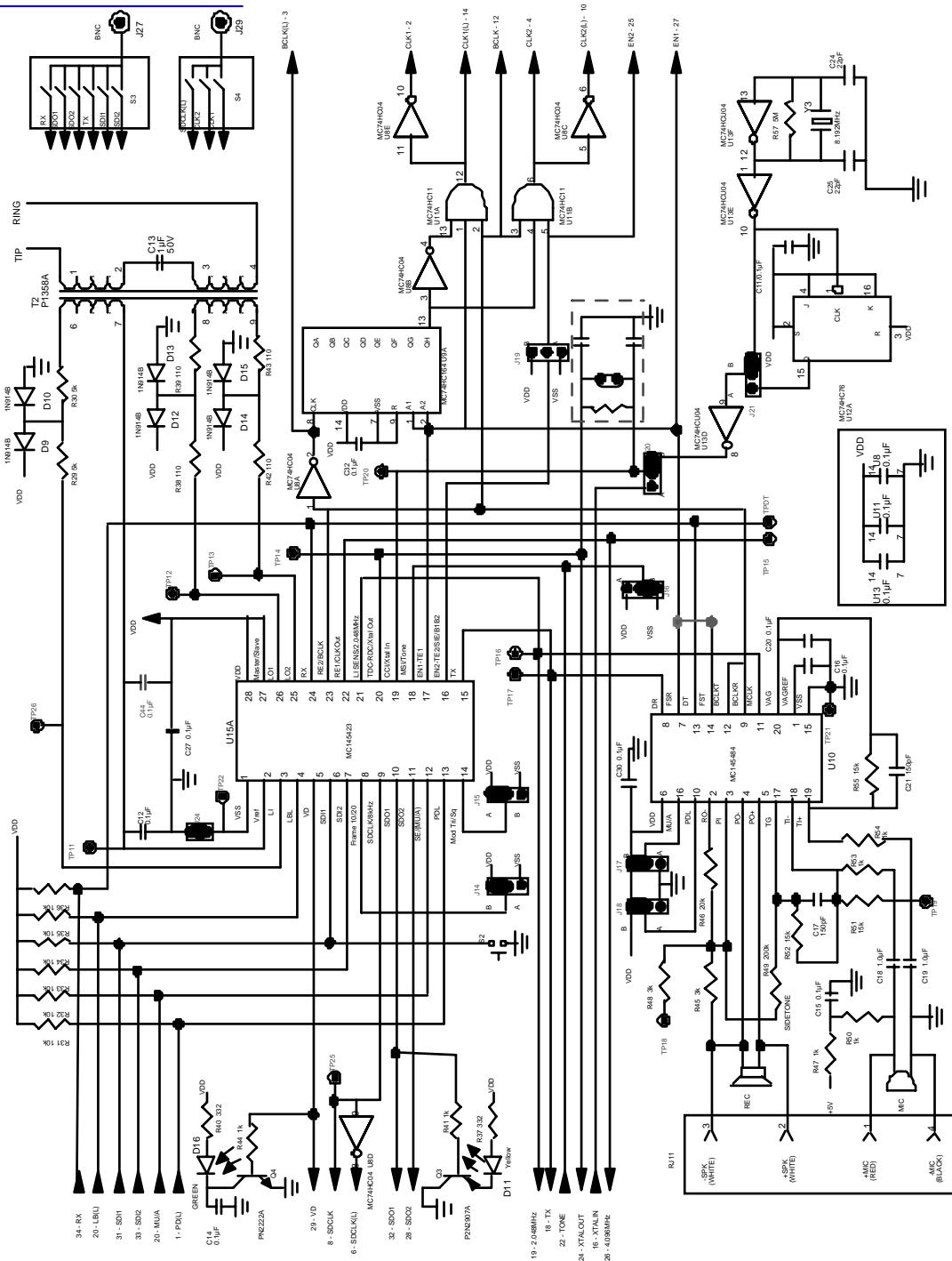
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Figure 12. UDLT-2 Slave Mode

"MC145423EVK" # Connectors J1 and J2

CAUTION

The edge connector pins and test points on the board are connected directly to the device pins. Precautions must be taken to prevent ESD damage to the high-impedance pins on the integrated circuits.
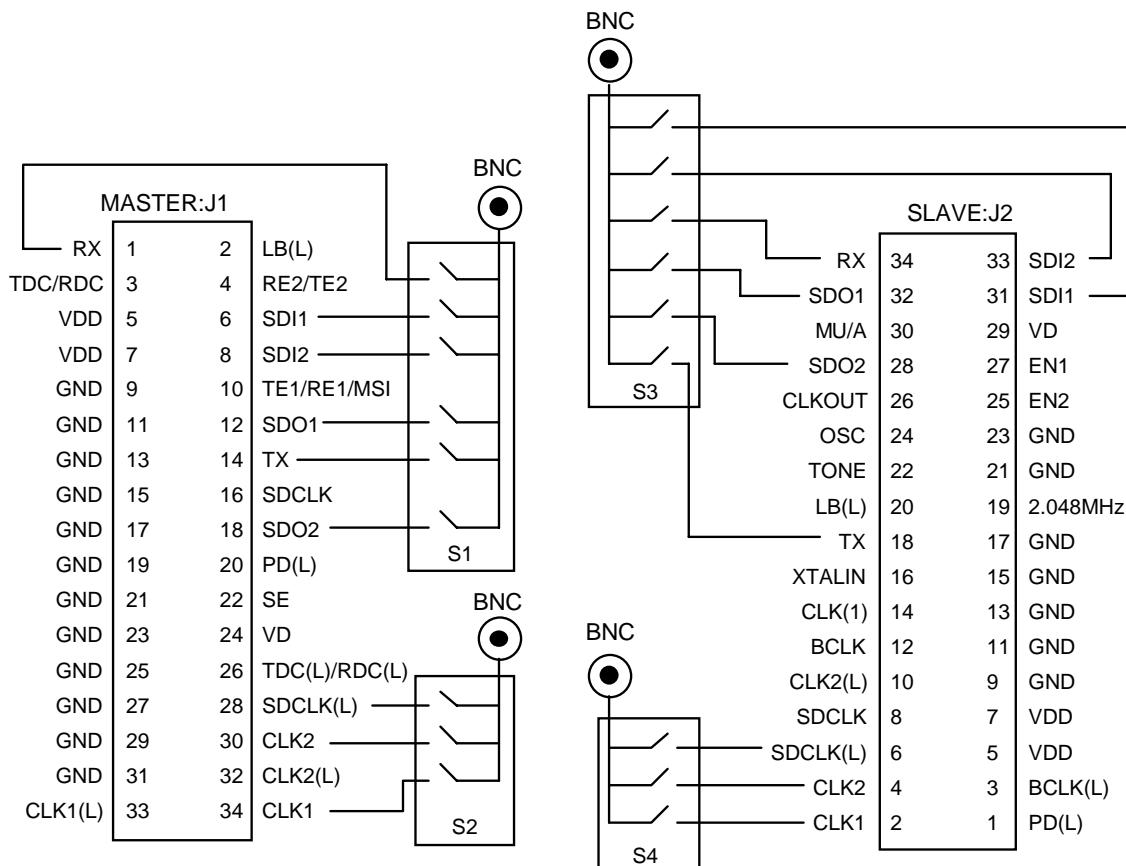
Figure 13. Connectors J1 and J2
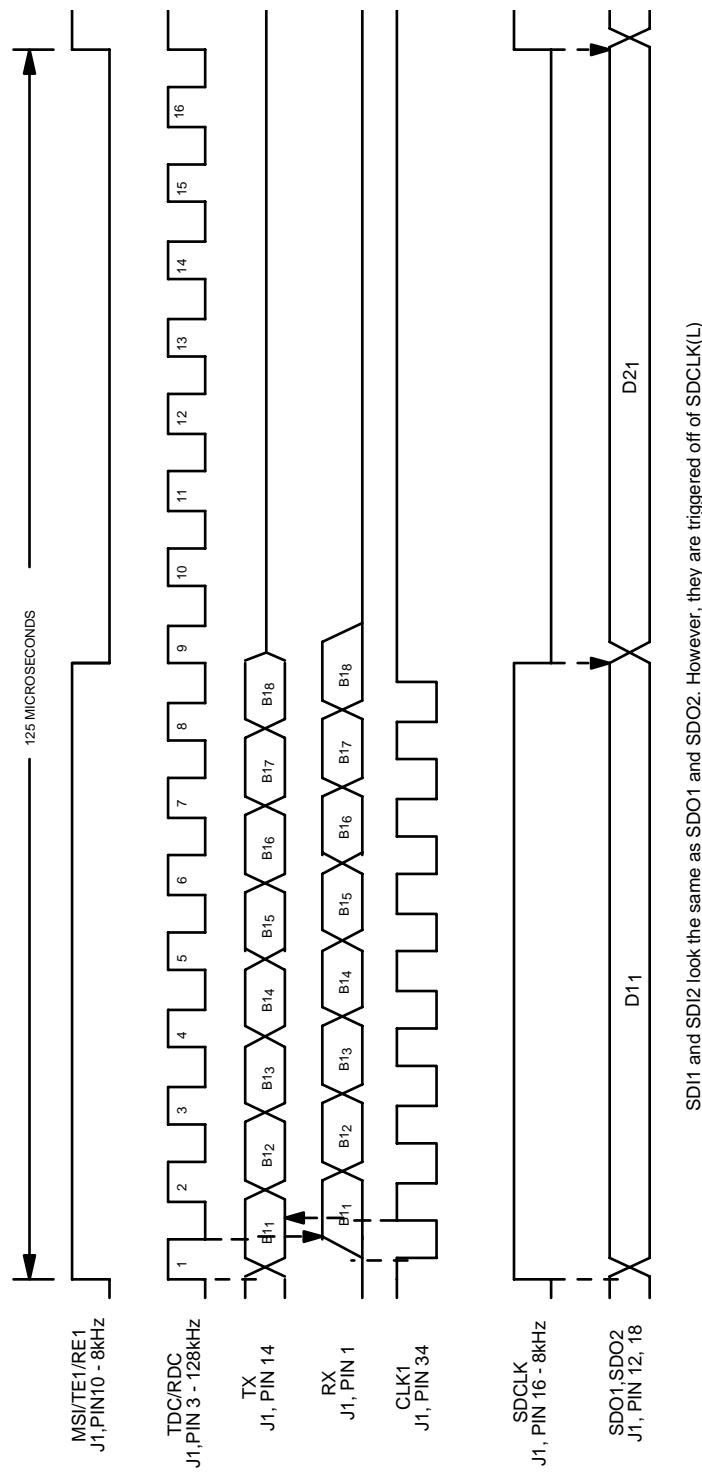
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Timing Diagrams

Figure 14. Master UDLT-1 EVK Timing Diagram

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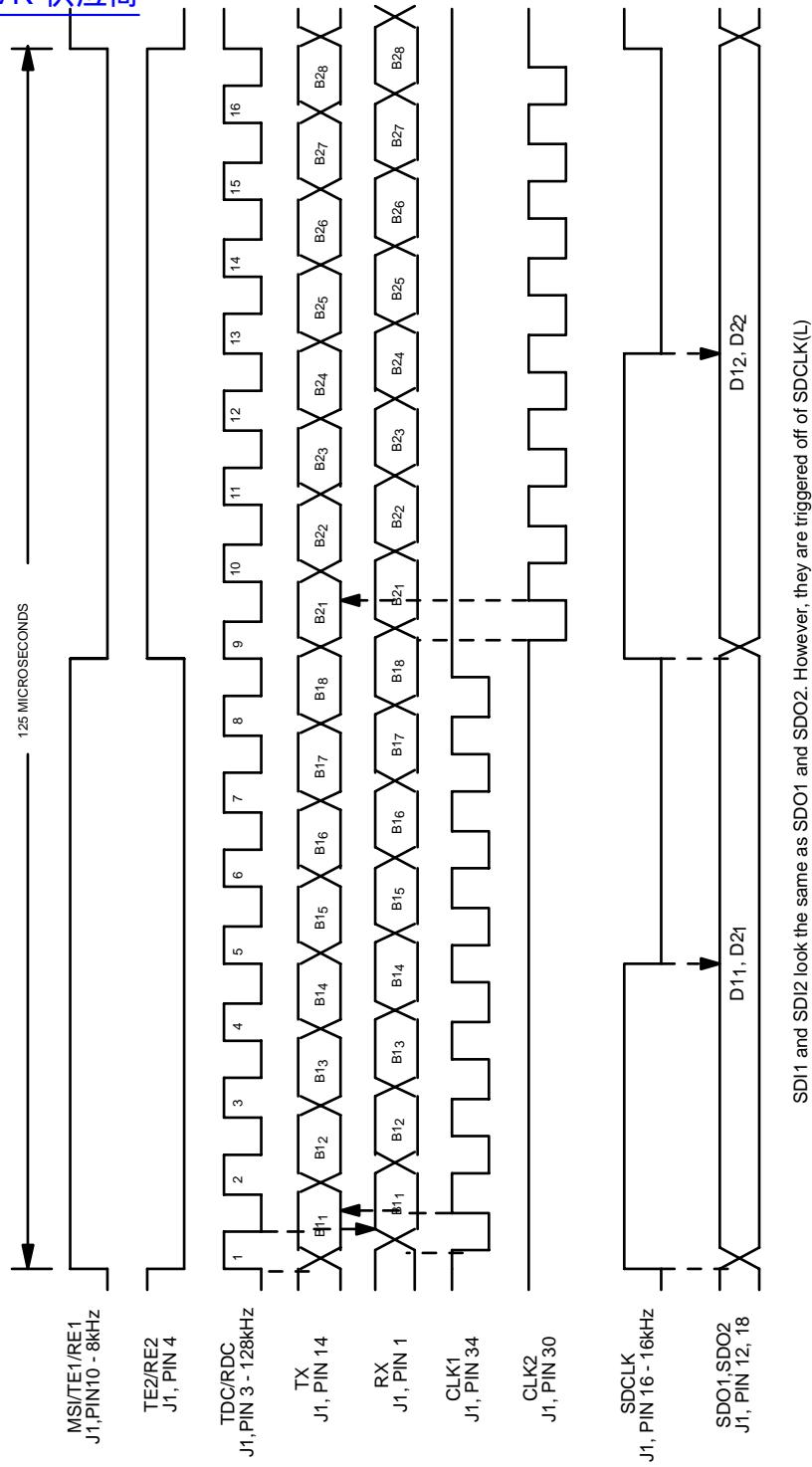
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Figure 15. Master UDLT-2 EVK Timing Diagram
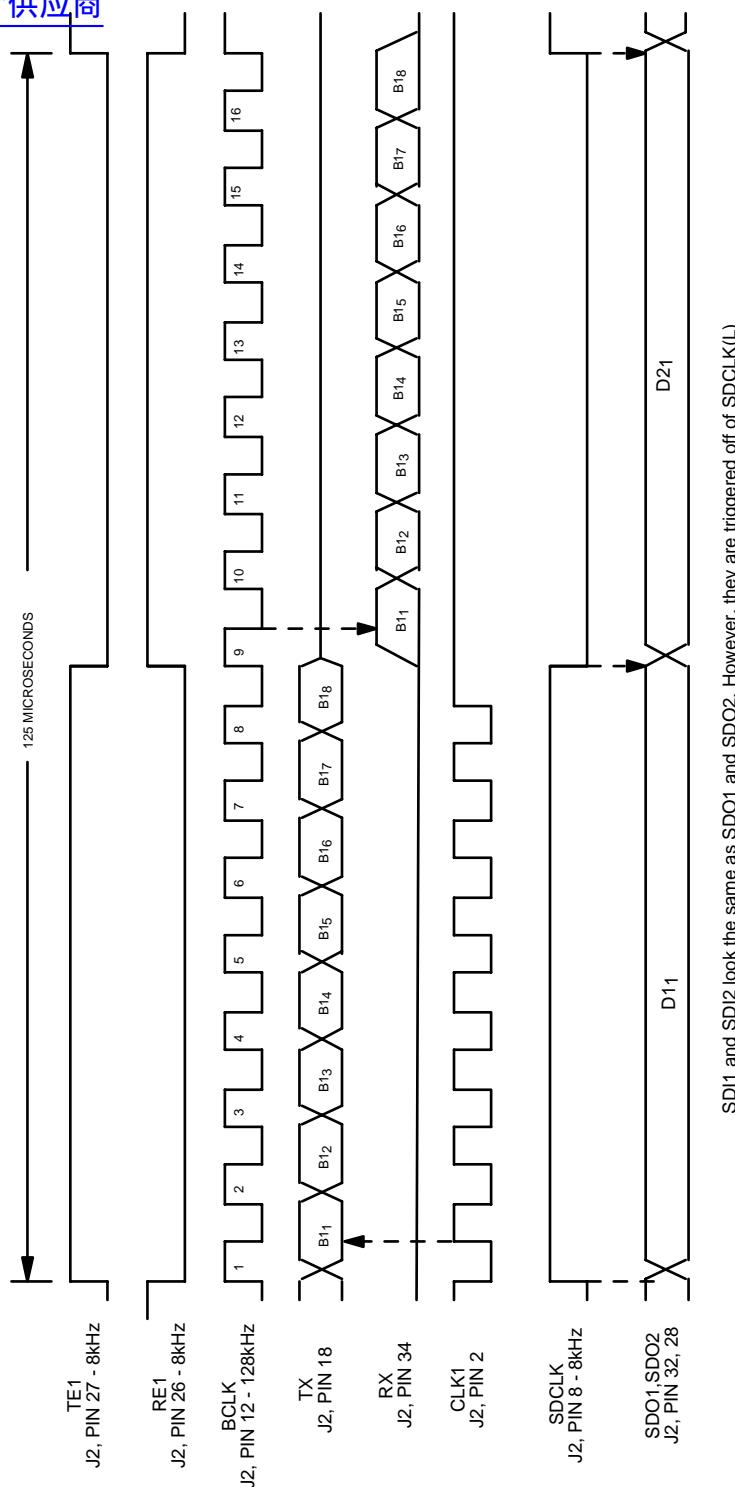
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Figure 16. Slave UDLT-1 EVK Timing Diagram—Nonsynchronous Tx/Rx
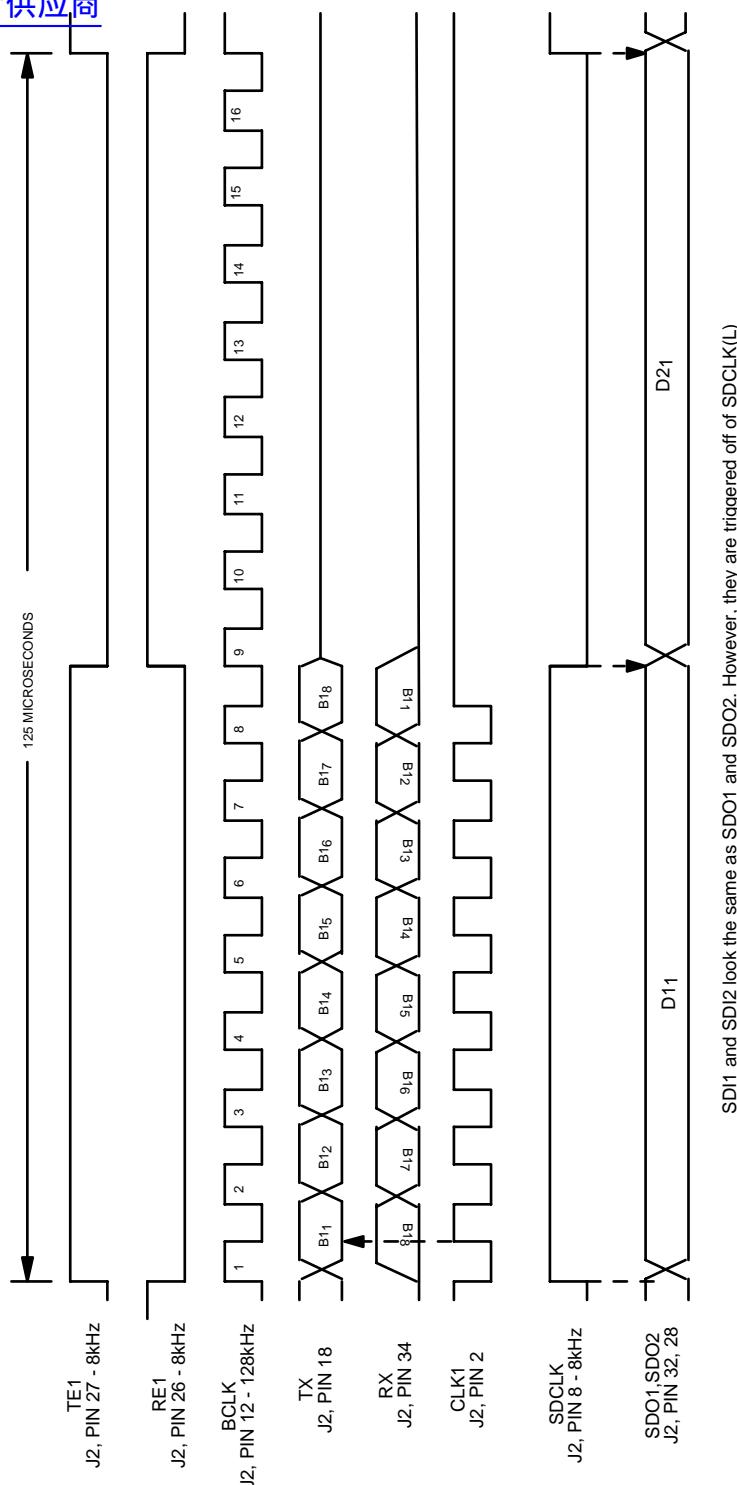
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Figure 17. Slave UDLT-1 EVK Timing Diagram—Synchronous Tx/Rx
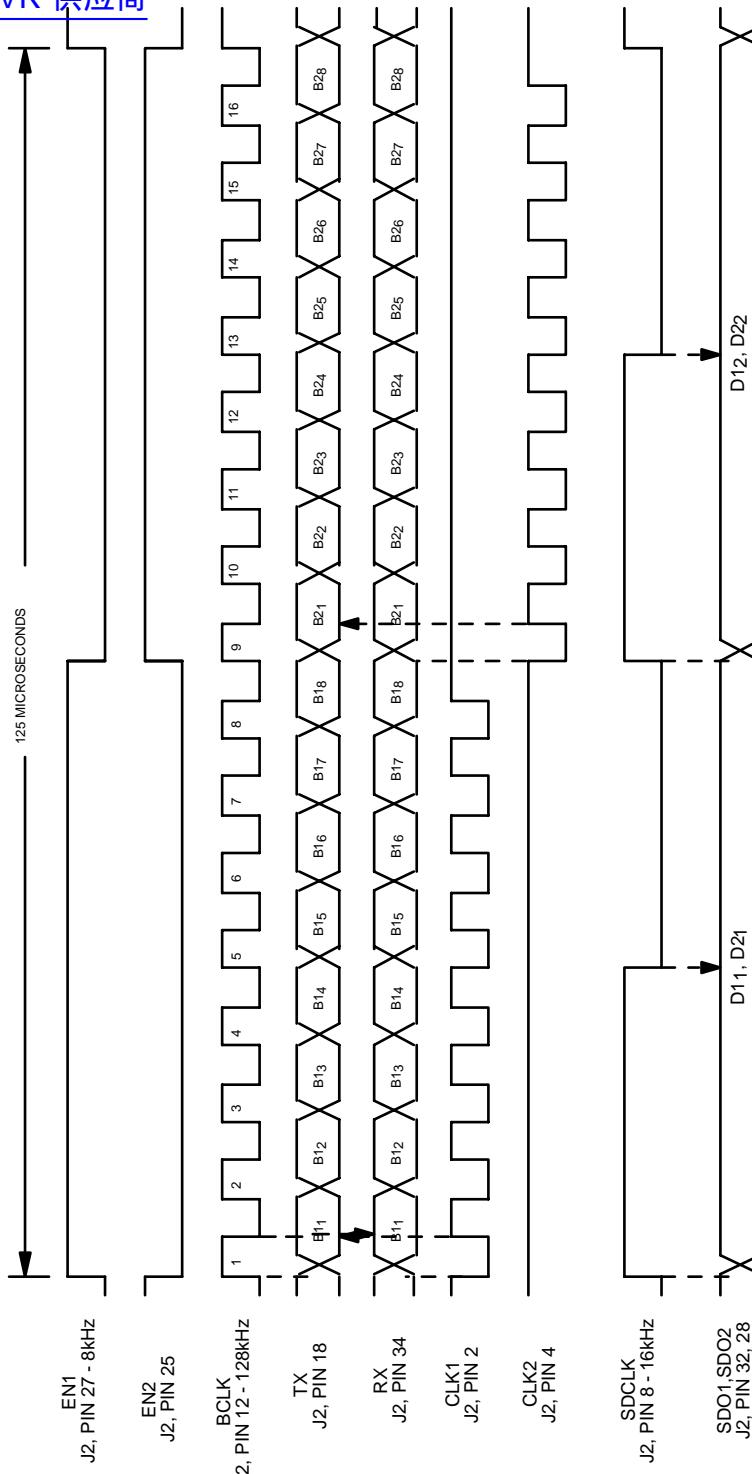
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Figure 18. Slave UDLT-2 EVK Timing Diagram

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Schematics

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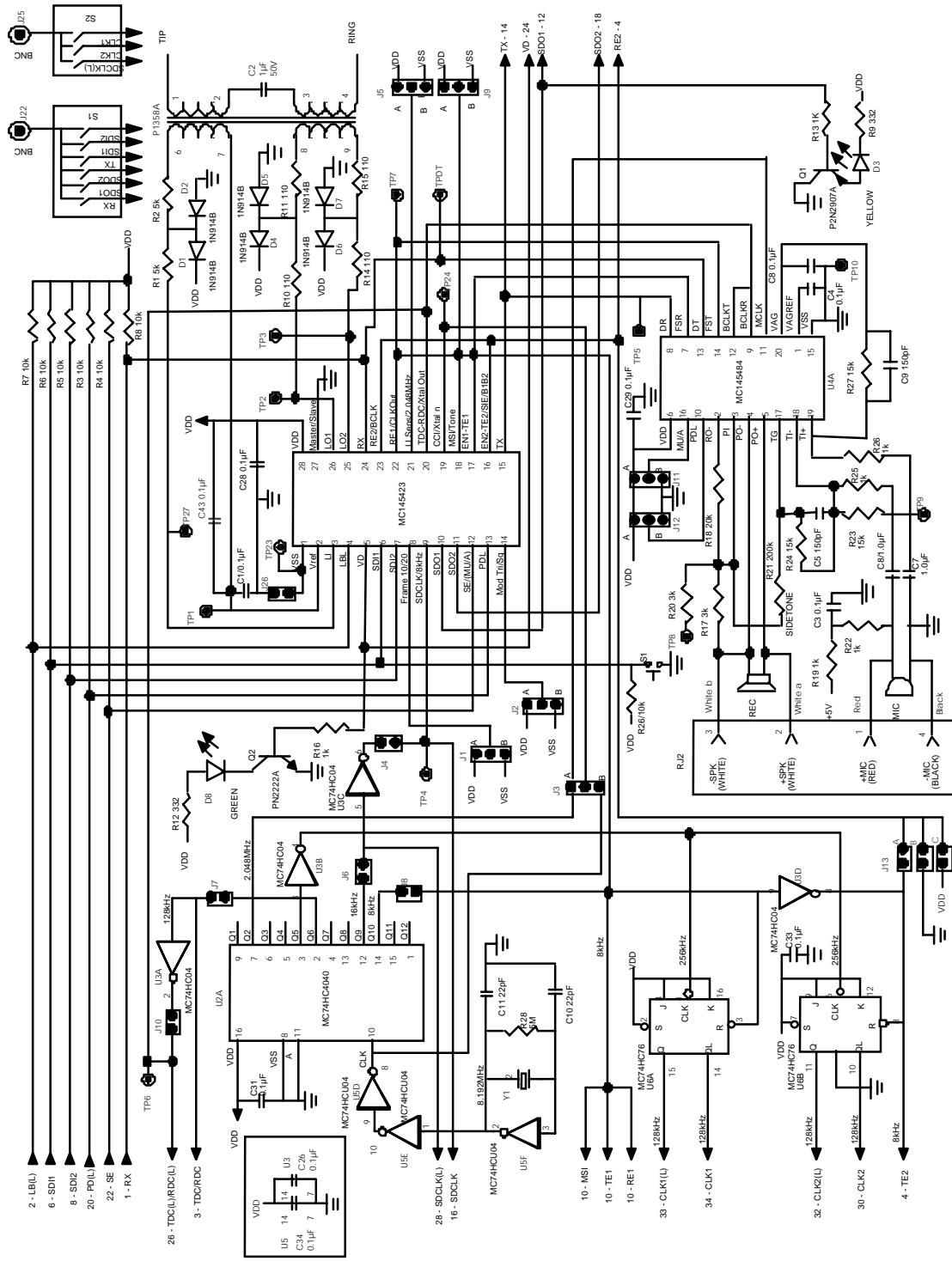
Figure 19. Master Schematic

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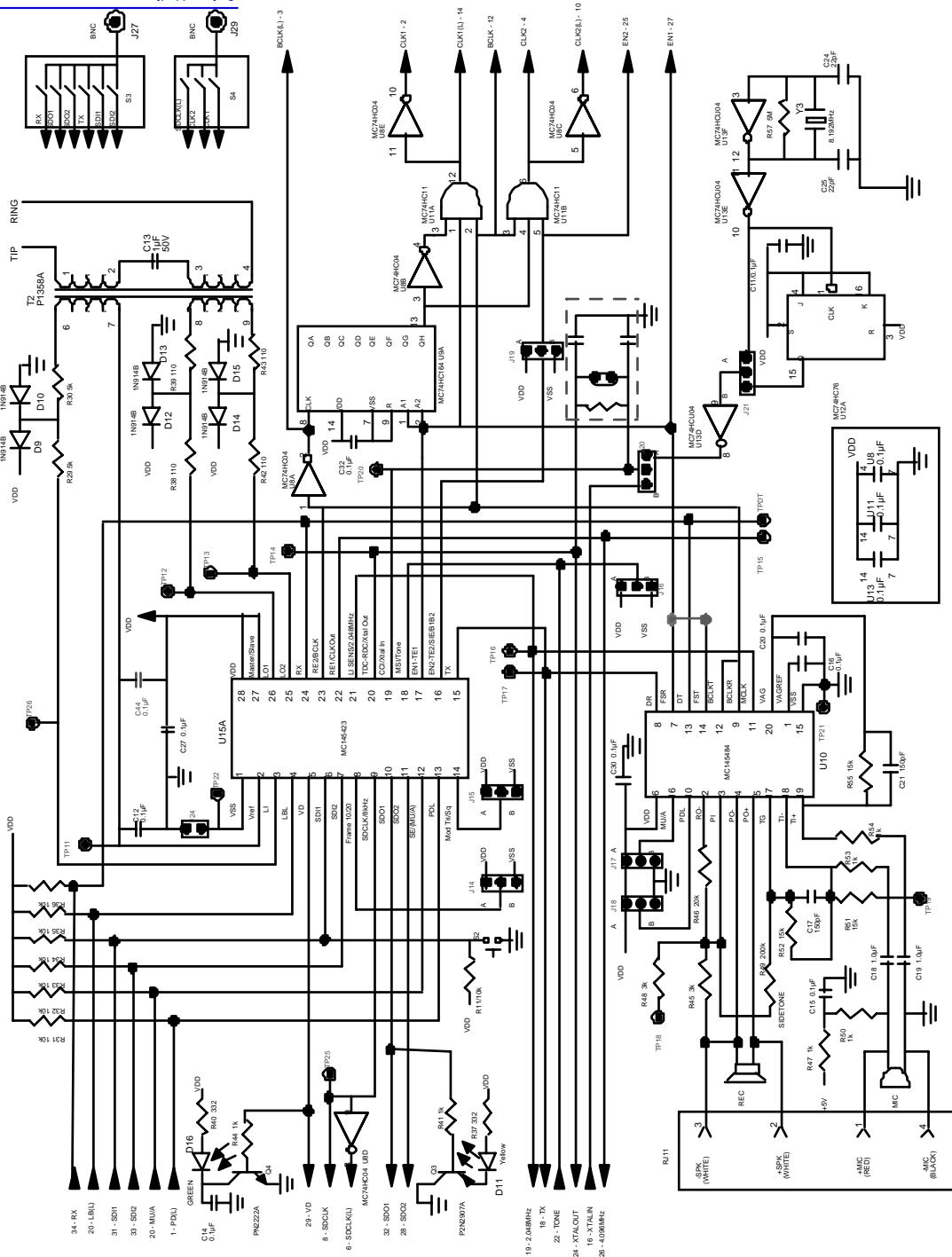
"MC145423EVK"

Figure 20. Slave Schematic

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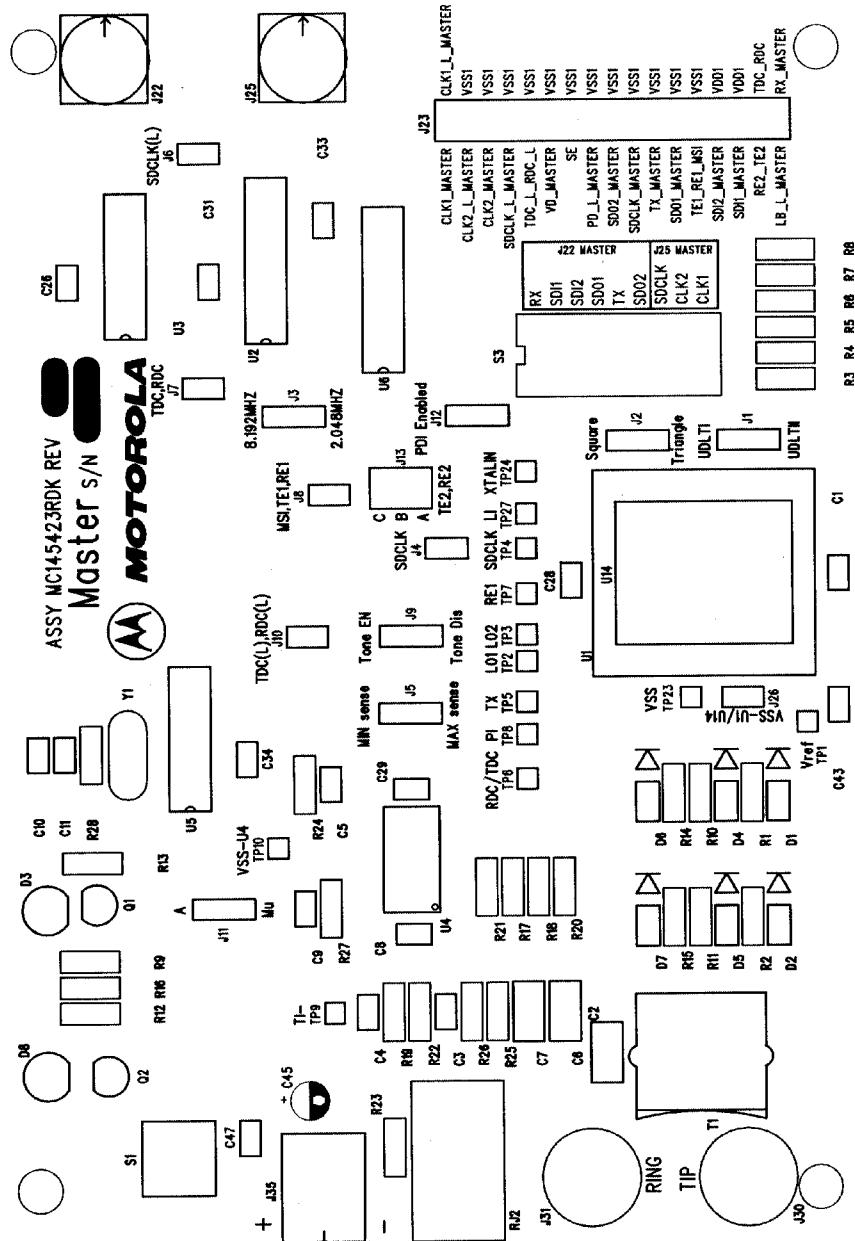
Board Layout

Figure 21. Master EVK Board Layout
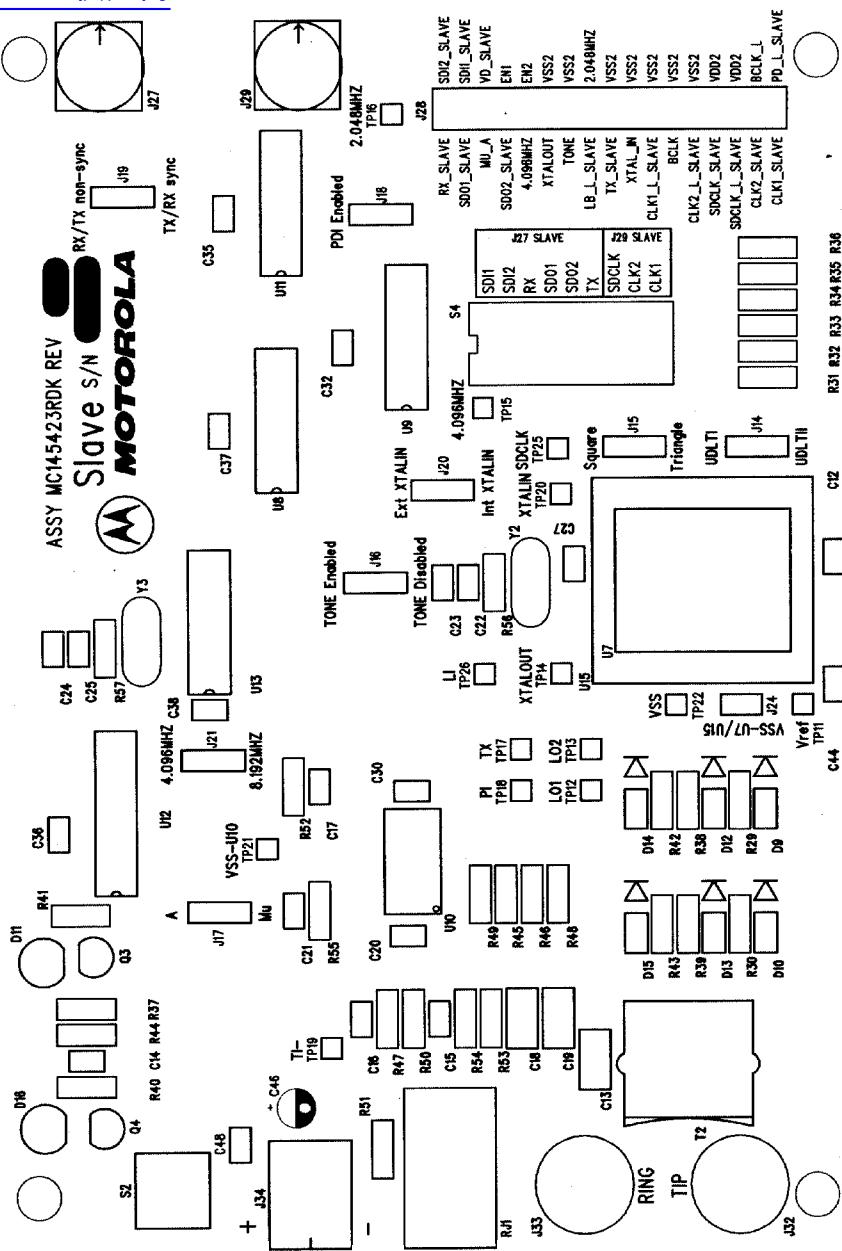
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Figure 22. Slave EVK Board Layout

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Test Example

It may be of interest for the user of this EVK board to check the bit error rate (BER) of the MC145423. The Hewlet Packard HP1645A data error analyzer may be used for this purpose.

The HP1645A can be configured for internally clocked standard data rate input/output (I/O), or externally clocked I/O. The external clock setting should be used to test the MC145423.

The connectors on the back of the data error analyzer need to supply an external transmit clock and an external receive clock. These externally supplied clocks allow the HP1645A to supply (to the MC145423) eight falling edges and eight rising edges (128 kHz) each MSI frame for each channel tested. On the rising edge of the clock fed to the HP1645A external receive clock, the HP1645A will input data at the Data In connector on the front panel. It will output data at the Data Out connector on the front panel, on the falling edge of the clock fed to the HP external transmit clock.

The external clocks for the HP1645A external inputs are generated on both the master and slave boards. The CLK1/CLK1(L) clock is used to test the B channel 1 BER and the CLK2/CLK2(L) is used to test the B channel 2 BER. For the D channel, the inverse of the DCLK will supply the clock needed to test either D channel.

Figure 23 illustrates how to test all of the B and D channels from the master to the slave and from the slave to the master. By looking for the channel to be tested in the Data Channel Select column of this figure, the appropriate signals and pin assignments can be found for connection of the demo board to the HP1645A Data Out, Data In, Tx Clock, and Rx Clock connectors. Figure 23 graphically shows how to hook up a test for the B1 channel, from the master to the slave.

In addition to testing the B channels individually, they may also be tested at the same time. In this configuration, the inverted TDC/RDC clock on the master side is connected to either the HP1645A Tx Clock or Rx Clock, and the inverted BCLK on the slave side is connected to the HP1645A clock, not used by the master board. During the first half of the MSI frame, channel 1 data is exchanged, and during the second half of the MSI frame, channel 2 data is exchanged. In this configuration, B channel 1 and B channel 2 appear as one 128 kbps channel through pins Rx and Tx of the MC145423.

The buffer on the diagram at the Data Out connector of the HP1645A is shown because the HP outputs TTL levels, and the MC145423 requires CMOS levels. Many times this buffer is not required, but if cables are used which attenuate the HP signals, problems are likely to be experienced.

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```
                                              Connector/Pin
                                  Channel      Master        Slave
                                  Selected     Board         Board

                                 •B1, M to S------Rx  (J1,1)
                                 •B1, S to M-------------------------Rx  (J2,34)
                                 •B2, M to S------Rx  (J1,1)
                                 •B2, S to M-------------------------Rx  (J2,34)
                                 •D1, M to S-----SDI1 (J1,6)
                                 •D1, S to M------------------------SDI1 (J2,31)
                                 •D2, M to S-----SDI2 (J1,8)
                                 •D2, S to M------------------------SDI2 (J2,33)

                                 •B1, M to S-------------------------Tx  (J2,18)
                                 •B1, S to M------Tx  (J1,14)
                                 •B2, M to S-------------------------Tx  (J2,18)
                                 •B2, S to M------Tx  (J1,14)
                                 •D1, M to S-------------------------SDO1 (J2,32)
                                 •D1, S to M-----SDO1 (J1,12)
                                 •D2, M to S-------------------------SDO2 (J2,28)
                                 •D2, S to M-----SDO2 (J1,18)

                                 •B1, M to S------CLK1 (J1,34)
                                 •B1, S to M-------------------------CLK1 (J2,2)
                                 •B2, M to S------CLK2 (J1,30)
                                 •B2, S to M-------------------------CLK2 (J2,4)
                                 •D1, M to S-----SDCLK(L) (J1,28)
                                 •D1, S to M------------------------SDCLK(L) (J2,6)
                                 •D2, M to S-----SDCLK(L) (J1,28)
                                 •D2, S to M------------------------SDCLK(L) (J2,6)

                                 •B1, M to S-------------------------CLK1 (J2,2)
                                 •B1, S to M------CLK1 (J1,34)
                                 •B2, M to S-------------------------CLK2 (J2,4)
                                 •B2, S to M------CLK2 (J1,30)
                                 •D1, M to S------------------------SDCLK(L) (J2,6)
                                 •D1, S to M-----SDCLK(L) (J1,28)
                                 •D2, M to S------------------------SDCLK(L) (J2,6)
                                 •D2, S to M-----SDCLK(L) (J1,28)
```

HP1645A DATA ERROR ANALYZER — Data Out, Data In, Tx Clock, Rx Clock

Figure 23. Test Setup to HP1645A

CAUTION

Be sure to move Master jumper 13 to position B: V_{SS} when testing BER.

Channels may be tested by hooking up the data and clock lines of the HP1645A to the signals on the EVK board corresponding (Figure 23) to Data Channel Selected. For example, the arrows show how to test the B1 channel of the M145423 from the master to the slave.

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Appendix I
Precautions

Board Handling

The test points and connector pins are connected directly to the integrated circuit pins on this board. Therefore, it is necessary for the user to exercise the same precautions when handling the M145423EVK as is used when directly handling an IC.

For a complete review of handling precautions refer to the *Motorola Communications Device Data*, Chapter 6, "Handling and Design Guidelines," Motorola Order No. DL136/D.

The following items are excerpts from that reference.

- All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.

- A circuit board containing CMOS devices is merely an extension of the device, and the same handling precautions apply. Contacting connectors wired directly to devices can cause damage.

- CMOS devices should be stored and/or transported in materials that are antistatic. Devices must not be inserted into conventional snow, styrofoam, or plastic trays, but should be left in their original container until ready to use.

- Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.

- Double check the equipment setup for proper polarity of voltage before conducting parametric or functional testing,

- The use of static detection meters is highly recommended.

Layout

Care must be taken during board layout to reduce the ability of other signals to interfere with the analog signals on the board. High frequency signal paths close to analog signal paths can degrade the analog signal. The following methods can be used for reducing interference.

- Minimize the length of analog signal traces

- Substantially decoupling the power supply

- Decouple all ICs with capacitors

- Keep other signals (especially high frequency signals) as far away as possible from the analog signals

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Appendix II
Parts Lists

Table 12. Parts List—Master

Component	Number/Value	Description
ICs	MC145423	UDLT-3
	MC74HC4040	12-Stage Bin Ripple Counter
	MC74HC04	Hex Inverter
	MC74HCU04	Hex Unbuffered Inverter
	MC74HC76	Dual JK Flip-Flop
	MC145484	CODEC
Transistors	Q1/MPS2222	NPN
	Q2/MPS2907	PNP
Diodes (ALL)	1N4004	
Crystal	8.192 MHz	
Resistors	R1-6/10 kΩ	1/4 watt
	R7-8/5 kΩ	
	R9-12/110 Ω	
	R13/5 kΩ	
	R14/330 Ω	
	R15/75 kΩ	
	R16-17/1 kΩ	
	R18-19/75 kΩ	
	R20/200 kΩ	
	R21/3 kΩ	
	R22/20 kΩ	
	R23/3 kΩ	
	R24-25/1 kΩ	
	R26-27/10 kΩ	
	R28/560 Ω	
	R29/5 mΩ	
Capacitors	C1-3/0.1 μF	15 V mica
	C4/0.01 μF	
	C5-6/420 pF	
	C7/68 μF	
	C8-9/1.0 μF	
	C10/0.1 μF	
	C11-12/24 pF	
	C13-14/0.1 μF	

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Table 12. Parts List—Master (continued)

Component	Number/Value	Description
Connectors	J1-2/IDH-34PK-T	Robinson Nugent—34-pin
	BNC	2 BNCs
Switches	S1	6-Position
	S2	3-Position
LEDS	DAILIGHT/521-9212	

Table 13. Parts List—Slave

Component	Number/Value	Description
ICs	MC145423	UDLT-3
	MC74HC164	8-Bit Shift Register
	MC74HC04	Hex Inverter
	MC74HCU04	Hex Unbuffered Inverter
	MC74HC76	Dual JK Flip-Flop
	MC74HC11	Triple 3-Input AND Gate
	MC145484	CODEC
Transistors	Q1/MPS2222	NPN
	Q2/MPS2907	PNP
Diodes (ALL)	1N4004	
Crystal	8.192 MHz	
Resistors	R1-6/10 kΩ	1/4 watt
	R7/560 Ω	
	R8/10 kΩ	
	R9/5 kΩ	
	R10/330 Ω	
	R11/10 kΩ	
	R12-13/3 kΩ	
	R14/200 kΩ	
	R15-16/1 kΩ	
	R17/20 kΩ	
	R18-19/75 kΩ	
	R20-21/1 kΩ	
	R22/75 kΩ	
	R23-24/5 kΩ	
	R25-28/110 Ω	
	R29/5 mΩ	

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Table 13. Parts List—Slave (continued)

Component	Number/Value	Description
Capacitors	C1-4/0.1 µF	15 V mica
	C5/0.01 µF	
	C6/420 pF	
	C7-8/1.0 µF	
	C9/68 µF	
	C10/420 pF	
	C11/0.1 µF	
	C12-13/24 pF	
	C14/0.1 µF	
Connectors	J1-2/IDH-34PK-T	Robinson Nugent—34 pin
	BNC	2 BNCs
Switches	S3	6-Position
	S4	3-Position
LEDS	DIALIGHT/521-9212	

Appendix III
Transformer Information

This device is used as a broadband transformer. It connects a differential transmitter and receiver to a balanced transmission line. Splitting the line windings allows DC power to be passed over the transmission line with minimum effect to the digital communication signals.

Applications Schematic
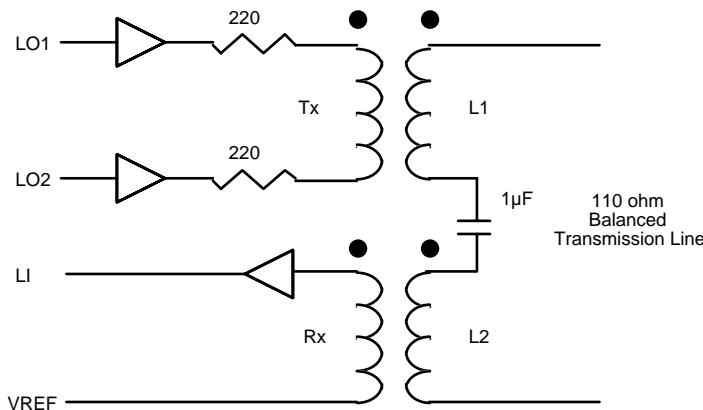
Specifications

1. Inductance: Tx inductance =1.75 mH min

2. Turns ratio: Rx (L1 + L2) = 4:1 ±2%/Tx (L1 + L2) = 2:1 ±2%

3. Bandwidth (3 dB) = 10 kHz to 500 kHz min

4. Insertion loss @ 180 kHz: line to Rx (TEST 1) <0.5 dB/Tx to line (TEST 2) <0.5 dB

5. Balance (TEST 3) 60 dB

6. DC current: through line windings series aiding, no AC parameter changes = 100 mA min

7. AC signal: signal fed to Tx winding 6 Vp-p min

8. H1POT: 1500 V AC any winding to another, and any winding to core—60 sec min

Vendors

Coilcraft Inc.	Leonard Electric Products Co
1102 Silver Lake Rd.	85 Industrial Dr.
Cary, Illinois 60013	Brownsville, Tx. 78521
Part Number: G6320-D	Part Number: P-1358-A

The transformer from Coilcraft is similar to the Leonard Electric device, except it has a Faraday shield between the Rx and Tx windings. The shield helps reduce the spurious radiation from the digital circuitry onto the twisted pair.

Test Circuit No. 1

V_L

440

Tx

L1

60

V_R

50
SOURCE

20k

Rx

L2

$$IL_{LR} = (20LOG\ V_L/V_R) + 12\ dB$$

Test Circuit No. 2

390

V_T

Tx

L1

V_L

50
SOURCE

110

20k

Rx

L2

$$IL_{TL} = (20LOG\ V_T/V_L) - 3\ dB$$

Test Circuit No. 3

$$BAL = [20LOG\,(V_L/V_R) / (V_{LB}/V_{RB})]$$
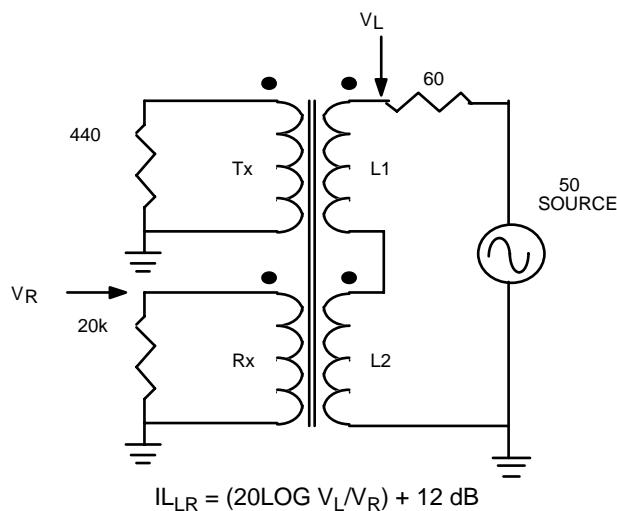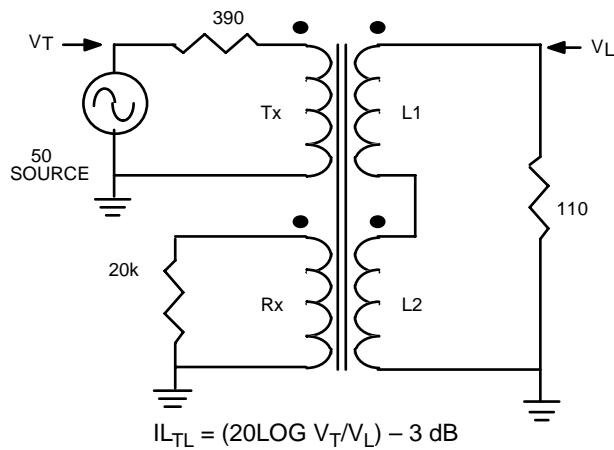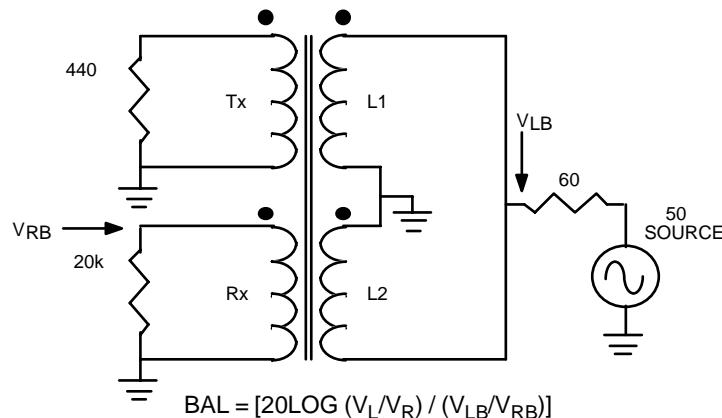
Note: V_L/V_R from Test No. 1.

Applications Circuit

* Battery feed limiting resistors; value up to user discretion
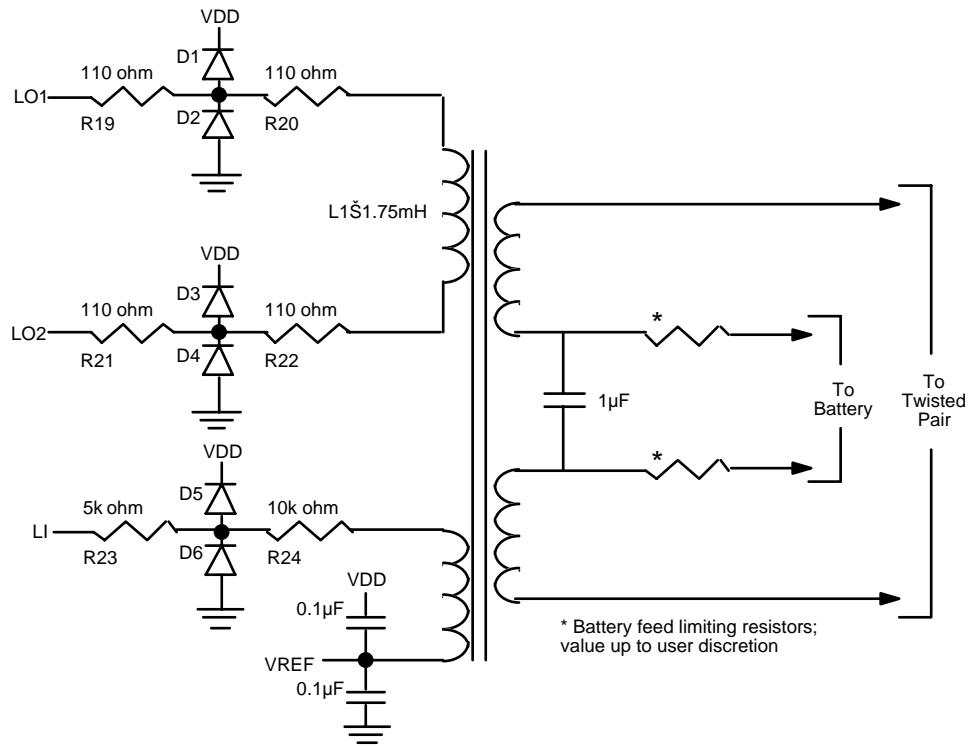
Application Circuit

At the frequencies of interest (128 kHz and 256 kHz), ordinary telephone wire has a characteristic impedance of about 110 Ω. In the schematic above, loading resistors R19–22 between LO1 and LO2 and the Tx windings of the transformer are set to 110 Ω. The series combination of these resistors is significantly higher than the 20-Ω output impedance of the LO1 and LO2 drivers, causing the resistance presented to the transformer to be set primarily by the resistors alone.

Clamp diodes D1–4 protect the LO1 and LO2 outputs from transient signals on the twisted pair. Line settling between data bursts is improved by selecting a bandwidth of 20 to 512 kHz for the transformer interface. The lower corner frequency is set by adjusting the inductance of the transformer's Tx winding to 1.75 mH. The upper corner frequency is determined by the design of the transformer winding technique.

The impedance matching network on the transmit side of the transformer attenuates the transmitted signal by 12 dB. This loss is recovered in the receive side of the transformer. A step-up of 4:1 directly compensates for the 12 dB loss. As with the transmit side, a protection network is required. D5 and D6 clamp the received signal to a safe level but are sufficiently isolated by R23 so that they do not load the transformer when they are conducting.

At 192 kHz (the spectral peak of MDPSK), 26 AWG wire attenuates signals about 17 dB/km. The receiver in the UDLT-3 has sufficient input dynamic range to operate on loops as long as 2 km.

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"MC145423EVK"

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