Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

The MC14569B is a programmable divide—by—N dual 4—bit binary or BCD down counter constructed with MOS P–Channel and N–Channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase–locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

Features

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning
- Pb-Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



http://onsemi.com

MARKING DIAGRAMS



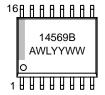
PDIP-16 P SUFFIX CASE 648 

TSSOP-16 DT SUFFIX CASE 948F





SOIC-16 DW SUFFIX CASE 751G



A = Assembly Location

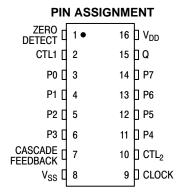
WL, L = Wafer Lot YY, Y = Year WW, W = Work Week

ORDERING INFORMATION

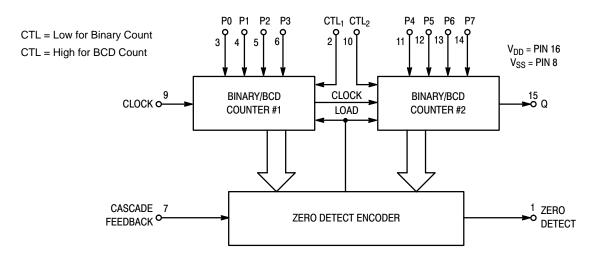
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

查询"MC14569BDWG"供应商



BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping [†]		
MC14569BCP	PDIP-16	500 Units / Rail		
MC14569BCPG	PDIP-16 (Pb-Free)	500 Units / Rail		
MC14569BDW	SOIC-16 WB	47 Units / Rail		
MC14569BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail		
MC14569BDWR2	SOIC-16 WB	1000 Units / Tape & Reel		
MC14569BDWR2G	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

	7.0 17.11	-1-3	.,	− 55°C			25°C			125°C	
Characteristic	C	Symbol	V _{DD} Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage V _{in} = V _{DD} or 0	"0" Level	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
$V_{in} = 0 \text{ or } V_{DD}$	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)		V _{IL}	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$		V _{IH}	5.0 10 15	3.5 7.0 11		3.5 7.0 11	2.75 5.50 8.25		3.5 7.0 11		Vdc
Output Drive Current $ (V_{OH} = 2.5 \text{ Vdc}) $ $ (V_{OH} = 4.6 \text{ Vdc}) $ $ (V_{OH} = 9.5 \text{ Vdc}) $ $ (V_{OH} = 13.5 \text{ Vdc}) $	Source	I _{OH}	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	- - -	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	- - - -	- 1.7 - 0.36 - 0.9 - 2.4	- - - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current		I _{in}	15	-	±0.1	_	±0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15	- - -	5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current (No (Dynamic plus Quiese Per Package) (C _L = 50 pF on all out buffers switching)	cent,	I _T	5.0 10 15			$I_{T} = (1$.58 μA/kHz) .20 μA/kHz) .95 μA/kHz)	f + I _{DD}			μAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

		V		All Types		
Characteristic	Symbol	V _{DD} Vdc	Min	Typ (Note 5)	Max	Unit
Output Rise Time	t _{TLH}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Output Fall Time	t _{THL}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Turn–On Delay Time Zero Detect Output	^t PLH	5.0 10 15	- - -	420 175 125	700 300 250	ns
Q Output		5.0 10 15	- - -	675 285 200	1200 500 400	ns
Turn–Off Delay Time Zero Detect Output	^t PHL	5.0 10 15	- - -	380 150 100	600 300 200	ns
Q Output		5.0 10 15	- - -	530 225 155	1000 400 300	ns
Clock Pulse Width	t _{WH}	5.0 10 15	300 150 115	100 45 30	- - -	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	- - -	3.5 9.5 13.0	2.1 5.1 7.8	MHz
Clock Pulse Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15		NO LIMIT		μS

^{5.} Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS

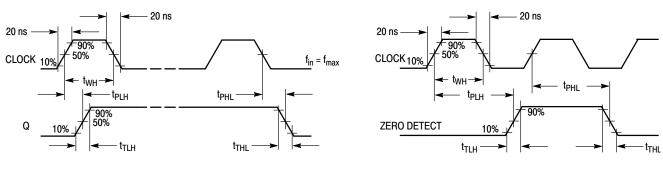


Figure 1. Figure 2.

PIN DESCRIPTIONS

查询"MC14569BDWG"供应商

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) – Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) – Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) – Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (**Pin 1**) – This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

 \mathbf{Q} (Pin 15) – Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) – This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

CTL₁ (Pin 2) – This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL₂ (Pin 10) – This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

 V_{SS} (Pin 18) – Negative Supply Voltage. This pin is usually connected to ground.

 V_{DD} (Pin 16) – Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 V to 18 V.

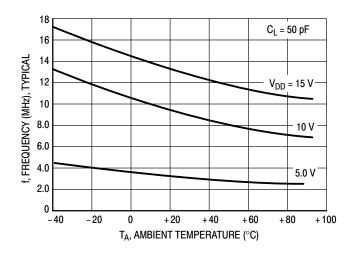
OPERATING CHARACTERISTICS

The MC14569B is a programmable divide—by—N dual 4—bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL₁ and CTL₂.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles,

one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to $V_{\rm DD}$.



查询"MC14569BDWG"供应**Table 1Mode Controls** (Cascade Feedback = Low)

Counter Cor	ntrol Values	Divide	Divide Ratio			
CTL ₁	CTL ₂	Zero Detect	Q			
0	0	256	256			
0	1	160	160			
1	0	160	160			
1	1	100	100			

NOTE: Data Preset Inputs (P0–P7) are "Don't Cares" while Cascade Feedback is Low.

 $\textbf{Table 2Mode Controls} \; (\text{CTL}_1 = \text{Low}, \; \text{CTL}_2 = \text{Low}, \; \text{Cascade Feedback} = \text{High})$

P7		Preset Inputs							Divide	e Ratio	
O	P7	P6	P5	P4	P3	P2	P1	P0		Q	Comments
O	0	0	0	0	0	0	0	0	256	256	Max Count
0 0 0 0 0 1 1 1 3 X	0	0	0	0	0	0	0	1	X	Х	Illegal State
. .	0	0	0	0	0	0	1	0	2	Х	Min Count
. .	0	0	0	0	0	0	1	1	3	X	
. .	•	•	•	•	•	•	•	•	•	Х	
0 0 0 0 1 1 1 1 15 X 0 0 0 1 0 0 0 0 16 X X X 0 0 1 0 0 0 0 0 32 X X X X X X X 	•	•	•	•	•	•	•	•	•	X	
0 0 0 1 0 0 0 0 16 X X X 0 0 1 0 0 0 0 0 32 X X X X X X X <	•	•	•	•	•	•	•	•	•		
. .	0	0	0	0	1	1	1	1	15		
. .	0	0	0	1	0	0	0	0	16	X	
. .	•	•	•	•	•	•	•	•	•	X	
0 0 1 0 0 0 0 0 32 X X X 0 1 0 0 0 0 0 64 X X X X X X <	•	•	•	•	•	•	•	•	•		
. .	•	•	•	•	•	•	•	•	•	X	
. .	0	0	1	0	0	0	0	0	32		
. .	•	•	•	•	•	•	•	•	•		
0	•	•	•	•	•	•	•	•	•	X	
. .	•	•	•	•	•	•	•	•	•		
. .	0	1	0	0	0	0	0	0	64		
. .	•	•	•	•	•	•	•	•	•		
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	•	•	•	•	•	•	•	•	•		
1 0 0 0 0 0 0 128 128 Q Output Active .	•	•	•	•	•	•	•	•	•		
1 0 <td>0</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1</td> <td></td> <td></td> <td></td> <td></td>	0						1				
1 0 0 0 1 0 0 0 136 1 0 0 0 0 0 0 0	1	0	0	0	0	0	0	0	128	128	Q Output Active
1 0 0 0 1 0 0 136 136 136 136 136 136 136 136 136 136	•	•	•	•	•	•	•	•	•	•	
1 0 0 0 0 0 136 136 • • • • • • • • • • • • • • • • • • • • •	•	•	•	•	•	•	•	•	•	•	
	•	•	•	•	•	•	•	•	-	•	
	1	0	0	0	1	0	0	0	136	136	
	•	•	•	•	•	•	•	•	•	•	
	•	•	•	•	•	•	•	•	•	•	
										_	
	1	1	1	1	1	1	1	1	255	255	▼
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	27	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	20			
128 64 32 16 8 4 2 1 Bit Value	128	64	32	16	8	4	2	1			Bit Value
Counter #2 Counter #1 Counting		Coun	ter #2			Coun	ter #1				Counting
Binary Binary Sequence											

X = No Output (Always Low)

<u>"IVIC1</u>	4569B	DVVG	Preset	inputs	- (-				Ratio	- · ·
								Zero		
P7	P6	P5	P4	P3	P2	P1	P0	Detect	Q	Comments
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	0	0	1	• 19	X	
0	0	1	0	Ö	0	0	0	20	X	
	•		•	•	•	•	•	•	X	
			.					•	X	
								•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•				•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•		•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	1	1	0	0	0	0	0	60	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	•	1	•	0	0	•	0	•	X X	
U	1		1			0		70	X	
•	•			•	•	•	•	•	X	
			:	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
:							•	•	•	
								•	•	
	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
				•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	0	0	0	0	150	150	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	1	0	0	1	159	159	Ψ
80	40	20	10	8	4	2	1			Bit Value
	Coun				Coun	ter #1				Counting
		ary			BC	D				Sequence
				1						

X = No Output (Always Low)

查询"MC14569BDWG"共和et Allow Controls (CTL₁ = Low, CTL₂ = High, Cascade Feedback = High)

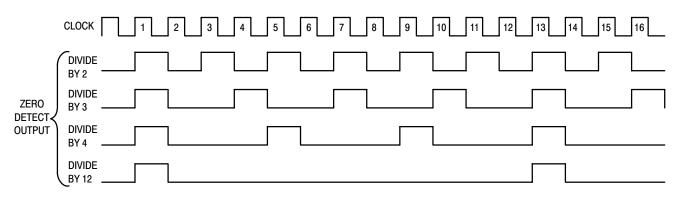
P7	IVICI	4569B		Preset	"] Values			, - 2		Ratio	
0											
0 0 0 0 0 0 0 0 0 0 0 1 1 X X X Min Count 0 0 0 0 0 0 0 0 0 1 1 0 2 X X Min Count 1 1 3 X X Min Count 1 1 3 X X Min Count 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	P7	P6	P5	P4	P3	P2	P1	P0	Detect	Q	Comments
O	0	0	0	0		0		0			
0				0		0	0				
											Min Count
	0	0	0	0	0	0	1	1	3		
0 0 0 0 0 1 1 0 0 0 0 1 1 1 1 1 1 1 1 5	•	•	•	•	•	•	•	•	•		
0 0 0 0 1 0 0 1 1 1 1 1 1 15 X 0 0 0 0 1 1 0 0 0 0 0 16 X 1	•	•	•	•	•	•	•	•	•		
0											
	0	0		1							
	•			•							
0											
0											
	0	0									
. .	•	•									
0	•	•									
	0	0									
			i :	:							
0											
0	•									•	
	0	1	0						64	X	
. .			_								
0	•	•	•	•	•	•	•	•	•		
. .	•		•	•	•	•	•	•	•		
	0	1	0	1	0	0	0	0	80	X	
0 1 1 1 0 0 0 0 112 X 1 0 0 0 0 0 112 X 1 0 0 0 0 0 0 128 128 Q Output Active 1 0 0 0 0 0 0 128 128 Q Output Active 1 0 0 1 0 0 0 0 144 144 1 0 0 1 0 0 0 0 144 144 1 0 0 1 1 1 1 1 159 159 27 26 25 24 23 22 21 20 128 64 32 16 8 4 2 1 Bit Value Counter#2 Counter#1	•	•	•	•	•	•	•	•	•	•	
0	•	•	•	•	•	•	•	•	•	•	
. .	•	•	•	•	•	•	•	•		•	
. .	0	1	1	1	0	0	0	0	112	X	
1 0 0 0 0 0 0 0 128 128 Q Output Active 1 0 0 0 0 0 128 128 Q Output Active 1 0 0 1 0 0 0 0 144 144 1 0 0 1 0 0 0 0 144 144 1 0 0 1 1 1 1 159 159 27 26 25 24 23 22 21 20 128 64 32 16 8 4 2 1 Counter #2 Counter #1	•	•	•	•	•	•	•	•	•	•	
1 0 0 0 0 0 0 128 128 Q Output Active 1 0 0 1 0 0 0 0 144 144 1 0 0 1 0 0 0 144 144 1 0 0 1 1 1 1 159 159 27 26 25 24 23 22 21 20 128 64 32 16 8 4 2 1 Bit Value Counter #1 Counting	•	•	•	•	•	•	•	•	•	•	
. .	•								•	•	
. .	1	0	0	0	0	0	0	0	128	128	Q Output Active
1 0 0 1 0 0 0 0 0 144 144 1 0 0 1 0 0 0 0 144 144 1 0 0 1 1 1 1 1 159 159 27 26 25 24 23 22 21 20 <	•	•								•	
1 0 0 1 0 0 0 0 144 144 . </td <td>•</td> <td>•</td> <td></td> <td>•</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>•</td> <td></td>	•	•		•						•	
1 0 0 1 1 1 1 1 1 159 159 27 26 25 24 23 22 21 20 128 64 32 16 8 4 2 1 Bit Value Counter #2 Counter #1 Counting	•	•		4							
1 0 0 1 1 1 1 1 159 159 27 26 25 24 23 22 21 20 128 64 32 16 8 4 2 1 Bit Value Counter #2 Counter #1	1	U	0	'	U	U	U	U	144	144	
1 0 0 1 1 1 1 1 159 159 27 26 25 24 23 22 21 20 128 64 32 16 8 4 2 1 Bit Value Counter #2 Counter #1	•	•	•	•	•	•	•	•	•		
1 0 0 1 1 1 1 159 159 \mathred{\textbf{V}} 27 26 25 24 23 22 21 20 128 64 32 16 8 4 2 1 Bit Value Counter #2 Counter #1		•	•			•	•		•		
27 26 25 24 23 22 21 20 128 64 32 16 8 4 2 1 Bit Value Counter #2 Counter #1 Counting		0	0	1	1				159	159	₩
128 64 32 16 8 4 2 1 Bit Value Counter #2 Counter #1 Counting										1	
Counter #2 Counter #1 Counting BCD Binary Sequence											Bit Value
BCD Binary Sequence		Coun	ter #2	•		Count	er #1				Counting
, , , , , , , , , , , , , , , , , , , ,											Sequence

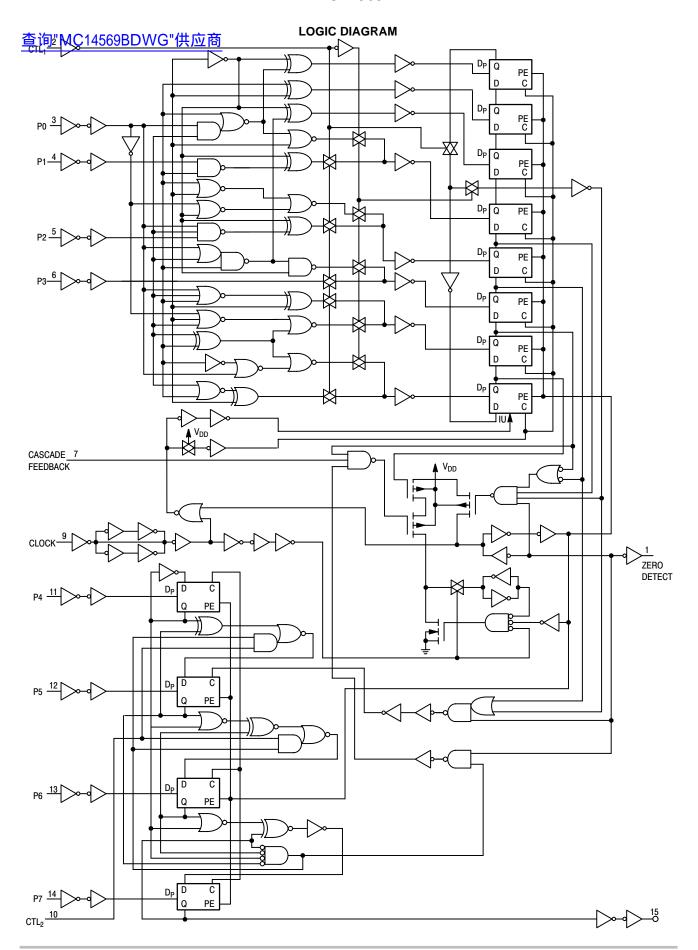
X = No Output (Always Low)

BI <u>II</u> VIL.	<u>////////////////////////////////////</u>	VV(¬"1共 /\V /								
,			Preset	Values				Divide	Ratio	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	100	100	Max Count
0	0	0	0	0	0	0	1	X	X	illegal state
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	Х	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	0	0	1	99	• 99	↓
80	40	20	10	8	4	2	1	33	99	Bit Value
- 60			10	٥			_ '			
		ter #2 CD			Coun B0					Counting
	B	טכ			B(טי				Sequence

X = No Output (Always Low)

TIMING DIAGRAM MC14569B





查询"MC14569BDWG"供应商

TYPICAL APPLICATIONS

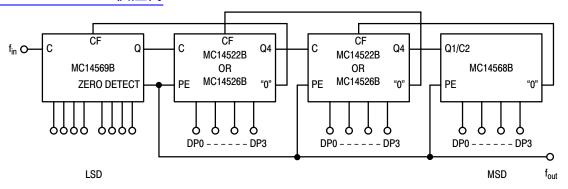


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B

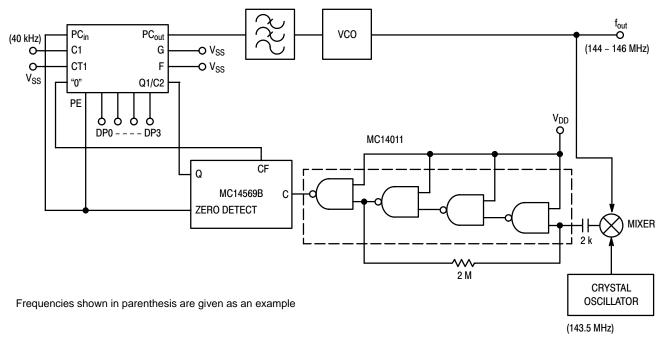
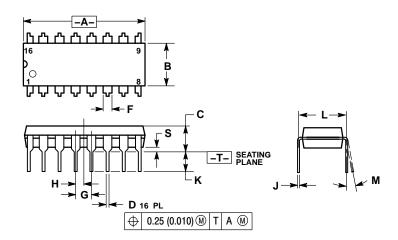


Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

查询"MC14569BDWG"供应商

PACKAGE DIMENSIONS

PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08 **ISSUE T**



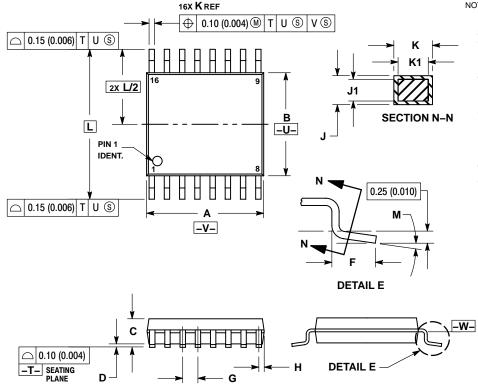
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL. 3.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.

 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54	BSC	
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295 0.305		7.50	7.74	
М	0° 10°		0°	10 °	
S	0.020	0.040	0.51	1.01	

TSSOP-16 **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948F-01 **ISSUE A**



NOTES:

- OTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

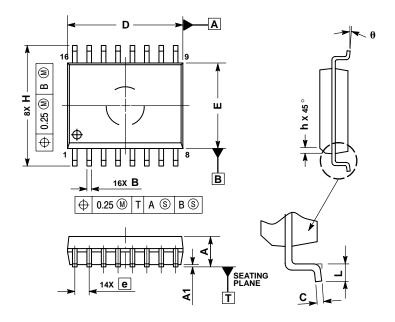
 5. DIMENSION K DOES NOT INCLUDE
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
C		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
H	0.18	0.28	0.007	0.011	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
M	0°	8°	0°	8 °	

查询"MC14569BDWG"供应商

PACKAGE DIMENSIONS

SOIC-16 WB **DW SUFFIX** PLASTIC SOIC PACKAGE CASE 751G-03 ISSUE C



NOTES:

- NOTES:

 1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETER						
DIM	MIN	MAX					
Α	2.35	2.65					
A1	0.10	0.25					
В	0.35	0.49					
С	0.23	0.32					
D	10.15	10.45					
E	7.40	7.60					
е	1.27	BSC					
Н	10.05	10.55					
h	0.25	0.75					
L	0.50	0.90					
а	0 °	7 °					

查询"MC14569BDWG"供应商

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability, arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082–1312 USA Phone: 480–829–7710 or 800–344–3860 Toll Free USA/Canada Fax: 480–829–7709 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center 2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051 Phone: 81–3–5773–3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.