

OptiMOS[®]-P Trench Power-Transistor



Features

- P-channel - Logic Level - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS Compliant)
- Ultra low Rds(on)
- 100% Avalanche tested
- Intended for reverse battery protection

Product Summary

V_{DS}	-30	V
$R_{DS(on),max}$ (SMD version)	4	mΩ
I_D	-100	A

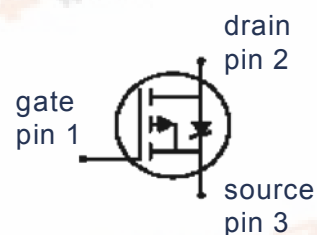
PG-TO263-3-2

PG-TO262-3-1

PG-TO220-3-1



Type	Package	Marking
IPB100P03P3L-04	PG-TO263-3-2	3P03L04
IPI100P03P3L-04	PG-TO262-3-1	3P03L04
IPP100P03P3L-04	PG-TO220-3-1	3P03L04



Maximum ratings, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25^\circ\text{C}$, $V_{GS}=-10\text{V}$	-100	A
		$T_C=100^\circ\text{C}$, $V_{GS}=-10\text{V}^{(2)}$	-100	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25^\circ\text{C}$	-400	
Avalanche energy, single pulse	E_{AS}	$I_D=-80\text{A}$	450	mJ
Gate source voltage	V_{GS}		-16 / +5	V
Power dissipation	P_{tot}	$T_C=25^\circ\text{C}$	200	W
Operating and storage temperature	T_j, T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}		-	-	0.65	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-475\mu A$	-1	-1.5	-2.1	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V, T_j=25\text{ °C}$	-	-0.1	-1	μA
		$V_{DS}=-30V, V_{GS}=0V, T_j=125\text{ °C}^{2)}$	-	-10	-100	
Gate-source leakage current	I_{GSS}	$V_{GS}=-16V, V_{DS}=0V$	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-50A$	-	4.8	7.6	m Ω
		$V_{GS}=-4.5V, I_D=-50A$, SMD version	-	4.5	7.3	
		$V_{GS}=-10V, I_D=-80A$	-	3.3	4.3	
		$V_{GS}=-10V, I_D=-80A$, SMD version	-	3.0	4	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$	-	7150	9300	pF
Output capacitance	C_{oss}		-	2150	2800	
Reverse transfer capacitance	C_{rss}		-	1650	2500	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-15V,$ $V_{GS}=-10V, I_D=-50A,$ $R_G=6\Omega$	-	30	-	ns
Rise time	t_r		-	45	-	
Turn-off delay time	$t_{d(off)}$		-	200	-	
Fall time	t_f		-	180	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-24V,$ $I_D=-80A,$ $V_{GS}=0$ to $-10V$	-	25	33	nC
Gate to drain charge	Q_{gd}		-	55	82.5	
Gate charge total	Q_g		-	150	200	
Gate plateau voltage	$V_{plateau}$		-	-3.0	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_A=25^\circ C$	-	-	-100	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_A=25^\circ C$	-	-	-400	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=-80A$	-0.6	-1	-1.2	V
Reverse recovery time ²⁾	t_{rr}	$V_R=-15V, I_F=-50A,$ $di_F/dt=100A/\mu s$	-	50	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	55	-	nC

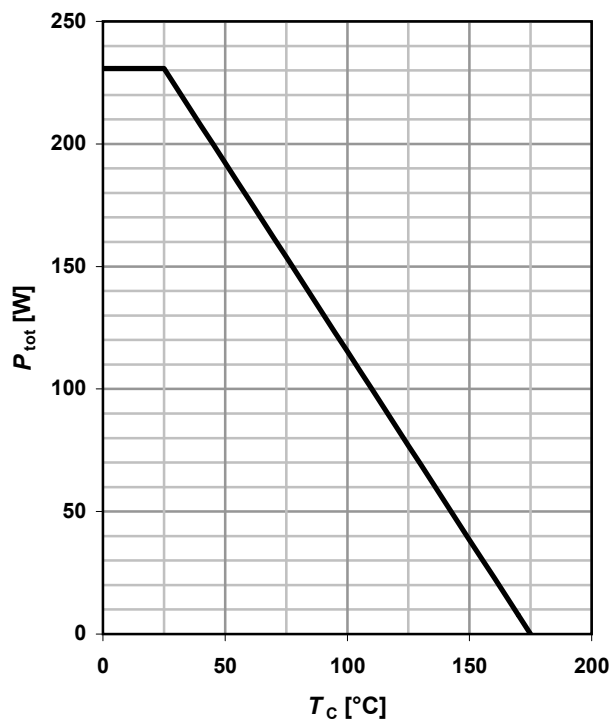
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.65$ K/W the chip is able to carry $I_D=-195A$ at $25^\circ C$. For detailed information see Application Note ANPS071E at www.infineon.com/optimos

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

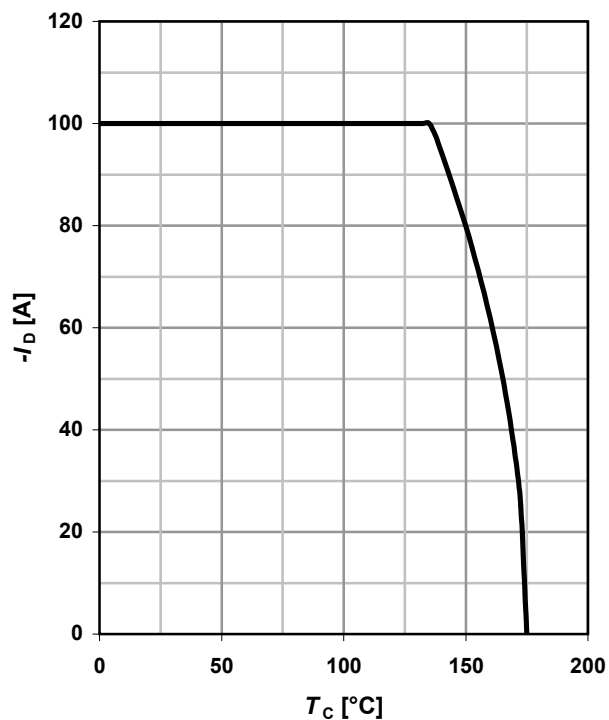
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \leq -4 \text{ V}$$



2 Drain current

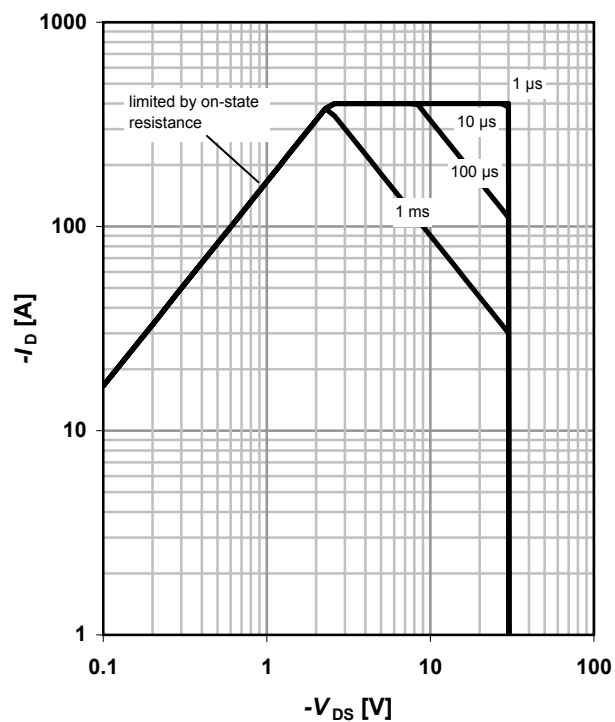
$$I_D = f(T_C); V_{\text{GS}} \leq -4 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

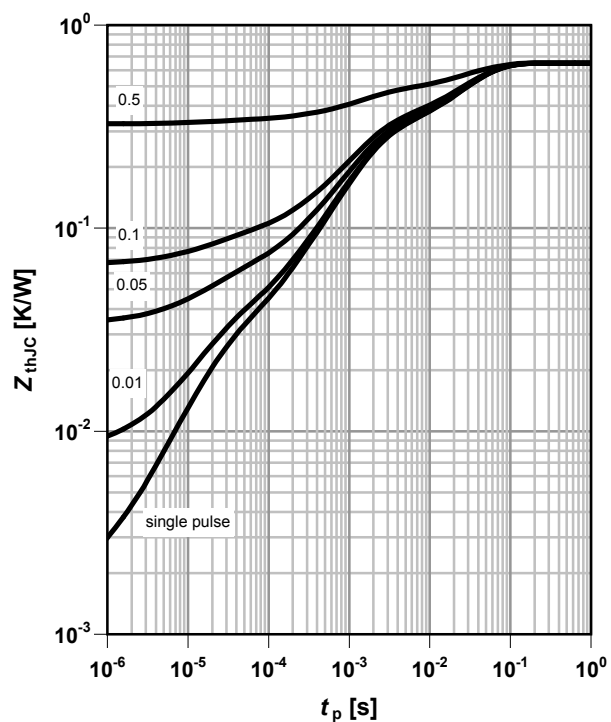
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

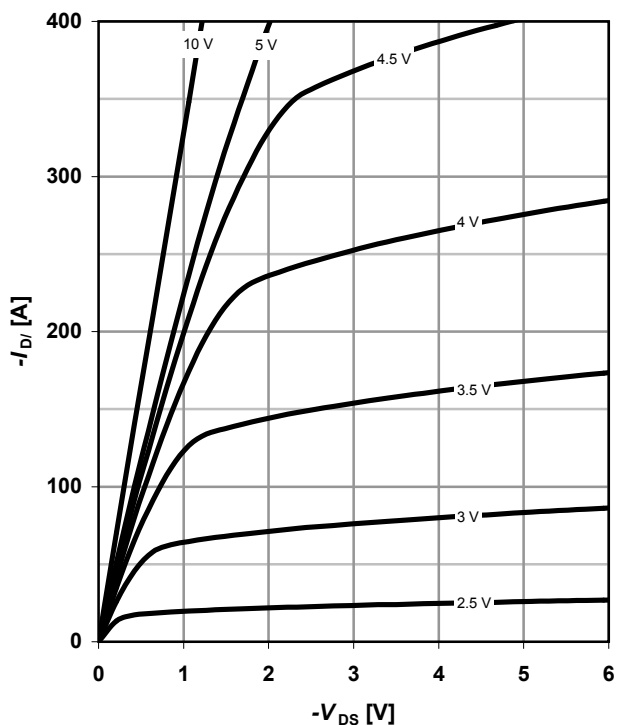
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

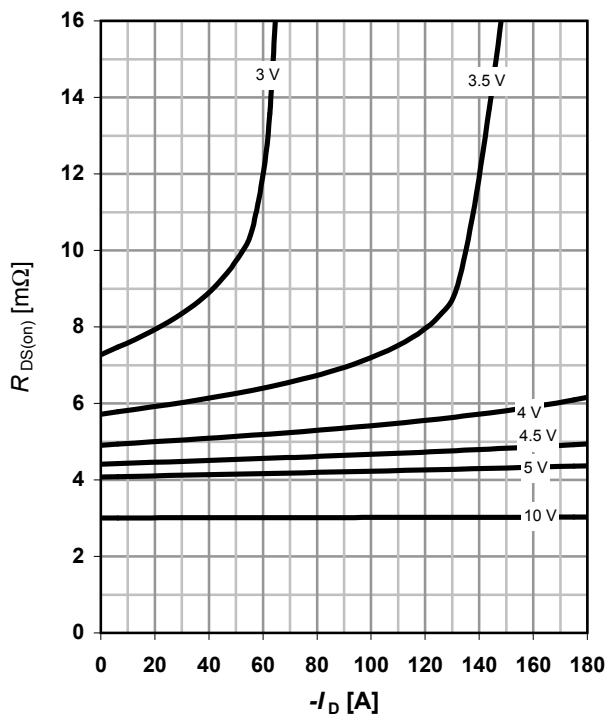
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

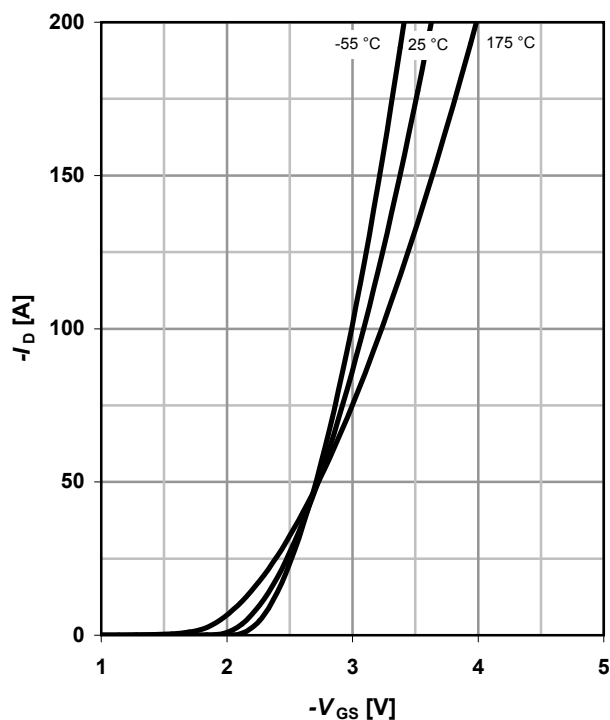
parameter: V_{GS}



7 Typ. transfer characteristics

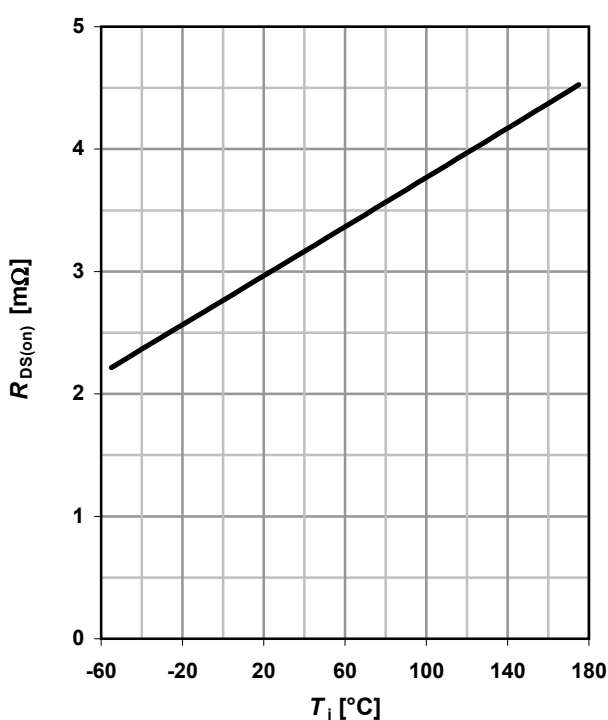
$I_D = f(V_{GS}); V_{DS} = 4\text{ V}$

parameter: T_j



8 Typ. drain-source on-state resistance

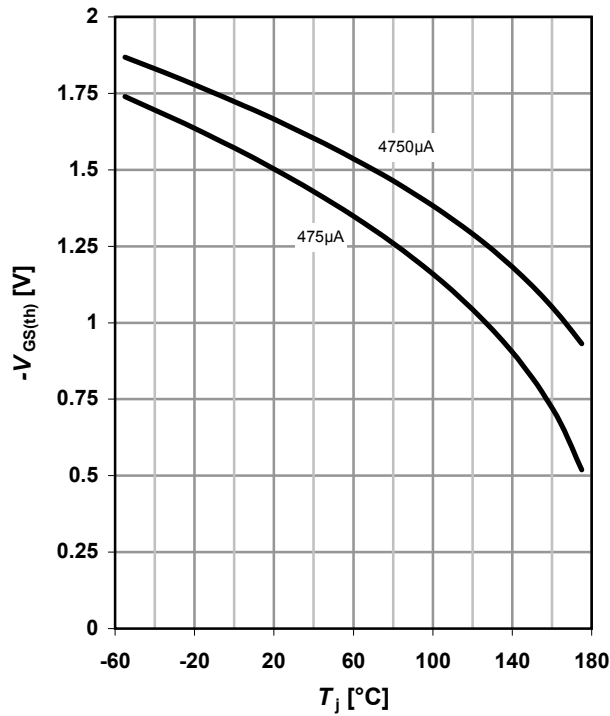
$R_{DS(on)} = f(T_j); I_D = -80\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

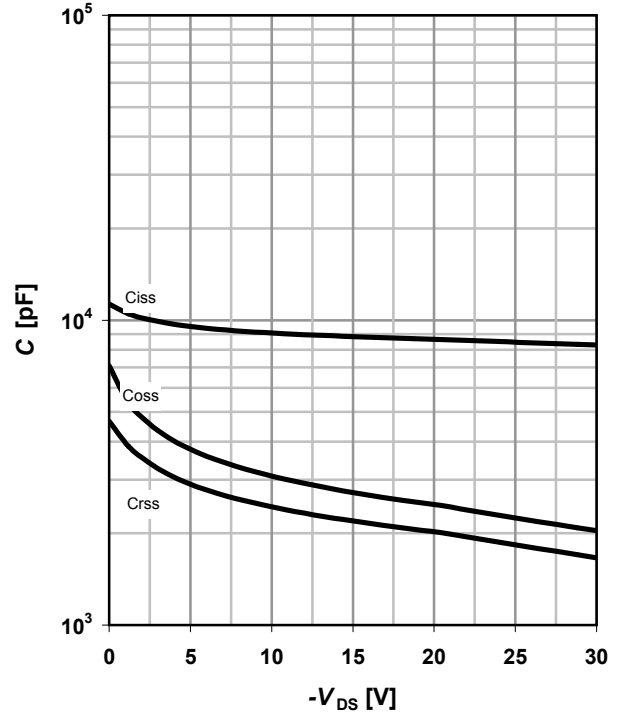
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

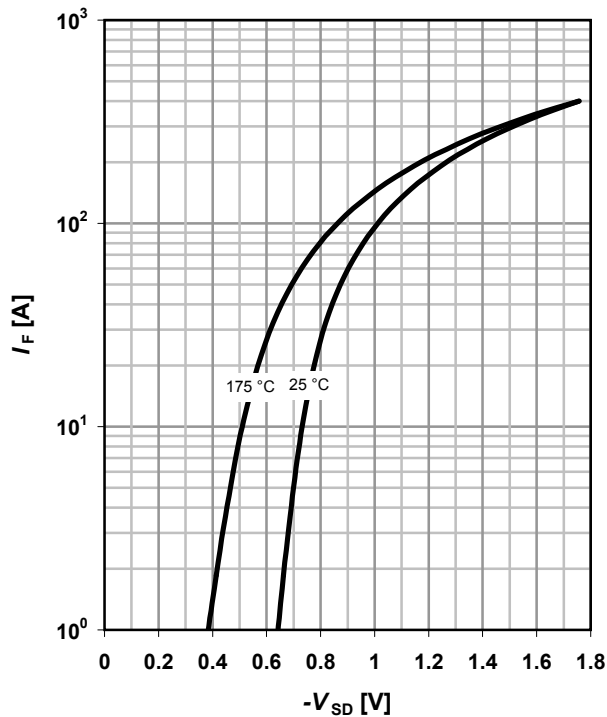
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

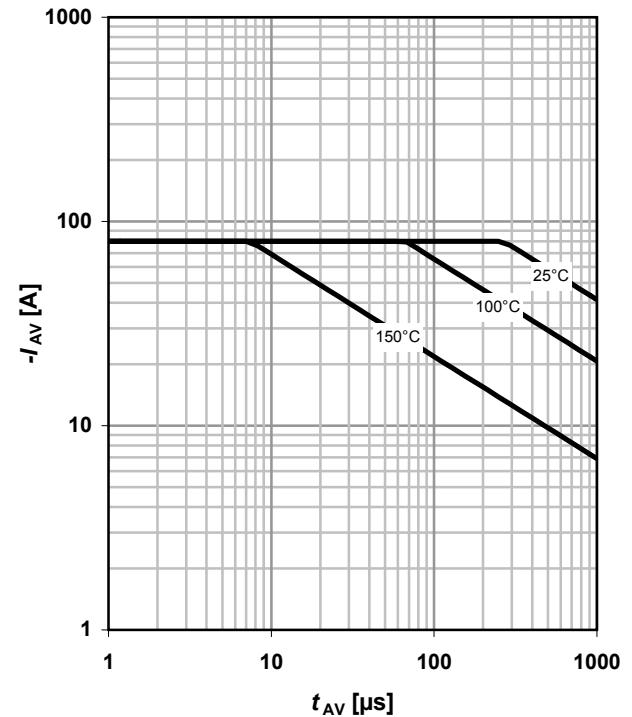
parameter: T_j



12 Typ. avalanche characteristics

$I_{AV} = f(t_{AV})$

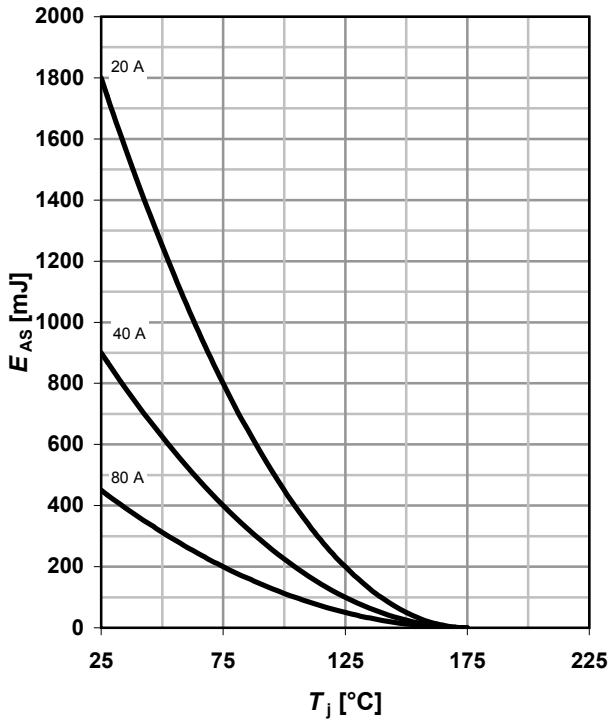
parameter: $T_{j(start)}$



13 Typical avalanche energy

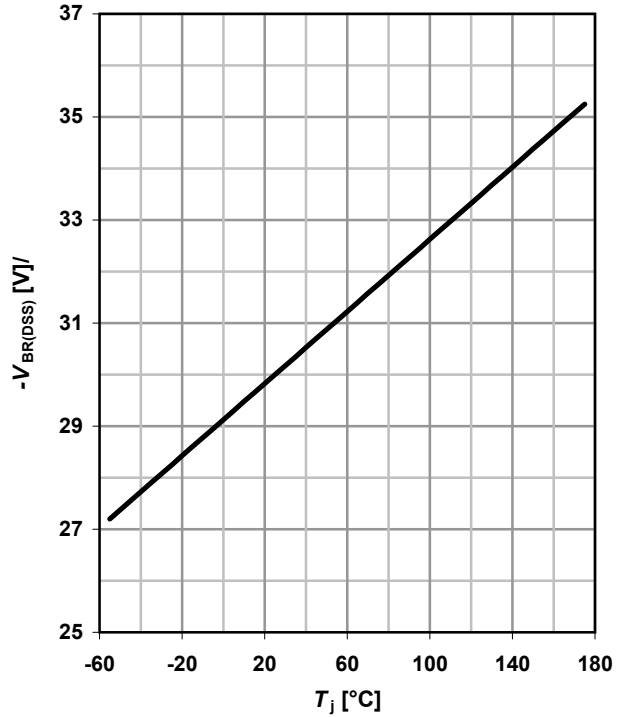
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

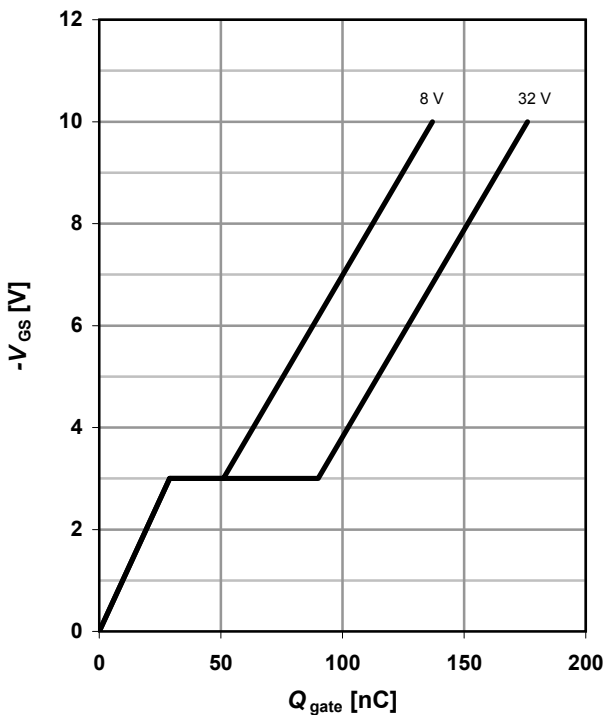
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$



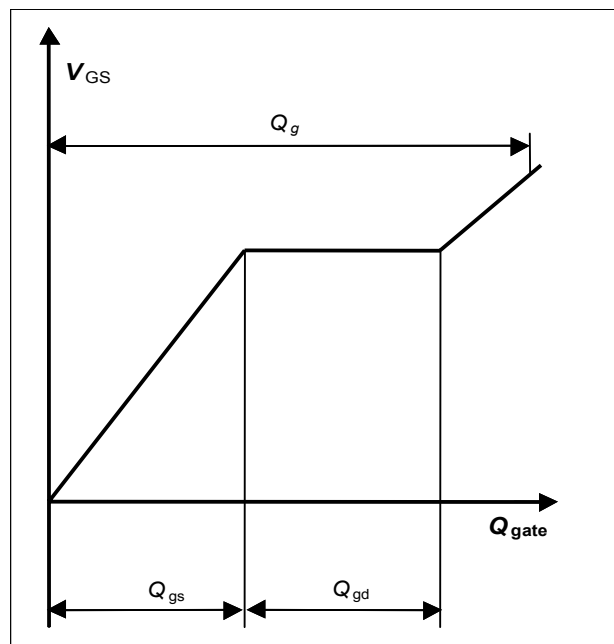
15 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = 80 \text{ A pulsed}$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Rev 1.1	25.09.2007	Type on page 1 changed from IP_100P06P3L-04 to IP_100P03PL04

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