16-Mbit (2M x 8) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.20V – 3.60V
- Ultra low standby power
  - Typical standby current: 1.5 µA
  - Maximum standby current: 12 µA
- Ultra low active power
  - Typical active current: 2.2 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-ball FBGA package. For Pb-free 48-pin TSOP I package, refer to CY62167EV30 data sheet.

Functional Description[1]

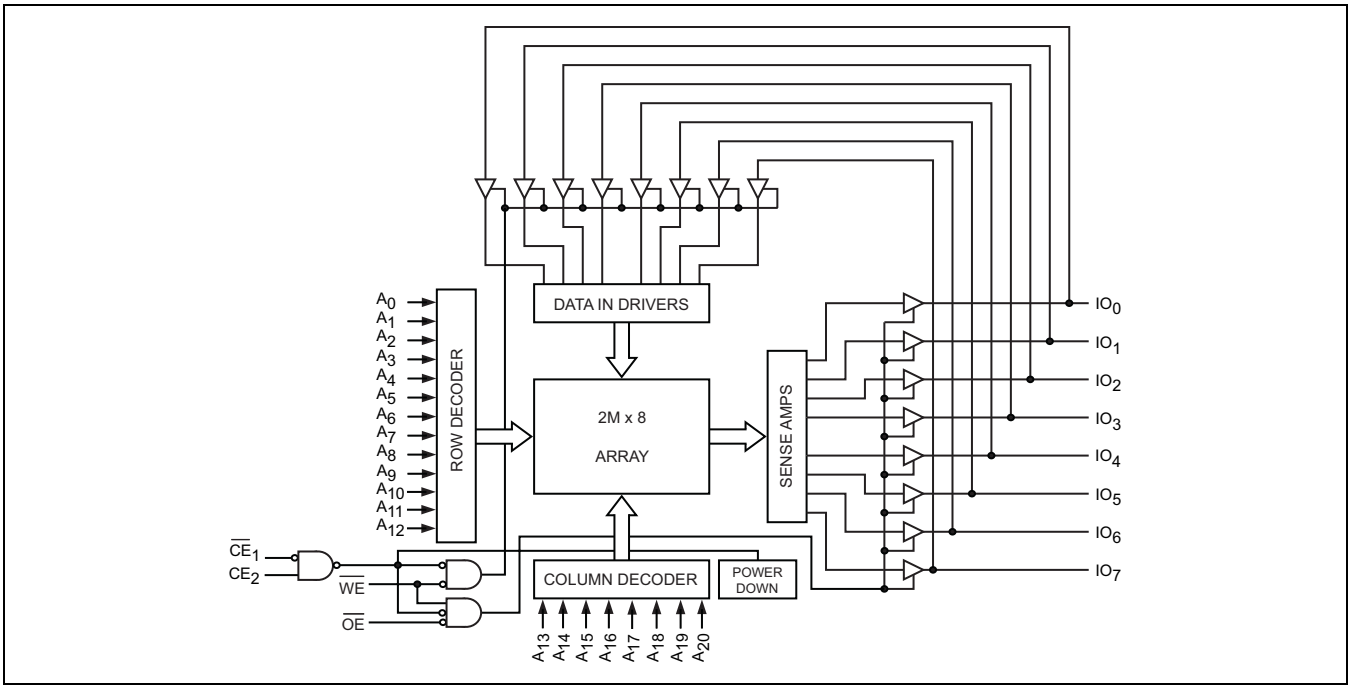
The CY62168EV30 is a high performance CMOS static RAM organized as 2M words by 8 bits. This device features advanced circuit design to provide an ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 90% when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW). The input and output pins (IO_0 through IO_7) are placed in a high impedance state when: the device is deselected (Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW), outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress (Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and $\overline{WE}$ LOW).

Write to the device by taking Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and the Write Enable (WE) input LOW. Data on the eight IO pins (IO_0 through IO_7) is then written into the location specified on the address pins (A_0 through A_{20}).

Read from the device by taking Chip Enable 1 ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW and Chip Enable 2 (CE_2) HIGH while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the IO pins.

The eight input and output pins (IO_0 through IO_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ LOW and CE_2 HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW). See the "Truth Table" on page 8 for a complete description of read and write modes.

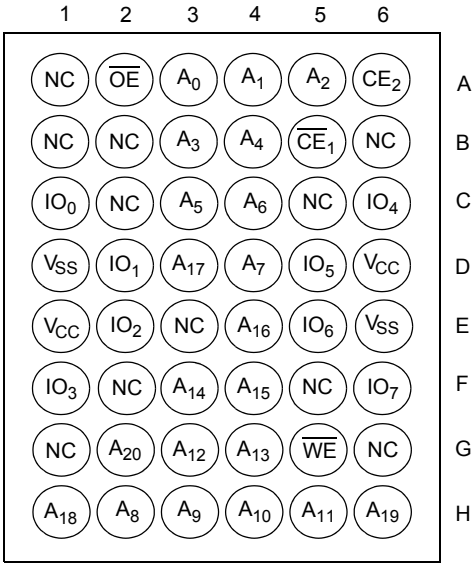
Logic Block Diagram



Note
1. For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Pin Configuration [2]

48-Ball FBGA Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[3]	Max		Typ[3]	Max	Typ[3]	Max	Typ[3]	Max
CY62168EV30LL	2.2	3.0	3.6	45	2.2	4.0	25	30	1.5	12

Notes
2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25°C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.3V to V_{CC}(max) + 0.3V

DC Voltage Applied to Outputs in High-Z State[4, 5] ..... –0.3V to V_{CC}(max) + 0.3V

DC Input Voltage[4, 5] ..... –0.3V to V_{CC}(max) + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (MIL-STD-883, Method 3015)

Latch up Current..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)[6]	V_{CC}[7]
Industrial	–40°C to +85°C	2.2V – 3.6V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		CY62168EV30-45			Unit
				Min	Typ[3]	Max	
V_{OH}	Output HIGH Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0			V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4			
V_{OL}	Output LOW Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA			0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = 2.1 mA			0.4	
V_{IH}	Input HIGH Voltage	$2.2 \le V_{CC} \le 2.7$		1.8		V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2		V_{CC} + 0.3	
V_{IL}	Input LOW Voltage	$2.2 \le V_{CC} \le 2.7$		–0.3		0.6	V
		$2.7 \le V_{CC} \le 3.6$		–0.3		0.8	
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		–1		+1	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	V_{CC} = 3.6V, I_{OUT} = 0 mA, CMOS level		25	30	mA
		f = 1 MHz			2.2	4.0	
I_{SB1}	Automatic CE Power Down Current — CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2V$, $CE_2 \le 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$, $V_{IN} \le 0.2V$, f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$)			1.5	12	µA
I_{SB2}[8]	Automatic CE Power Down Current— CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2V$, $CE_2 \le 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0, V_{CC} = 3.6V			1.5	12	µA

Capacitance[9]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = V_{CC}(typ)	8	pF
C_{OUT}	Output Capacitance		10	pF

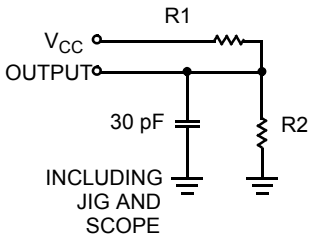
Notes

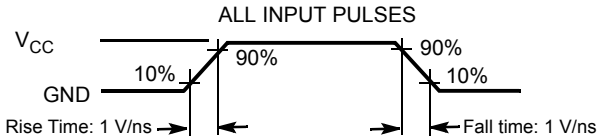
4. V_{IL}(min) = –0.2V for pulse durations less than 20 ns.
5. V_{IH}(max) = V_{CC} + 0.75V for pulse durations less than 20 ns.
6. T_A is the "Instant-On" case temperature.
7. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 100 µs wait time after V_{CC} stabilization.
8. Only chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
9. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance[9]

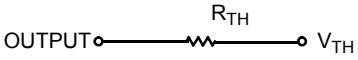
Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		16	°C/W

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



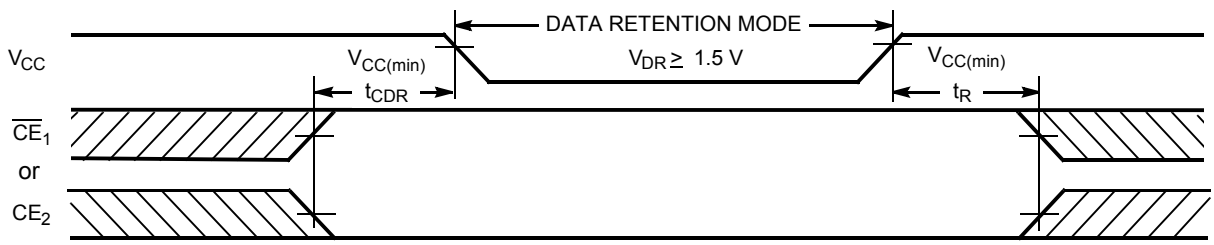
Parameters	2.5V (2.2V to 2.7V)	3.0V (2.7V to 3.6V)	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.2	1.75	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ[3]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5		3.6	V
I_{CCDR}[8]	Data Retention Current	V_{CC} = 1.5V $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			10	µA
t_{CDR}[9]	Chip Deselect to Data Retention Time		0			ns
t_R[10]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Note

10. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC}(min) \geq 100\ \mu s$ or stable at $V_{CC}(min) \geq 100\ \mu s$.

Switching Characteristics

Over the Operating Range [11]

Parameter	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[12]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[12, 13]		18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[12]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z[12, 13]		18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power Down		45	ns
Write Cycle[14]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35		ns
t_{AW}	Address Setup to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		ns
t_{SD}	Data Setup to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[12, 13]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[12]	10		ns

Notes

11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1V/ns), timing reference levels of V_{CC}(typ)/2, input pulse levels of 0 to V_{CC}(typ), and output loading of the specified I_{OL}/I_{OH} as shown in "AC Test Loads and Waveforms" on page 4.
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
13. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
14. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 1 shows address transition controlled read cycle waveforms.[15, 16]

Figure 1. Read Cycle No. 1

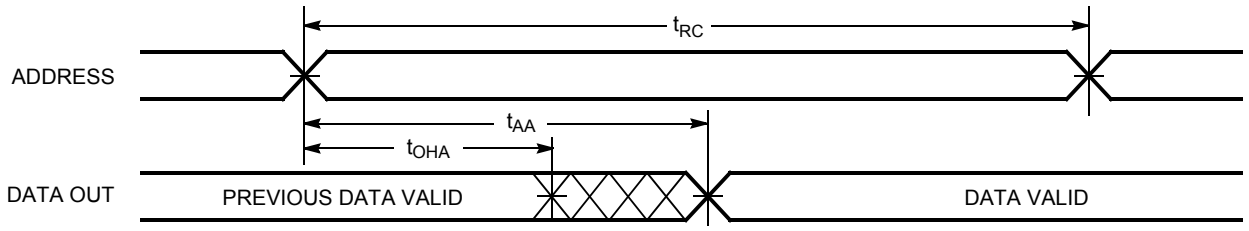
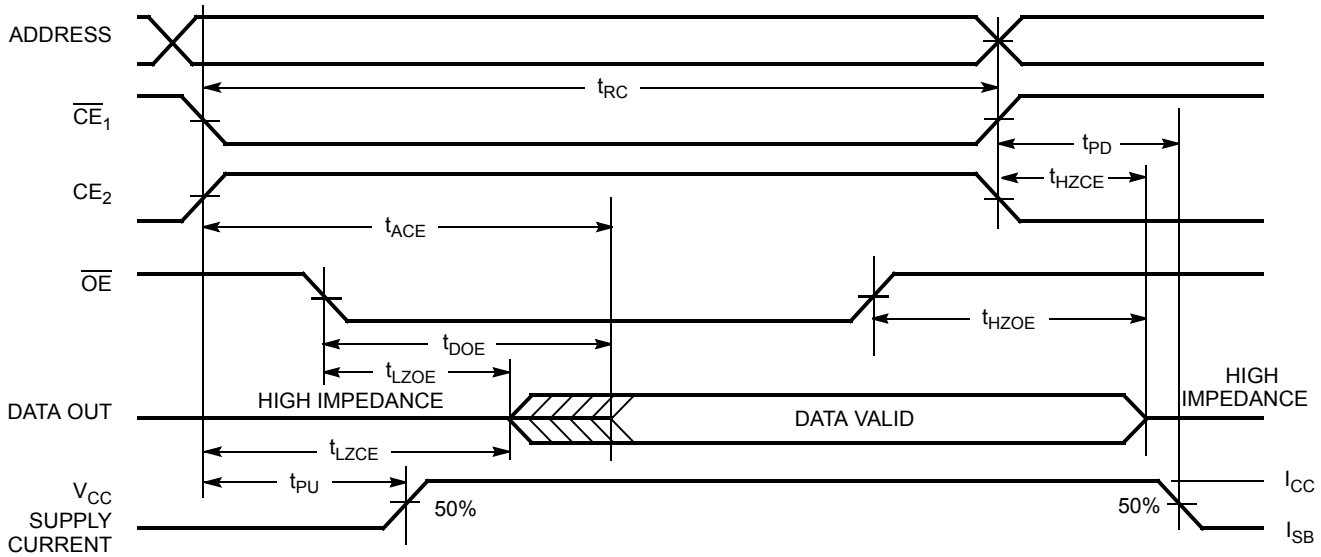


Figure 2 shows $\overline{OE}$ controlled read cycle waveforms.[16, 17]

Figure 2. Read Cycle No. 2



Notes
15. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid before or similar to $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 3 shows $\overline{WE}$ controlled write cycle waveforms.[14, 18, 19]

Figure 3. Write Cycle No. 1

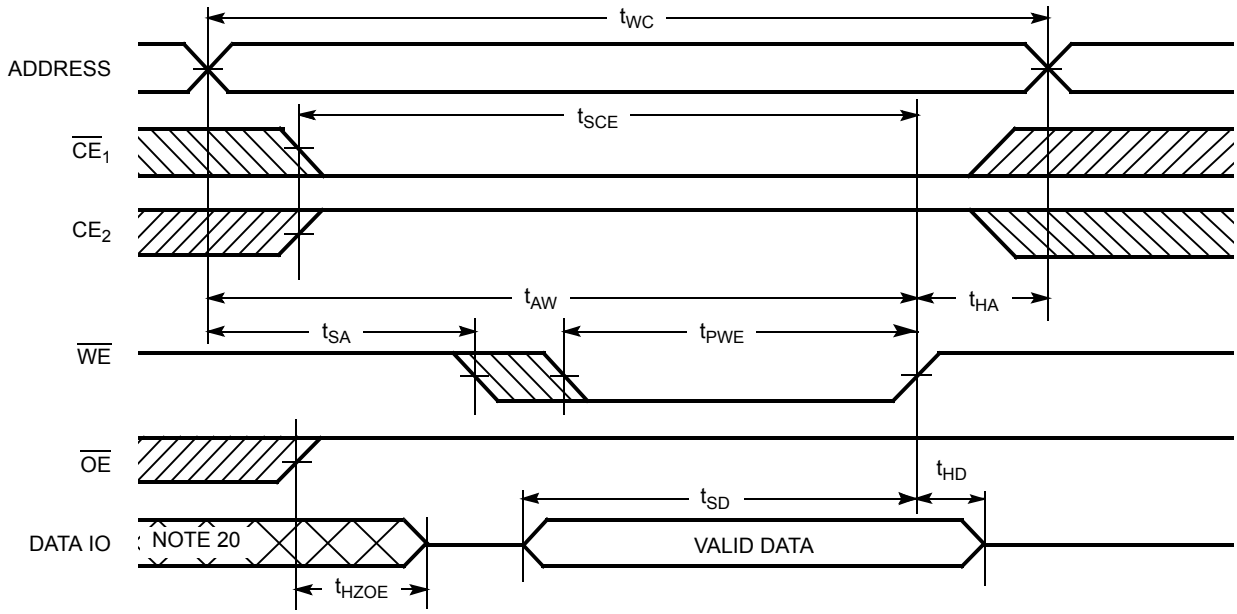
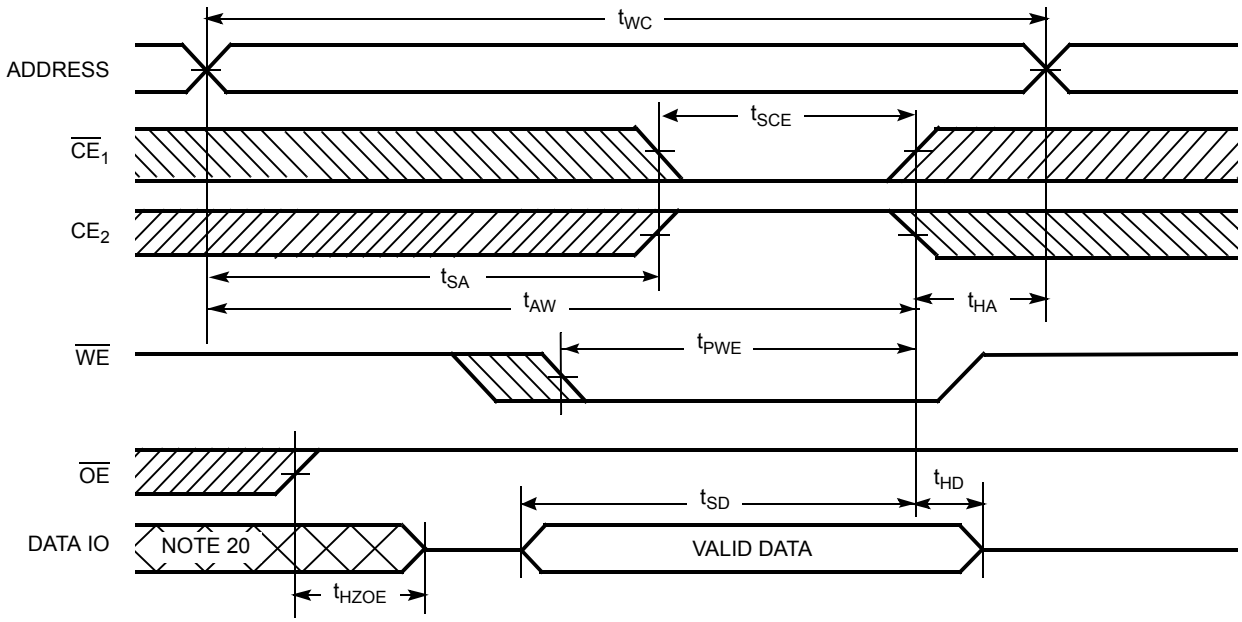


Figure 4 shows $\overline{CE}_1$ or CE_2 controlled write cycle waveforms.[14, 18, 19]

Figure 4. Write Cycle No. 2

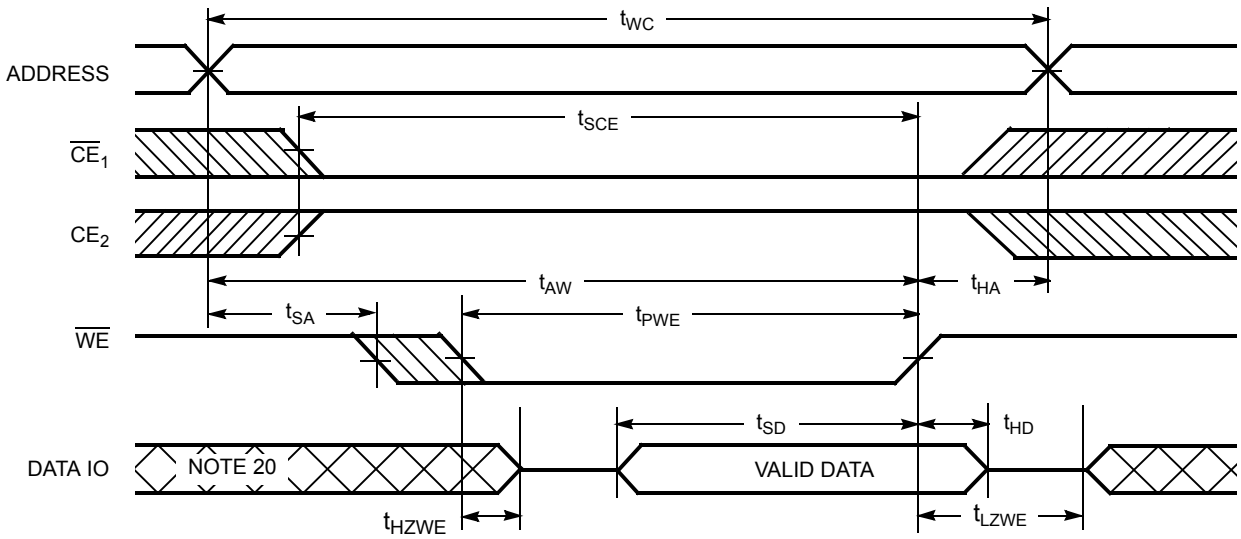


Notes
18. Data IO is high impedance if $\overline{OE} = V_{IH}$.
19. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
20. During this period the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 5 shows $\overline{WE}$ controlled, $\overline{OE}$ LOW write cycle waveforms.[19]

Figure 5. Write Cycle No. 3



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	Data Out (IO_0-IO_7)	Read	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	Data in (IO_0-IO_7)	Write	Active (I_{CC})

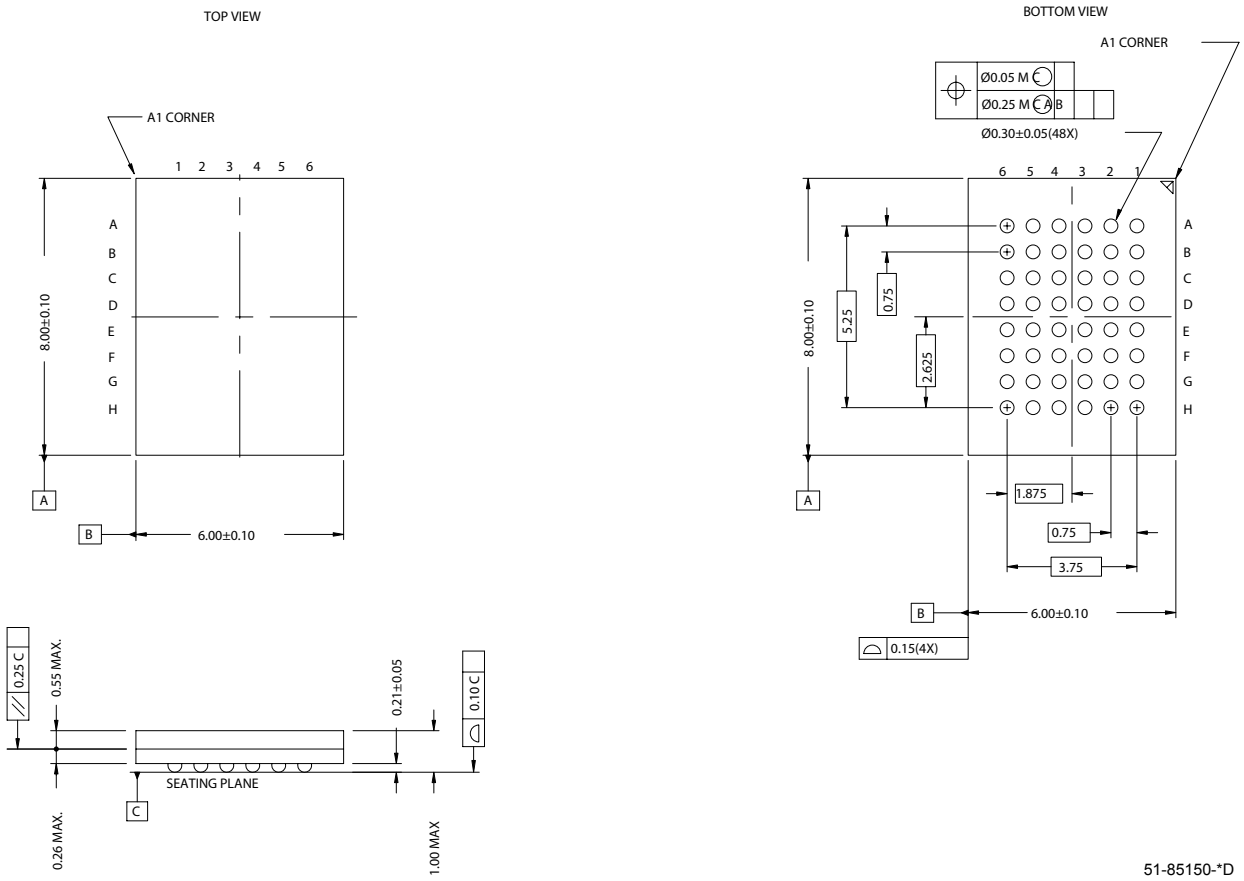
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62168EV30LL-45BVXI	51-85150	48-ball Fine Pitch BGA (Pb-free)	Industrial

Contact your local Cypress sales representative for availability of these parts.

Package Diagrams

Figure 6. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150



Document History Page

Document Title: CY62168EV30 MoBL® 16-Mbit (2M x 8) Static RAM Document Number: 001-07721				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	457686	See ECN	NXR	New Data Sheet
*A	464509	See ECN	NXR	Removed TSOP I package; Added reference to CY62167EV30 TSOP I package which can be used as a 2M x 8 SRAM Changed the $I_{SB2(Typ)}$ value from 1.3 μA to 1.5 μA Changed the $I_{CC(Typ)}$ value from 2 mA to 2.2 mA for f=1MHz Test condition Changed the $I_{CC(Typ)}$ value from 15 mA to 22 mA and $I_{CC(Max)}$ value from 40 mA to 25 mA for f=1MHz Test condition Changed the $I_{CCDR(Max)}$ value from 8.5 μA to 8 μA
*B	1138883	See ECN	VKN	Converted from preliminary to final Changed $I_{CC(max)}$ spec from 2.8 mA to 4.0 mA for f=1MHz Changed $I_{CC(typ)}$ spec from 22 mA to 25 mA for f=f_{max} Changed $I_{CC(max)}$ spec from 25 mA to 30 mA for f=f_{max} Added footnote# 8 related to I_{SB2} and I_{CCDR} Changed I_{SB1} and I_{SB2} spec from 8.5 μA to 12 μA Changed I_{CCDR} spec from 8 μA to 10 μA