

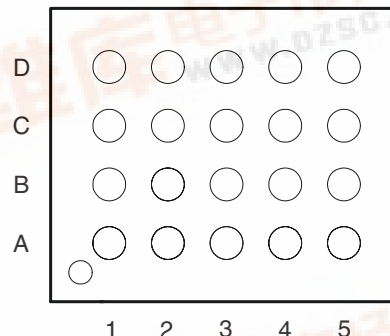
1-GHz BANDWIDTH, 8-CHANNEL SPST SWITCH

Check for Samples: [TS2DDR2811](#)

FEATURES

- Wide Bandwidth (BW = 1100 MHz Typ)
- Low Crosstalk ($X_{TALK} = -37$ dB Typ)
- Low Bit-to-Bit Skew ($t_{sk(o)} = 100$ ps Max)
- Low and Flat ON-State Resistance ($r_{ON} = 4 \Omega$ Typ, $r_{ON(flat)} = 0.5 \Omega$ Typ)
- Low Input/Output Capacitance ($C_{ON} = 8$ pF Typ)
- Rail-to-Rail Switching on Data I/O Ports (0 V to 5 V)
- V_{CC} Operating Range From 3 V to 3.6 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

ZXY PACKAGE
(BOTTOM VIEW)



TERMINAL ASSIGNMENTS

D	B ₆	B ₅	B ₃	SEL	B ₀
C	B ₇	B ₄	B ₂	B ₁	N.C.
B	GND	A ₅	A ₃	A ₁	V _{CC}
A	A ₇	A ₆	A ₄	A ₂	A ₀
	1	2	3	4	5

APPLICATIONS

- DDR2 Signal Switching
- GbE LAN Signal Switching
- Hub and Router Signal Switching
- Audio/Video Switching

DESCRIPTION/ORDERING INFORMATION

The TS2DDR2811 is a 8-channel single-pole single-throw (SPST) signal switch capable of switching signals with bandwidth in excess of 1 GHz. The device includes a select pin (SEL) that is used to select any 1 of the 8 channel inputs. This select pin controls the data path of the SPST switch. The device provides a low and flat ON-state resistance (r_{ON}) and an excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various high-bandwidth applications, such as DDR2, 10/100/1000 Base-T, audio, and video.

Table 1. ORDERING INFORMATION

T _A	PACKAGE ^{(1) (2)}		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	BGA – ZXY	Tape and reel	TS2DDR2811ZXYR	SJ811

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

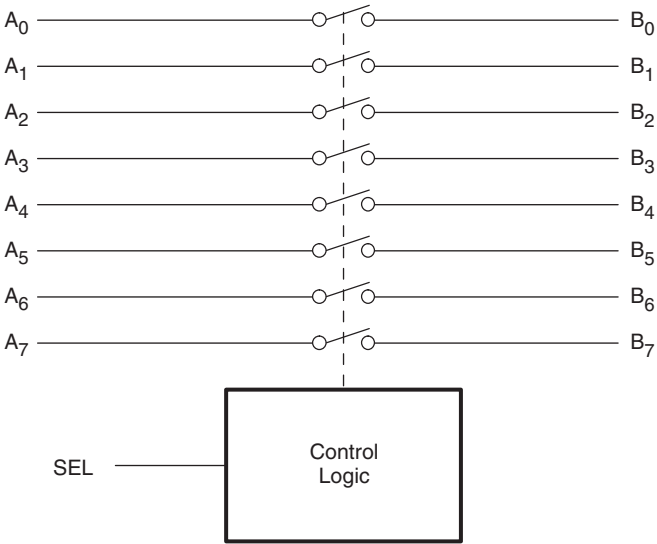
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FUNCTION TABLE

INPUT SEL	INPUT	OUTPUT	FUNCTION
H	A_n	B_n	$A_n = B_n$
L	-	-	A_n and B_n are Hi-Z

LOGIC DIAGRAM



TERMINAL FUNCTIONS

BALL		DESCRIPTION
NAME	NO.	
$A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7$	$A_5, B_4, A_4, B_3, A_3, B_2, A_2, A_1$	Data I/Os
$B_0, B_1, B_2, B_3, B_4, B_5, B_6, B_7$	$D_5, C_4, C_3, D_3, C_2, D_2, D_1, C_1$	Data I/Os
GND	B1	Ground
SEL	D4	Select inputs
V_{CC}	B5	Supply voltage

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	4.6	V
V _{IN}	Control input voltage range ^{(2) (3)}	–0.5	7	V
V _{I/O}	Switch I/O voltage range ^{(2) (3) (4)}	–0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0 or V _{IN} > V _{CC}		–50 mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0 or V _{I/O} > V _{CC}		–50 mA
I _{I/O}	ON-state switch current ⁽⁵⁾		±128	mA
	Continuous current through V _{DD} or GND		±100	mA
θ _{JA}	Package thermal impedance ⁽⁶⁾		31.8	°C/W
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	3	3.6	V
V _{IH}	High-level control input voltage	2	5.5	V
V _{IL}	Low-level control input voltage	0	0.8	V
V _I	Input voltage	0	5.5	V
V _{I/O}	Input/output voltage	0	V _{CC}	V
T _A	Operating free-air temperature	–40	85	°C

- (1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

for 1000 Base-T Ethernet switching over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}	SEL, V _{CC} = 3.6 V, I _{IN} = –18 mA	–0.7	–1.2		V
I _{IH}	SEL, V _{CC} = 3.6 V, V _{IN} = V _{CC}		±1		μA
I _{IL}	SEL, V _{CC} = 3.6 V, V _{IN} = GND		±1		μA
I _{CC}	V _{CC} = 3.6 V, I _{I/O} = 0, Switch ON or OFF		250	500	μA
C _{IN}	SEL, f = 1 M Hz, V _{IN} = 0		2	2.5	pF
C _{OFF}	B port, V _I = 0, f = 1 MHz, Outputs open, Switch OFF		2.5	4	pF
C _{ON}	V _I = 0, f = 1 MHz, Outputs open, Switch ON		8	TBD	pF
r _{ON}	V _{CC} = 3 V, 1.5 V ≤ V _I ≤ V _{CC} , I _O = –40 mA		4	6	Ω
r _{ON(flat)} ⁽³⁾	V _{CC} = 3 V, V _I = 1.5 V and V _{CC} , I _O = –40 mA		0.5		Ω
Δr _{ON} ⁽⁴⁾	V _{CC} = 3 V, 1.5 V ≤ V _I ≤ V _{CC} , I _O = –40 mA		0.4	1	Ω

- (1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
- (2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
- (3) r_{ON(flat)} is the difference of r_{ON} in a given channel at specified voltages.
- (4) Δr_{ON} is the difference of r_{ON} from center (A₄, A₅) ports to any other port.

ELECTRICAL CHARACTERISTICS

for 10/100 Base-T Ethernet switching over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}	SEL	$V_{CC} = 3.6 \text{ V}$, $I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
I_{IH}	SEL	$V_{CC} = 3.6 \text{ V}$, $V_{IN} = V_{CC}$			± 1	μA
I_{IL}	SEL	$V_{CC} = 3.6 \text{ V}$, $V_{IN} = \text{GND}$			± 1	μA
I_{CC}		$V_{CC} = 3.6 \text{ V}$, $I_{I/O} = 0$, Switch ON or OFF		250	500	μA
C_{IN}	SEL	$f = 1 \text{ MHz}$, $V_{IN} = 0$		2	2.5	pF
C_{OFF}	B port	$V_I = 0$, $f = 1 \text{ MHz}$, Outputs open, Switch OFF		2.5	4	pF
C_{ON}		$V_I = 0$, $f = 1 \text{ MHz}$, Outputs open, Switch ON		8		pF
r_{ON}		$V_{CC} = 3 \text{ V}$, $1.25 \text{ V} \leq V_I \leq V_{CC}$, $I_O = -10 \text{ mA}$ to -30 mA		4	6	Ω
$r_{ON(\text{flat})}$ ⁽³⁾		$V_{CC} = 3 \text{ V}$, $V_I = 1.25 \text{ V}$ and V_{CC} , $I_O = -10 \text{ mA}$ to -30 mA		0.5		Ω
Δr_{ON} ⁽⁴⁾		$V_{CC} = 3 \text{ V}$, $1.25 \text{ V} \leq V_I \leq V_{CC}$, $I_O = -10 \text{ mA}$ to -30 mA		0.4	1	Ω

- (1) V_I , V_O , I_I , and I_O refer to I/O pins. V_{IN} refers to the control inputs.
 (2) All typical values are at $V_{CC} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.
 (3) $r_{ON(\text{flat})}$ is the difference of r_{ON} in a given channel at specified voltages.
 (4) Δr_{ON} is the difference of r_{ON} from center (A_4 , A_5) ports to any other port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $R_L = 200 \Omega$, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see [Figure 5](#) and [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{pd} ⁽²⁾	A or B	B or A		40		ps
t_{PZH} , t_{PZL}	SEL	A or B	0.5		15	ns
t_{PHZ} , t_{PLZ}	SEL	A or B	0.9		9	ns
$t_{sk(o)}$ ⁽³⁾	A or B	B or A		50	100	ps
$t_{sk(p)}$ ⁽⁴⁾				50	150	ps

- (1) All typical values are at $V_{CC} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.
 (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
 (3) Output skew between center port (A_4 to A_5) to any other port
 (4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP ⁽¹⁾	UNIT
X_{TALK}	$R_L = 100 \Omega$,	$f = 250 \text{ MHz}$,	See Figure 8	-37	dB
O_{IRR}	$R_L = 100 \Omega$,	$f = 250 \text{ MHz}$,	See Figure 9	-37	dB
BW	$R_L = 50 \Omega$,	See Figure 7		1100	MHz

- (1) All typical values are at $V_{CC} = 3.3 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

OPERATING CHARACTERISTICS

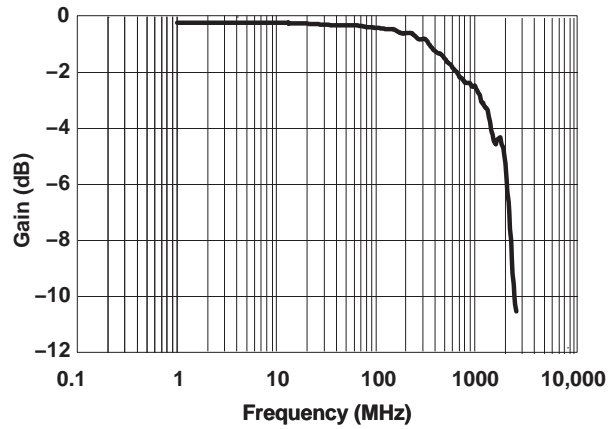


Figure 1. Gain vs Frequency

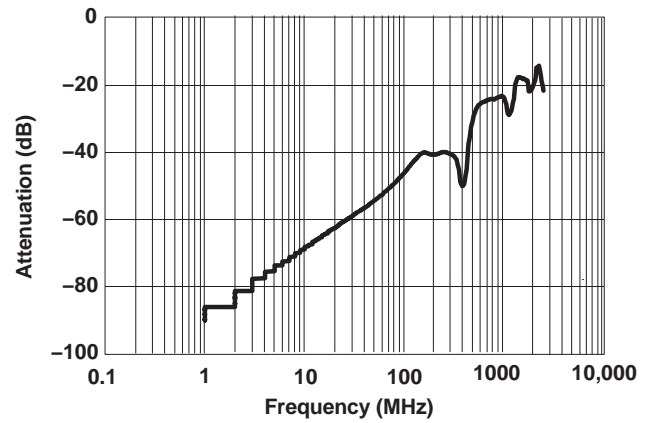


Figure 2. OFF Isolation vs Frequency

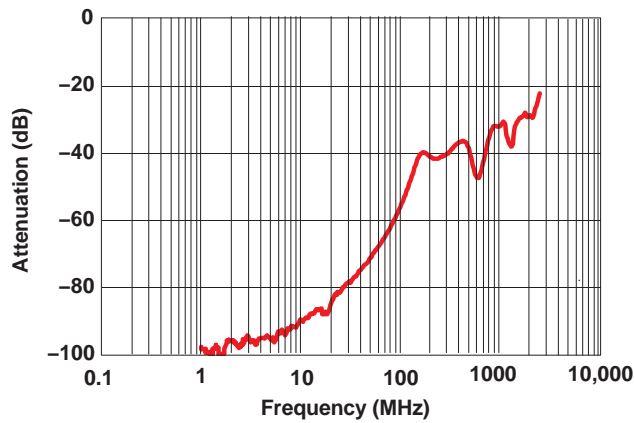


Figure 3. Crosstalk vs Frequency

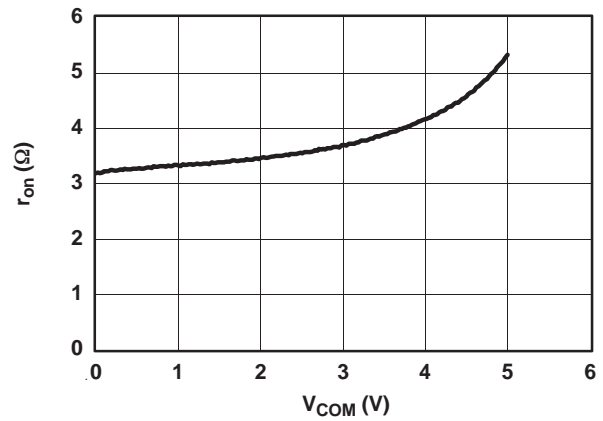
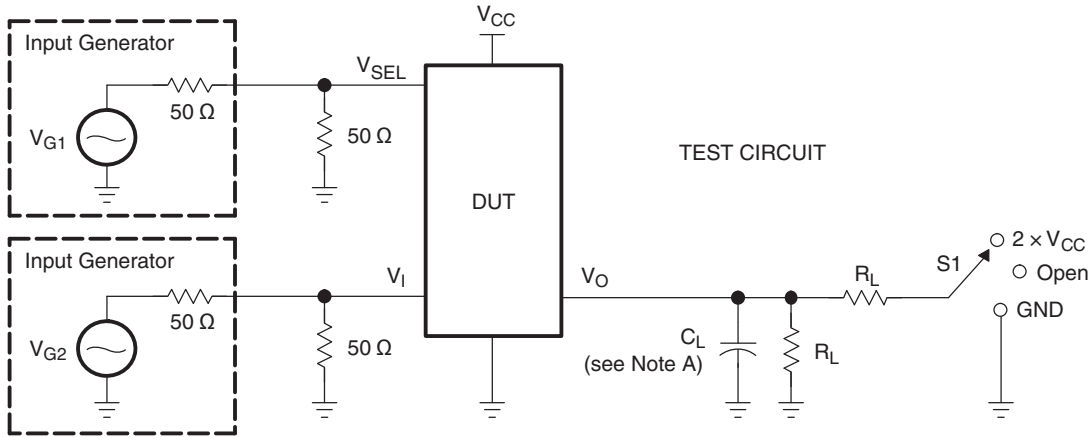
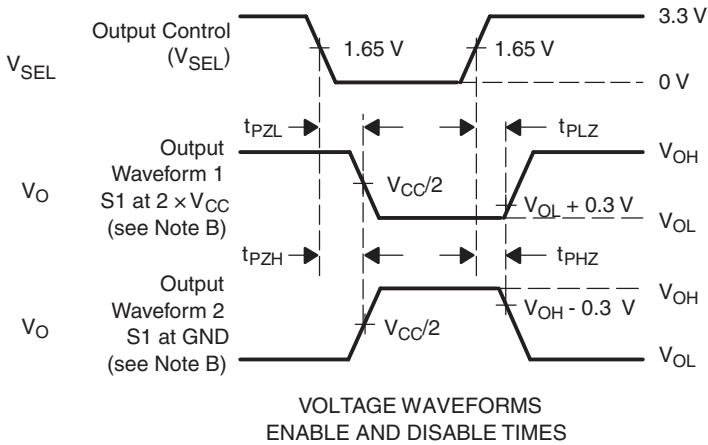


Figure 4. r_{ON} (Ω) vs V_{com} (V)

PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



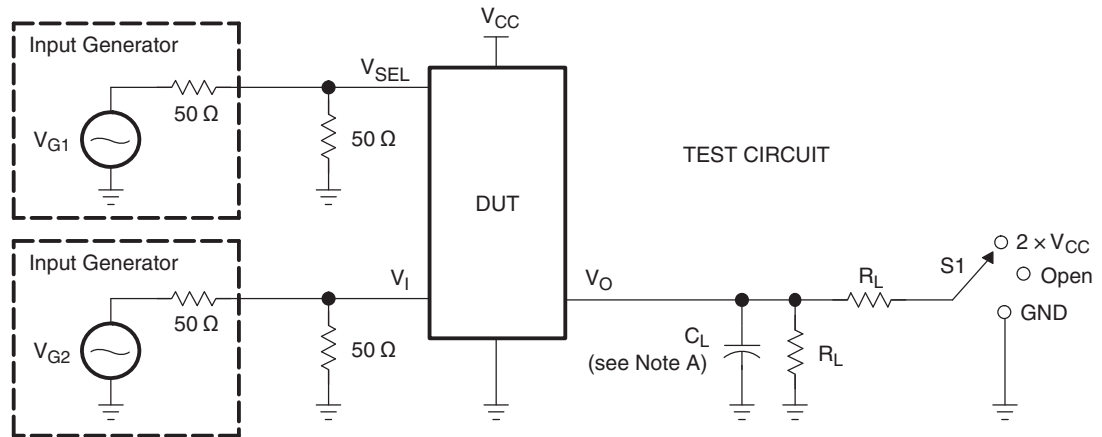
TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{PLZ} /t _{PZL}	3.3 V ± 0.3 V	2 × V _{CC}	200 Ω	GND	10 pF	0.3 V
t _{PHZ} /t _{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V _{CC}	10 pF	0.3 V



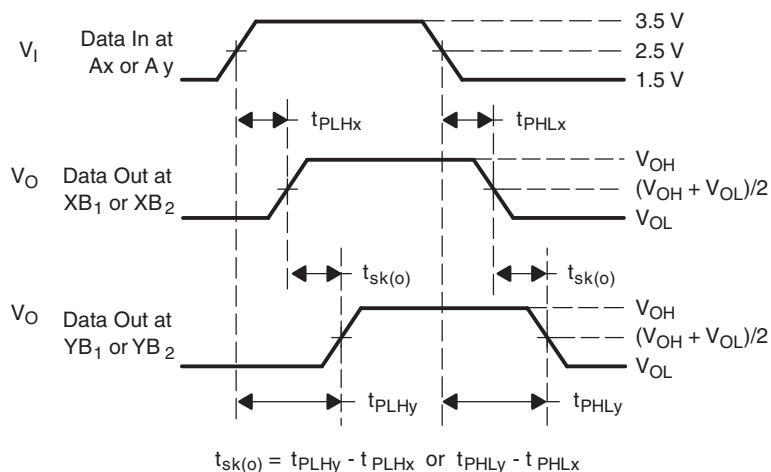
- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Test Circuit and Voltage Waveforms

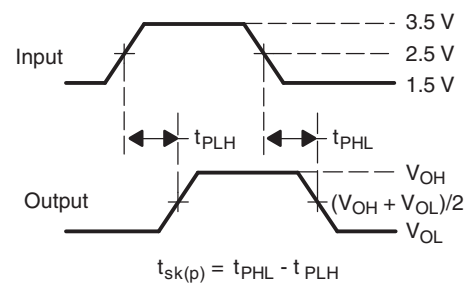
PARAMETER MEASUREMENT INFORMATION (Skew)



TEST	V _{CC}	S1	R _L	V _{in}	C _L
t _{sk(o)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	10 pF
t _{sk(p)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	10 pF



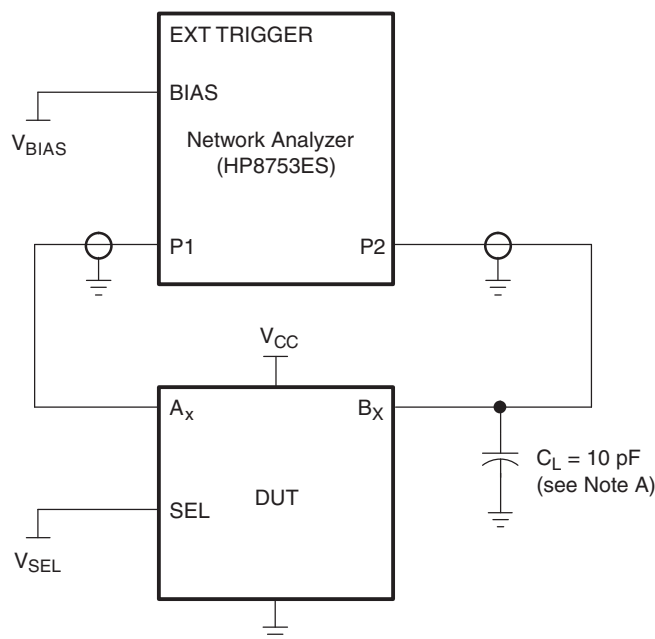
VOLTAGE WAVEFORMS
OUTPUT SKEW [t_{sk(o)}]



VOLTAGE WAVEFORMS
PULSE SKEW [t_{sk(p)}]

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- The outputs are measured one at a time, with one transition per measurement.

Figure 6. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

A. C_L includes probe and jig capacitance.

Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_{SEL} = 0$ and A_0 is the input, the output is measured at B0. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35\text{ V}$
 ST = 2 s
 P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)

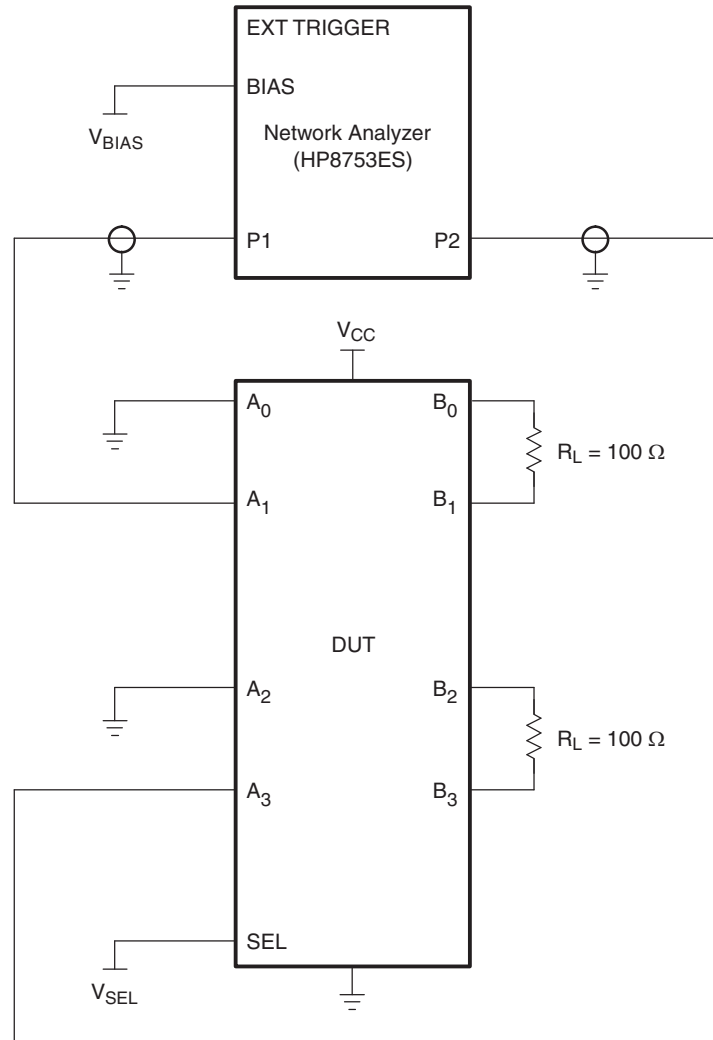


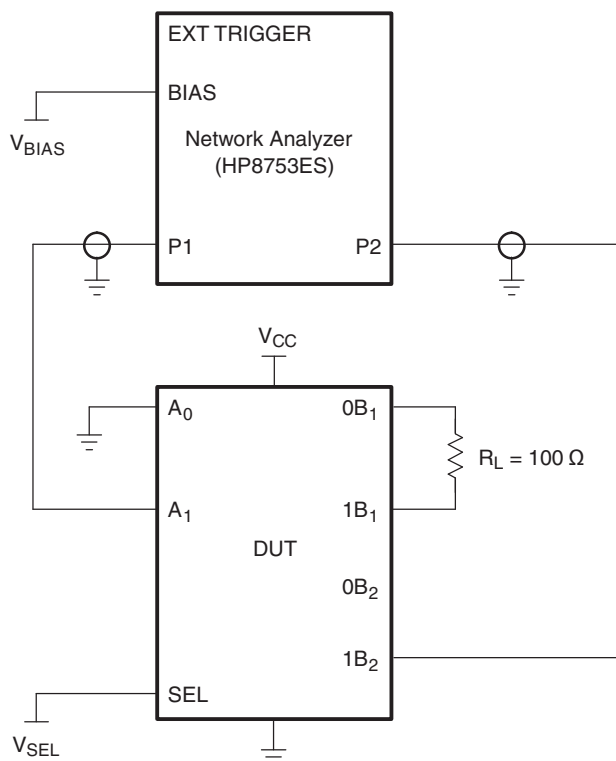
Figure 8. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{SELn} = 0$ and A_0 is the input, the output is measured at B_0 . All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50- Ω pulldown resistors.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
 ST = 2 s
 P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

Figure 9. Test Circuit for Off Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_{SELn} = V_{CC}$ and A_0 is the input, the output is measured at B0. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50- Ω pulldown resistors.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
 ST = 2 s
 P1 = 0 dBm

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TS2DDR2811ZXYR	ACTIVE	BGA MI CROSTA R JUNI OR	ZXY	20	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

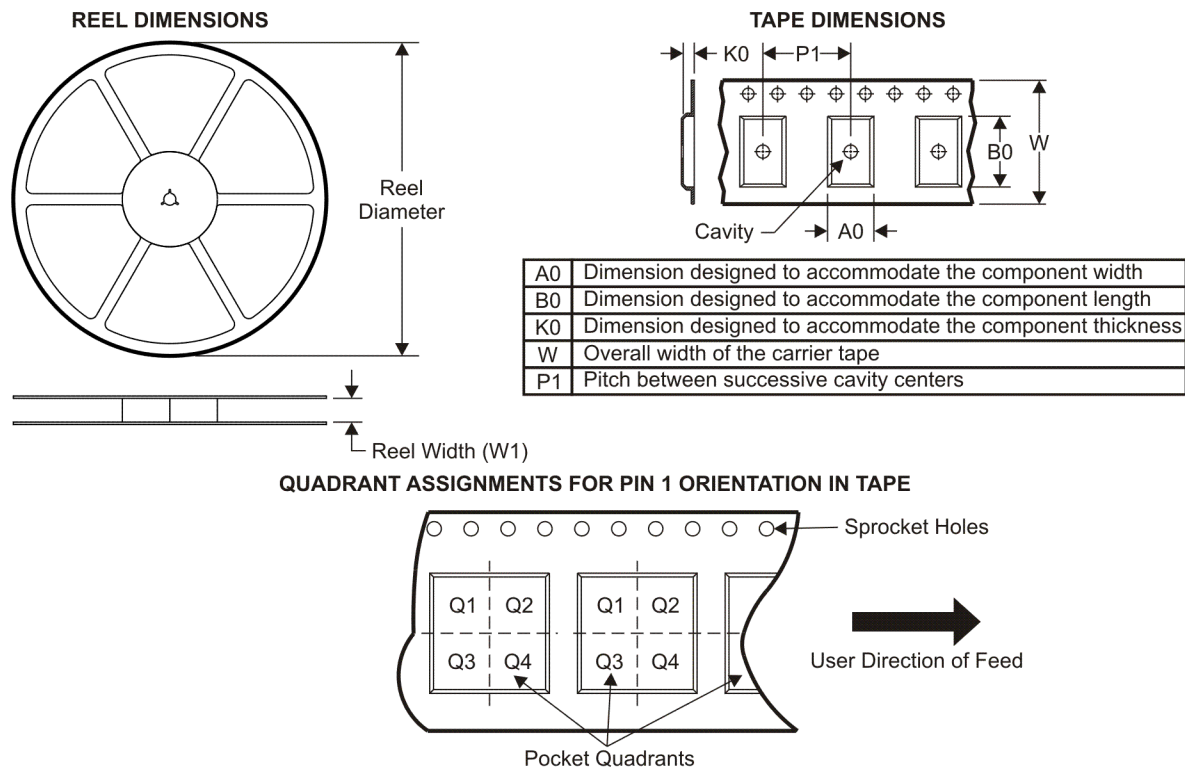
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS2DDR2811ZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	330.0	12.4	2.8	3.3	1.0	4.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

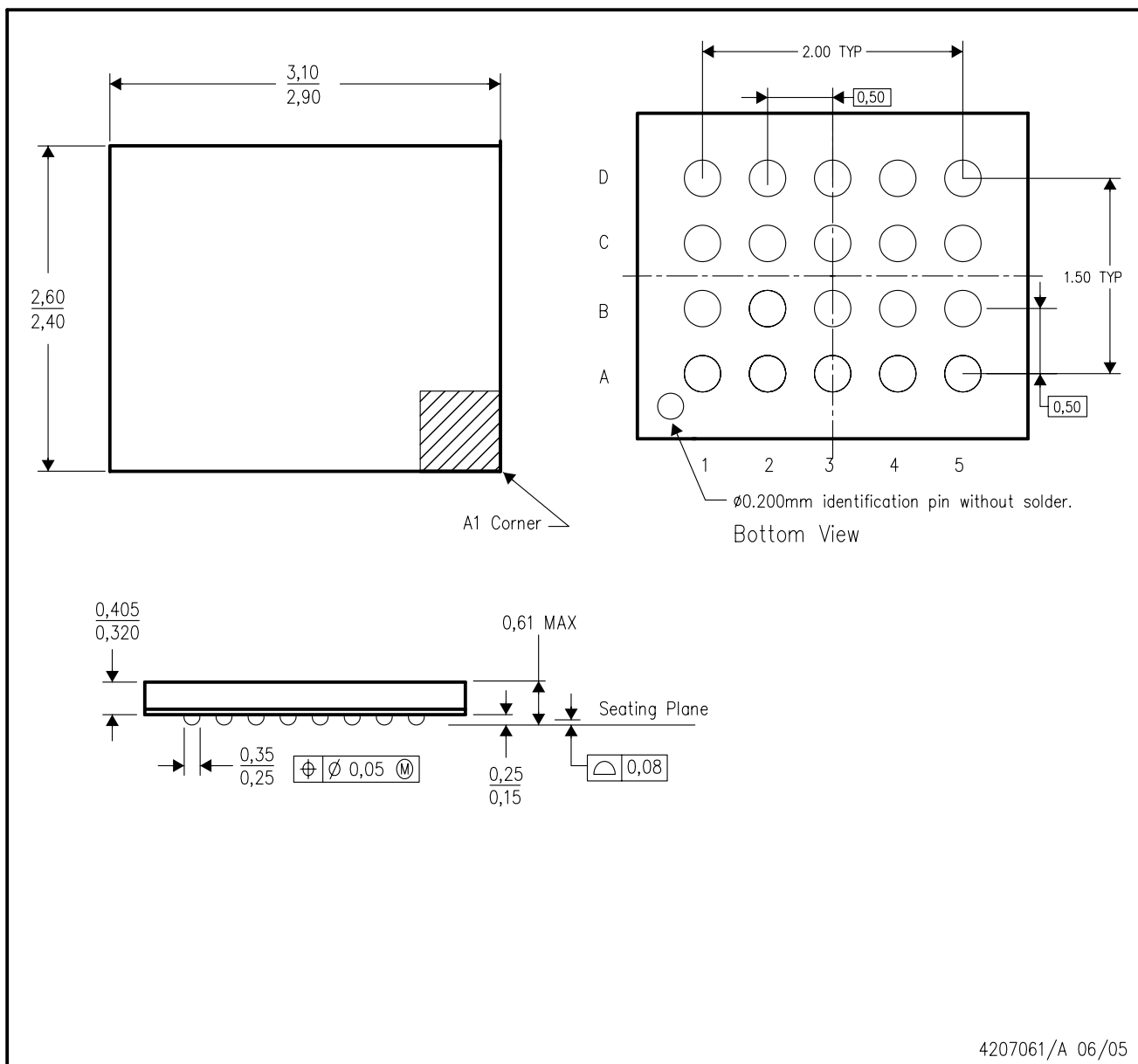


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS2DDR2811ZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	340.5	338.1	20.6

ZXY (S-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This package is a lead-free solder ball design.

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