

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
	<a href="#">查询"5962-9687001QXA"供应商</a>		

REV																				
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SHEET	15	16	17	18	19															
REV STATUS OF SHEETS				REV SHEET																
				1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Joseph A. Kerby	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216		
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY Charles F. Saffle, Jr.			MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, 18-BIT UNIVERSAL BUS TRANSCEIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON
	APPROVED BY Monica L. Poelking			
	DRAWING APPROVAL DATE 97-04-16	SIZE <b>A</b>	CAGE CODE <b>67268</b>	
	REVISION LEVEL	SHEET 1 OF 19		

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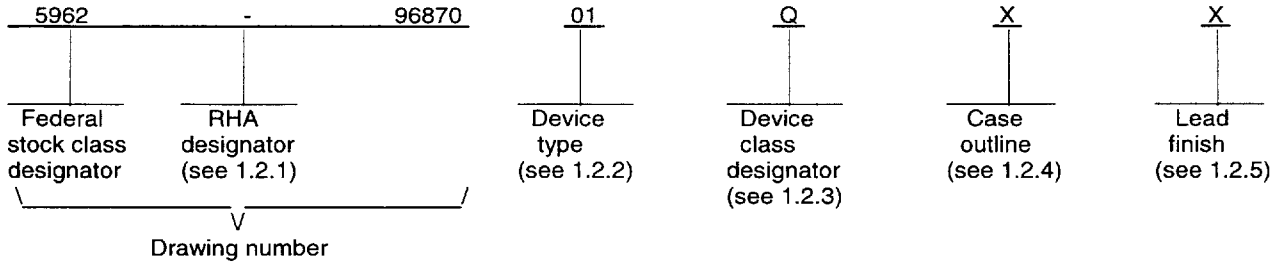
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1. SCOPE

查询"5962-9687001QXA"供应商

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ABT16500	18-bit universal bus transceiver with three-state outputs, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	GDFP1-F56	56	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		<b>REVISION LEVEL</b>	<b>SHEET 2</b>

1.3 Absolute maximum ratings. 1/ 2/ 3/

查询"5962-9687001QXA"供应商

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V dc to +7.0 V dc
DC input voltage range ( $V_{IN}$ ) (except I/O port) .....	-0.5 V dc to +7.0 V dc 4/
DC output voltage range ( $V_{OUT}$ ):	
In the disabled or power off state .....	-0.5 V dc to +5.5 V dc 4/
In the high state .....	-0.5 V dc to $V_{CC}$ 4/
DC output current applied to output in the low state ( $I_{OL}$ ) (per output) .....	+96 mA
DC input clamp current ( $I_{IK}$ ) ( $V_{IN} < 0.0$ V) .....	-18 mA
DC output clamp current ( $I_{OK}$ ) ( $V_{OUT} < 0.0$ V) .....	-50 mA
Maximum power dissipation at ( $P_D$ ) .....	500 mW
Storage temperature range ( $T_{STG}$ ) .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case ( $\Theta_{JC}$ ) .....	See MIL-STD-1835
Junction temperature ( $T_J$ ) .....	+175°C

1.4 Recommended operating conditions. 2/ 3/ 5/

Supply voltage range ( $V_{CC}$ ) .....	+4.5 V dc to +5.5 V dc
Input voltage range ( $V_{IN}$ ) .....	0.0 V dc to $V_{CC}$
Output voltage range ( $V_{OUT}$ ) .....	0.0 V dc to $V_{CC}$
Minimum high level input voltage ( $V_{IH}$ ) .....	2.0 V
Maximum low level input voltage ( $V_{IL}$ ) .....	0.8 V
Maximum high level output current ( $I_{OH}$ ) .....	-24 mA
Maximum low level output current ( $I_{OL}$ ) .....	48 mA
Maximum input rise and fall rate ( $\Delta t/\Delta V$ ) (outputs enabled) .....	10 ns/V
Operating case temperature range ( $T_C$ ) .....	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) .....	XX percent 6/
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- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ The limits for the parameters specified herein shall apply over the full specified  $V_{CC}$  range and case temperature range of -55°C to +125°C.
- 4/ The input and output negative voltage ratings may be exceeded provided that the input and output clamp current ratings are observed.
- 5/ Unused or floating inputs (inputs or I/O) must be held high or low.
- 6/ Values will be added when they become available.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>	<b>5962-96870</b>
	<b>REVISION LEVEL</b>	<b>SHEET 3</b>

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
 MIL-STD-973 - Configuration Management.  
 MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216	SIZE <b>A</b>		<b>5962-96870</b>
		REVISION LEVEL	SHEET <b>4</b>

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method <sup>1/</sup>	Symbol	Test conditions <sup>2/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified		Device type	V <sub>CC</sub>	Group A subgroups	Limits <sup>3/</sup>		Unit
							Min	Max	
Negative input clamp voltage 3022	V <sub>IK</sub>	For input under test, I <sub>IN</sub> = -18 mA		All	4.5 V	1, 2, 3		-1.2	V
High level output voltage 3006	V <sub>OH1</sub>	For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OH</sub> = -3.0 mA		All	4.5 V	1, 2, 3	2.5		V
	V <sub>OH2</sub>	For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OH</sub> = -3.0 mA		All	5.0 V	1, 2, 3	3.0		
	V <sub>OH3</sub>	For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OH</sub> = -24 mA		All	4.5 V	1, 2, 3	2.0		
Low level output voltage 3007	V <sub>OL</sub>	For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OL</sub> = 48 mA		All	4.5 V	1, 2, 3		0.55	V
Input current high 3010	I <sub>IH</sub> <sup>4/</sup>	For input under test, V <sub>IN</sub> = 5.5 V	Control pins	All	5.5 V	1, 2, 3		5.0	μA
			A or B ports	All		1, 2, 3		100	μA
Input current low 3009	I <sub>IL</sub> <sup>4/</sup>	For input under test, V <sub>IN</sub> = 0.0 V	Control pins	All	5.5 V	1, 2, 3		-5.0	μA
			A or B ports	All		1, 2, 3		-100	μA
Three-state output leakage current high 3021	I <sub>OZH</sub> <sup>5/</sup>	For control inputs affecting outputs under test, V <sub>IN</sub> = 2.0 V or 0.8 V V <sub>OUT</sub> = 2.7 V		All	5.5 V	1, 2, 3		50.0	μA
Three-state output leakage current low 3021	I <sub>OZL</sub> <sup>5/</sup>	For control inputs affecting outputs under test, V <sub>IN</sub> = 2.0 V or 0.8 V V <sub>OUT</sub> = 0.5 V		All	5.5 V	1, 2, 3		-50.0	μA
Quiescent supply current 3005	I <sub>CCH</sub>	For all inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0.0 A	Outputs high	All	5.5 V	1, 2, 3		1.0	mA
	I <sub>CCL</sub>		Outputs low					68.0	
	I <sub>CCZ</sub>		Outputs disabled					1.0	
Output high-state leakage current	I <sub>CEX</sub>	For output under test, V <sub>OUT</sub> = 5.5 V Outputs at high logic state		All	5.5 V	1, 2, 3		50.0	μA

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		REVISION LEVEL	SHEET 5

TABLE I. Electrical performance characteristics - Continued.

查询"5962-9687001QXA"供应商

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified		Device type	V <sub>CC</sub>	Group A subgroups	Limits 3/		Unit
							Min	Max	
Output short circuit current	I <sub>OS</sub>	V <sub>OUT</sub> = 2.5 V		All	5.5 V	1, 2, 3	-50	-180	mA
Quiescent supply current delta, TTL input levels 3005	ΔI <sub>CC</sub> Z/	For input under test, V <sub>IN</sub> = 3.4 V For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND	Data inputs, outputs enabled	All	5.5 V			2.5	mA
			Data inputs, outputs disabled					1.0	
			Control inputs					2.5	
Off-state leakage current	I <sub>OFF</sub>	For input or output under test V <sub>IN</sub> or V <sub>OUT</sub> = 5.5 V		All	0.0 V	1		±100	μA
Low level ground bounce noise	V <sub>OLP</sub>	V <sub>IH</sub> = 3.0 V, V <sub>IL</sub> = 0.0 V T <sub>A</sub> = +25°C See figure 4 See 4.4.1d		All	5.0 V	4		1100	mV
Low level ground bounce noise	V <sub>OLV</sub>			All	5.0 V	4		-1700	
High level V <sub>CC</sub> bounce noise	V <sub>OHP</sub>			All	5.0 V	4		1500	
High level V <sub>CC</sub> bounce noise	V <sub>OHV</sub>			All	5.0 V	4		-900	
Input capacitance 3012	C <sub>IN</sub>	T <sub>C</sub> = +25°C See 4.4.1c		All	0.0 V	4		10.5	pF
I/O capacitance 3012	C <sub>I/O</sub>	T <sub>C</sub> = +25°C See 4.4.1c		All	5.0 V	4		15.0	pF
Functional test 3014	9/	V <sub>IN</sub> = 0.8 V or 2.0 V Verify output V <sub>O</sub> See 4.4.1b		All	4.5 V	7, 8	L	H	
					5.5 V				
Clock frequency	f <sub>clk</sub> 10/	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω		All	4.5 V and 5.5 V	9, 10, 11	0	150	MHz
Pulse duration, LEAB or LEBA high	t <sub>w1</sub> 10/	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5		All	4.5 V and 5.5 V	9, 10, 11	3.3		ns
Pulse duration, <u>CLKAB</u> or <u>CLKBA</u> high or low	t <sub>w2</sub> 10/	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5		All	4.5 V and 5.5 V	9, 10, 11	3.3		ns

See footnotes at end of table.

STANDARD  
MICROCIRCUIT DRAWING  
DEFENSE SUPPLY CENTER, COLUMBUS  
COLUMBUS, OHIO 43216

SIZE  
A

5962-96870

REVISION LEVEL

SHEET  
6

TABLE I. Electrical performance characteristics - Continued.

查询"5962-9687001QXA"供应商

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Device type	V <sub>CC</sub>	Group A subgroups	Limits 3/		Unit
						Min	Max	
Setup time, high or low, An before <u>CLKAB</u> !	t <sub>s1</sub> <u>10/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5	All	4.5 V and 5.5 V	9, 10, 11	4.5		ns
Setup time, high or low, Bn before <u>CLKBA</u> !	t <sub>s2</sub> <u>10/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5	All	4.5 V and 5.5 V	9, 10, 11	4.0		ns
Setup time, high or low, An before LEAB! or Bn before LEBA!	t <sub>s3</sub> <u>10/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5 <u>CLKAB</u> or <u>CLKBA</u> high	All	4.5 V and 5.5 V	9, 10, 11	1.5		ns
		C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5 <u>CLKAB</u> or <u>CLKBA</u> low		4.5 V and 5.5 V		4.5		
Hold time, high or low, An after <u>CLKAB</u> ! or Bn after <u>CLKBA</u> !	t <sub>h1</sub> <u>10/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5	All	4.5 V and 5.5 V	9, 10, 11	0.0		ns
Hold time, high or low, An after LEAB! or Bn after LEBA!	t <sub>h2</sub> <u>10/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5 <u>CLKAB</u> or <u>CLKBA</u> high	All	4.5 V and 5.5 V	9, 10, 11	1.5		ns
	t <sub>h3</sub> <u>10/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5 <u>CLKAB</u> or <u>CLKBA</u> low	All	4.5 V and 5.5 V	9, 10, 11	1.5		ns
Propagation delay time, Bn to An or An to Bn 3003	t <sub>PLH1</sub> <u>11/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5	All	4.5 V and 5.5 V	9	1.0	5.5	ns
	t <sub>PHL1</sub> <u>11/</u>				10, 11	1.0	6.5	
				All	4.5 V and 5.5 V	9	1.0	
					10, 11	1.0	7.0	

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		REVISION LEVEL	SHEET 7

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <sup>1/</sup>	Symbol	Test conditions <sup>2/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Device type	V <sub>CC</sub>	Group A subgroups	Limits <sup>3/</sup>		Unit
						Min	Max	
Propagation delay time, LEBA to An or LEAB to Bn 3003	t <sub>PLH2</sub> <u>11/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5	All	4.5 V and 5.5 V	9	1.0	6.0	ns
					10, 11	1.0	7.0	
	t <sub>PHL2</sub> <u>11/</u>		All	4.5 V and 5.5 V	9	1.0	6.8	
					10, 11	1.0	7.8	
Propagation delay time, $\overline{\text{CLKBA}}$ to An or $\overline{\text{CLKAB}}$ to Bn 3003	t <sub>PLH3</sub> <u>11/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5	All	4.5 V and 5.5 V	9	1.0	6.5	ns
					10, 11	1.0	7.5	
	t <sub>PHL3</sub> <u>11/</u>		All	4.5 V and 5.5 V	9	1.0	7.0	
					10, 11	1.0	8.0	
Propagation delay time, output enable, OEAB to Bn or $\overline{\text{OEBA}}$ to An 3003	t <sub>PZH</sub> <u>11/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5	All	4.5 V and 5.5 V	9	1.0	5.6	ns
					10, 11	1.0	6.3	
	t <sub>PZL</sub> <u>11/</u>		All	4.5 V and 5.5 V	9	1.0	6.0	
					10, 11	1.0	6.5	
Propagation delay time, output disable, OEAB to Bn or $\overline{\text{OEBA}}$ to An 3003	t <sub>PHZ</sub> <u>11/</u>	C <sub>L</sub> = 50 pF minimum R <sub>L</sub> = 500Ω See figure 5	All	4.5 V and 5.5 V	9	1.0	6.5	ns
					10, 11	1.0	7.2	
	t <sub>PLZ</sub> <u>11/</u>		All	4.5 V and 5.5 V	9	1.0	6.0	
					10, 11	1.0	6.8	

- <sup>1/</sup> For tests not listed in the referenced MIL-STD-883 (e.g. ΔI<sub>CC</sub>), utilize the general test procedure of 883 under the conditions listed herein.
- <sup>2/</sup> Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I<sub>CC</sub> and ΔI<sub>CC</sub> tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V<sub>IN</sub> ≤ 0.8 V or ≥ 2.0 V.
- <sup>3/</sup> For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.
- <sup>4/</sup> For I/O ports, the limit includes I<sub>OZH</sub> or I<sub>OZL</sub> leakage current from the output circuitry.
- <sup>5/</sup> For I/O ports, the limit includes I<sub>IH</sub> or I<sub>IL</sub> leakage current from the input circuitry. This test shall be guaranteed, if not tested, to the limits specified in table I herein, when performed with control inputs that affect the state of the output under test at V<sub>IN</sub> = 0.8 V or 2.0 V.
- <sup>6/</sup> Not more than one output should be tested at one time, and the duration of the test condition should not exceed one second.

STANDARD  
MICROCIRCUIT DRAWING  
DEFENSE SUPPLY CENTER, COLUMBUS  
COLUMBUS, OHIO 43216

SIZE  
**A**

**5962-96870**

REVISION LEVEL

SHEET

**8**



TABLE I. Electrical performance characteristics - Continued.

- 7/ 查询"5962-9687001QXA"供应商 This is the increase supply current for each input that is at one of the specified TTL voltage levels rather than 0.0 V or  $V_{CC}$ . This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at  $V_{IN} = V_{CC} - 2.1$  V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times  $\Delta I_{CC}$  maximum and the preferred method and limits are guaranteed.
- 8/ This test is for qualification only. Ground and  $V_{CC}$  bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500 $\Omega$  of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from  $V_{CC}$  to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and  $V_{CC}$  bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50 $\Omega$  input impedance.
- The device inputs shall be conditioned such that all outputs are at a high nominal  $V_{OH}$  level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at  $V_{OH}$  as all other outputs possible are switched from  $V_{OH}$  to  $V_{OL}$ .  $V_{OHV}$  and  $V_{OHP}$  are then measured from the nominal  $V_{OH}$  level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from  $V_{OL}$  to  $V_{OH}$ .
- The device inputs shall be conditioned such that all outputs are at a low nominal  $V_{OL}$  level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at  $V_{OL}$  as all other outputs possible are switched from  $V_{OL}$  to  $V_{OH}$ .  $V_{OLP}$  and  $V_{OLV}$  are then measured from the nominal  $V_{OL}$  level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from  $V_{OH}$  to  $V_{OL}$ .
- 9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. The allowable tolerances per MIL-STD-883 have already been incorporated. For outputs,  $L \leq 0.8$  V,  $H \geq 2.0$  V.
- 10/ This parameter shall be guaranteed, if not tested, to the limits specified in table I herein.
- 11/ For propagation delay tests, test all functions of each input and output.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		<b>REVISION LEVEL</b>	<b>SHEET 9</b>

查询"5962-9687001QXA"供应商

Device type		01	
Case outline		X	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	OEAB	29	GND
2	LEAB		
3	A1	30	CLKBA
4	GND	31	B18
5	A2	32	GND
6	A3	33	B17
7	V <sub>CC</sub>	34	B16
		35	V <sub>CC</sub>
8	A4		
9	A5	36	B15
10	A6	37	B14
11	GND	38	B13
12	A7	39	GND
13	A8	40	B12
14	A9	41	B11
15	A10	42	B10
16	A11	43	B9
17	A12	44	B8
18	GND	45	B7
19	A13	46	GND
20	A14	47	B6
21	A15	48	B5
22	V <sub>CC</sub>	49	B4
		50	V <sub>CC</sub>
23	A16		
24	A17	51	B3
25	GND	52	B2
26	A18	53	GND
		54	B1
27	OEBA		
28	LEBA	55	CLKAB
		56	GND

Pin description	
Terminal symbol	Description
A <sub>n</sub> (n = 1 to 18)	Data inputs/outputs, A port
B <sub>n</sub> (n = 1 to 18)	Data inputs/outputs, B port
OEAB/OEBA	Output enable control inputs
LEAB/LEBA	Latch enable control inputs
CLKAB/CLKBA	Clock inputs (active low)

FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		<b>REVISION LEVEL</b>	<b>SHEET 10</b>

DESC FORM 193A  
JUL 94

9004708 0028418 4TT

Device type 01 <u>1/</u>				
Inputs				Outputs
OEAB	LEAB	$\overline{\text{CLKAB}}$	An	Bn
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B <sub>0</sub>
H	L	L	X	B <sub>0</sub> <u>2/</u>

H = High voltage level  
 L = Low voltage level  
 X = Irrelevant  
 Z = Disabled  
 ↓ = Low-to-high transition of clock.  
 B<sub>0</sub> = The output level of B before the indicated steady-state input conditions were established.

1/ A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{\text{OEBA}}$ , LEBA, and  $\overline{\text{CLKBA}}$ .

2/ Output level before the indicated steady-state input conditions were established, provided that  $\overline{\text{CLKAB}}$  was low before LEAB went low.

FIGURE 2. Truth table.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		<b>REVISION LEVEL</b>	<b>SHEET 11</b>

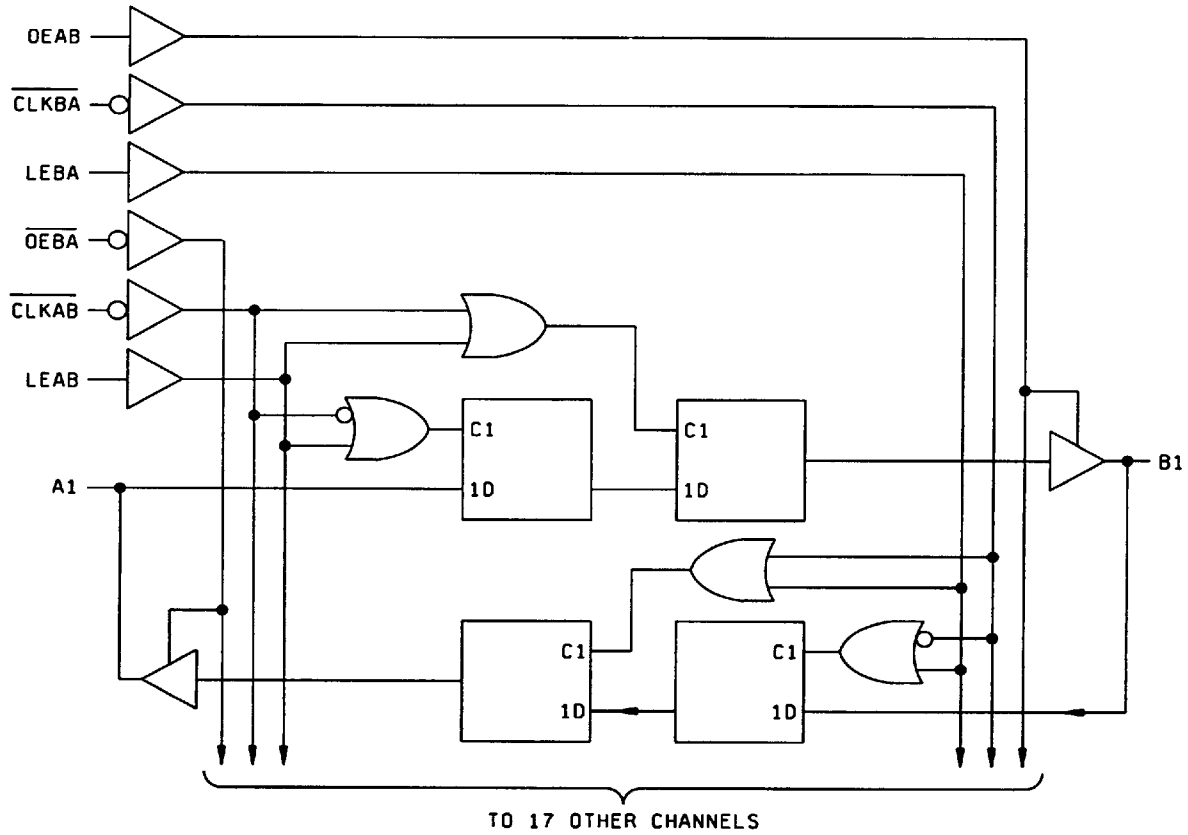
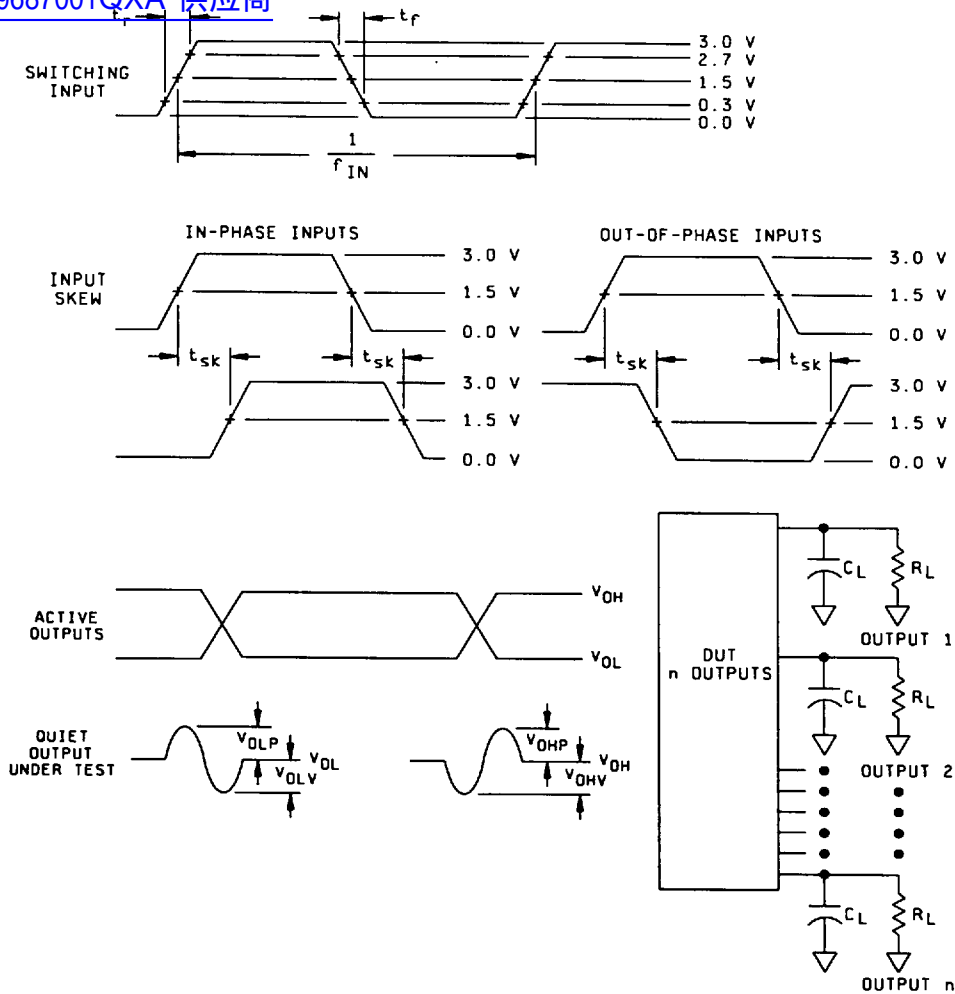


FIGURE 3. Logic diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216	SIZE <b>A</b>		5962-96870
		REVISION LEVEL	SHEET <b>12</b>



NOTES:

1.  $C_L$  includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2.  $R_L = 450\Omega \pm 1$  percent, chip resistor in series with a  $50\Omega$  termination. For monitored outputs, the  $50\Omega$  termination shall be the  $50\Omega$  characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
  - a.  $V_{IN} = 0.0$  V to 3.0 V; duty cycle = 50 percent;  $f_{IN} \geq 1$  MHz.
  - b.  $t_r, t_f = 3$  ns  $\pm 1.0$  ns. For input signal generators incapable of maintaining these values of  $t_r$  and  $t_f$ , the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the  $\pm 1.0$  ns tolerance and guaranteeing the results at 3.0 ns  $\pm 1.0$  ns; skew between any two switching inputs signals ( $t_{sk}$ ):  $\leq 250$  ps.

FIGURE 4. Ground bounce load circuit and waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216	SIZE <b>A</b>		5962-96870
		REVISION LEVEL	SHEET <b>13</b>

查询"5962-9687001QXA"供应商

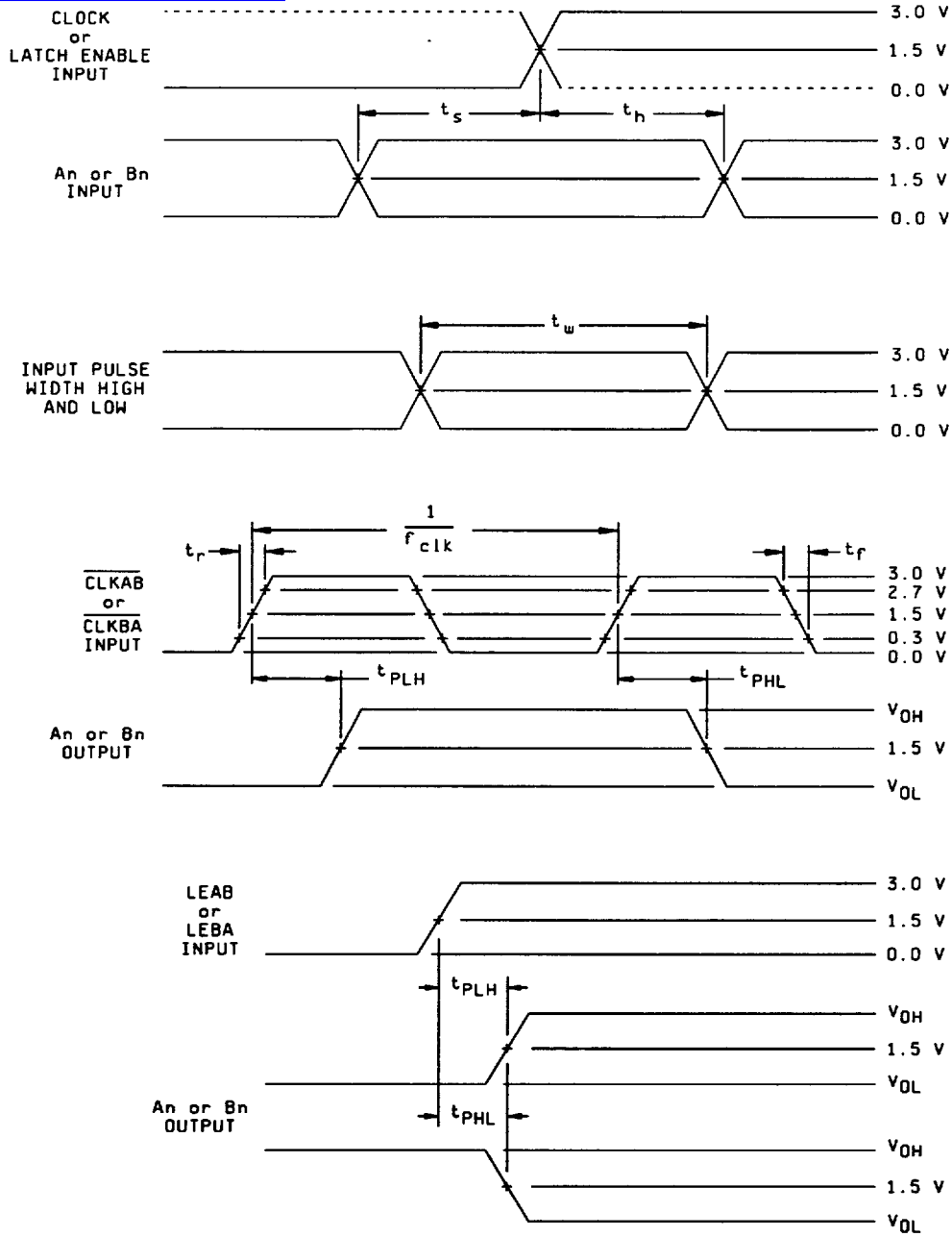
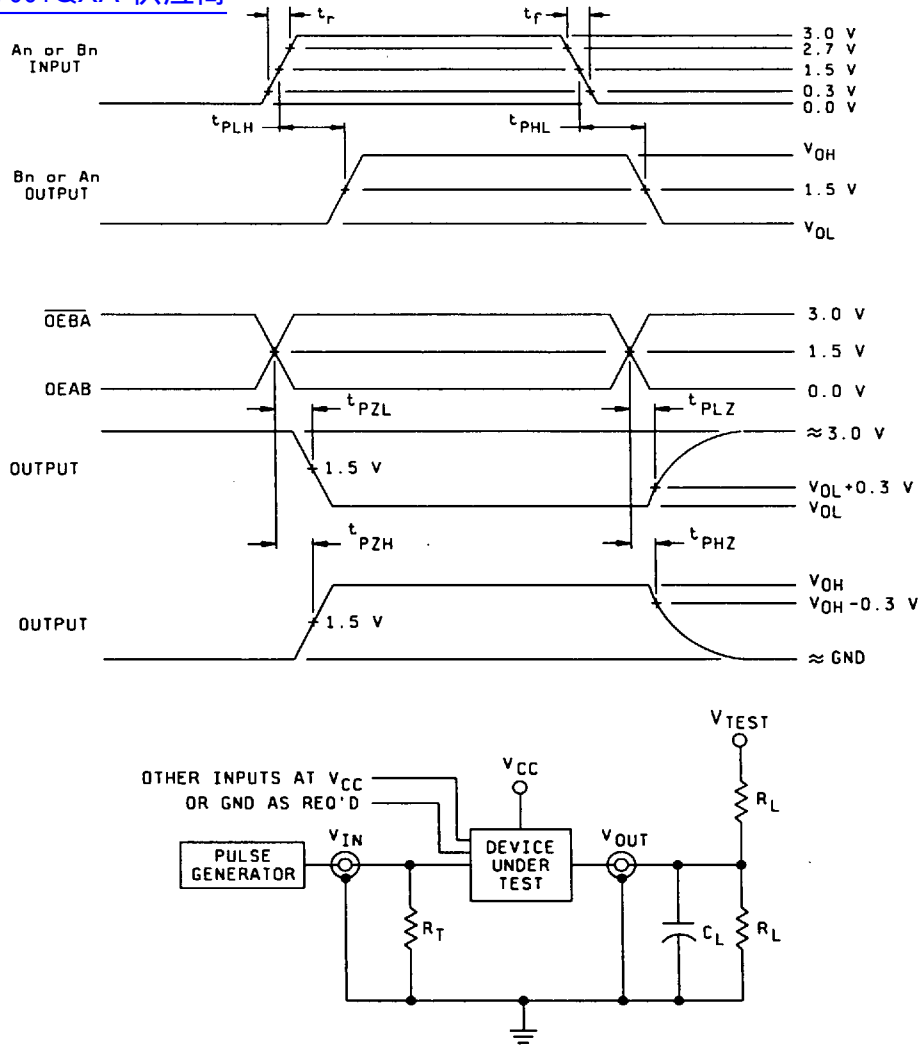


FIGURE 5. Switching waveforms and test circuit.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216	<b>SIZE A</b>		<b>5962-96870</b>
		REVISION LEVEL	SHEET <b>14</b>

DESC FORM 193A  
JUL 94

9004708 0028422 920



NOTES:

1. When measuring  $t_{PLH}$  and  $t_{PHL}$ :  $V_{TEST} = \text{open}$ .
2. When measuring  $t_{PLZ}$  and  $t_{PZL}$ :  $V_{TEST} = 7.0$  V.
3. When measuring  $t_{PHZ}$  and  $t_{PZH}$ :  $V_{TEST} = \text{GND}$ .
4. The  $t_{PZL}$  and  $t_{PLZ}$  reference waveform is for the output under test with internal conditions such that the output is at  $V_{OL}$  except when disabled by the output enable control. The  $t_{PZH}$  and  $t_{PHZ}$  reference waveform is for the output under test with internal conditions such that the output is at  $V_{OH}$  except when disabled by the output enable control.
5.  $C_L = 50$  pF minimum or equivalent (includes test jig and probe capacitance).
6.  $R_L = 500\Omega$  or equivalent.
7.  $R_T = 50\Omega$  or equivalent.
8. Input signal from pulse generator:  $V_{IN} = 0.0$  V to 3.0 V;  $PRR \leq 10$  MHz;  $t_r \leq 2.5$  ns;  $t_f \leq 2.5$  ns;  $t_r$  and  $t_f$  shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
9. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
10. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		REVISION LEVEL	SHEET <b>15</b>

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 126 (see MIL-PRF-38535, appendix A).

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

##### 4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

##### 4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

STANDARD  
MICROCIRCUIT DRAWING  
DEFENSE SUPPLY CENTER, COLUMBUS  
COLUMBUS, OHIO 43216

SIZE  
A

5962-96870

REVISION LEVEL

SHEET

16



b. Interim and final electrical test parameters shall be as specified in table II herein.

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c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		<b>REVISION LEVEL</b>	<b>SHEET 17</b>

4.4.1 Group A inspection.

a. Tests shall be as specified in table I herein.

- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- c.  $C_{IN}$  and  $C_{I/O}$  shall be measured only for initial qualification and after process or design changes which may affect capacitance.  $C_{IN}$  and  $C_{I/O}$  shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test ( $V_{BIAS}$ ) = 2.5 V or 3.0 V. For  $C_{IN}$  and  $C_{I/O}$ , test all applicable pins on five devices with zero failures.

For  $C_{IN}$  and  $C_{I/O}$ , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the  $C_{IN}$  and  $C_{I/O}$  tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DSCC-VA the device functions listed in each functional group and the test results for each device tested.

- d. Ground and  $V_{CC}$  bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture.  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DSCC-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DSCC-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DSCC-VA data from testing on both fixtures, that shall include all measured peak values for each device tested and detailed oscilloscope plots for each  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For  $V_{OHP}$ ,  $V_{OHV}$ ,  $V_{OLP}$ , and  $V_{OLV}$ , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the  $V_{OHP}$ ,  $V_{OHV}$ ,  $V_{OLP}$ , and  $V_{OLV}$  tests. The device manufacturer may then test one device function from a functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturers shall submit to DSCC-VA the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		<b>REVISION LEVEL</b>	<b>SHEET 18</b>

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ , after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center, Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43216</b>	<b>SIZE A</b>		<b>5962-96870</b>
		<b>REVISION LEVEL</b>	<b>SHEET 19</b>

DATE: 97-04-16

Approved sources of supply for SMD 5962-96870 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9687001QXA	27014	54ABT16500W-QML

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

Vendor name  
and address

27014

National Semiconductor  
2900 Semiconductor Drive  
P. O. Box 58090  
Santa Clara, CA 95052-8090  
Point-of-contact: 333 Western Avenue  
South Portland, ME 04106

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