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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:

27 June 1986

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY:

APPROVED BY:

SIZE: A

CODE IDENT. NO.: 14933

REV

MILITARY DRAWING

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TITLE: MICROCIRCUITS SYSTEM TIMING CONTROLLER, MONOLITHIC SILICON

DWG NO. 5962-85523

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5962-E849

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DESC FORM 193

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-85523	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	9513A	System timing controller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40 lead 9/16" x 2 1/16"), dual-in-line package
X	C-5 (44 terminal .650" x .650"), square chip carrier

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.5 W
Lead temperature (soldering, 5 seconds)	270°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	See MIL-M-38510, appendix C
Case X	15°C/W 1/
Junction temperature (T_J)	150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	5.0 V dc +/-5%
High-level input voltage (V_{IH})	All inputs except X2; 2.2 V dc minimum, at V_{CC} maximum X2 input 3.8 V minimum, at V_{CC} maximum
Low-level input voltage (V_{IL})	V_{SS} -0.5 V dc minimum to 0.8 maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ When a thermal resistance value for this case is included in MIL-M-38510, appendix C, that value supersedes the value indicated herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

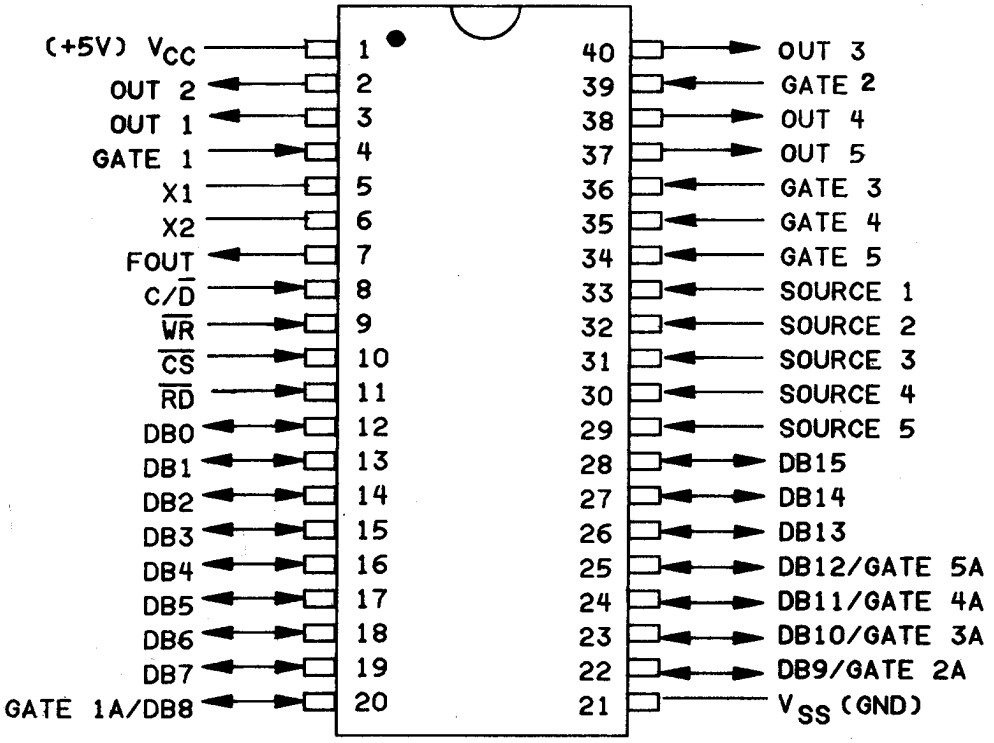
3.2.3 Function table. The function table shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

Case Q



Note: Pin 1 is marked for orientation

FIGURE 1. Terminal connections.

Case X

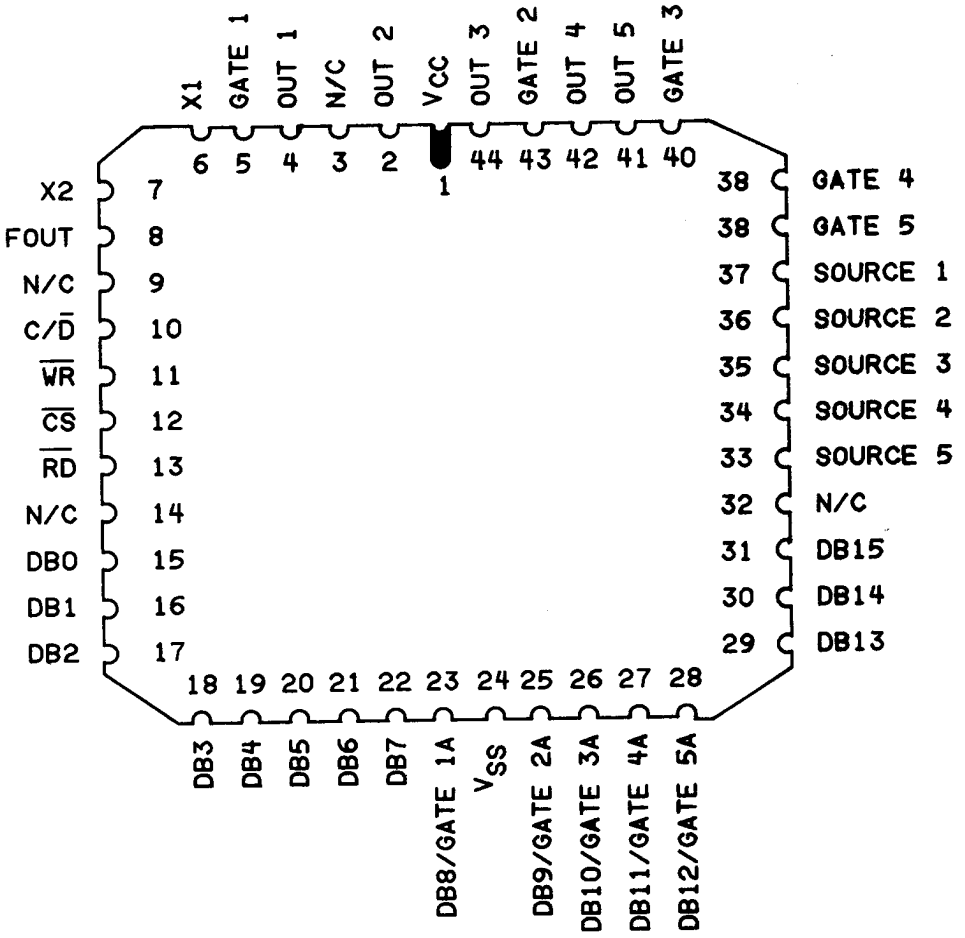


FIGURE 1. Terminal connections-Continued.

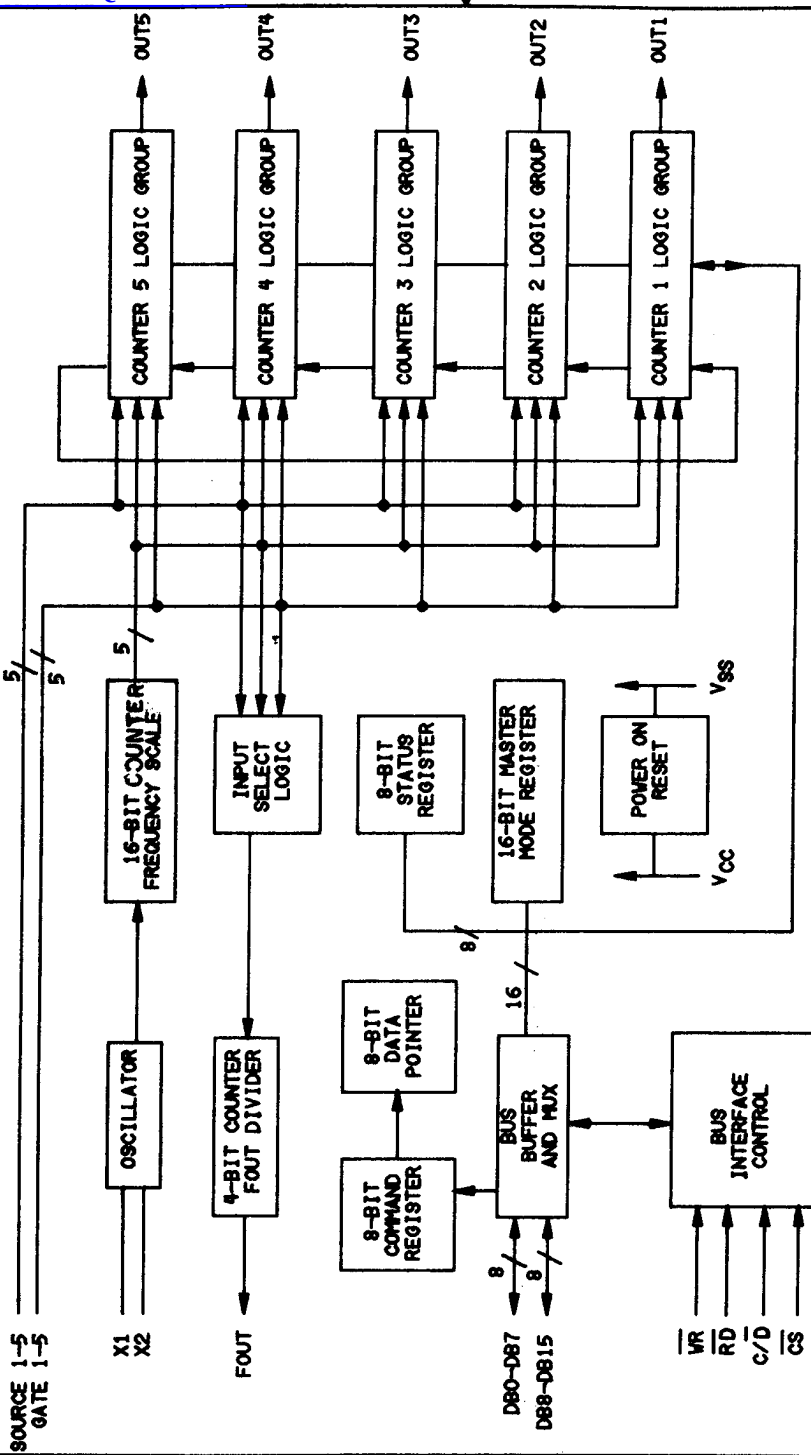


FIGURE 2. Block diagram.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-85523
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DESC FORM 193A
FEB 86

Counter Mode	A	B	C	D	E	F	G	H	I	J	K	L
Special Gate (CM7)	0	0	0	0	0	0	0	0	0	0	0	0
Reload Source (CM6)	0	0	0	0	0	0	1	1	1	1	1	1
Repetition (CM5)	0	0	0	1	1	1	0	0	0	1	1	1
Gate Control (CM15-CM13)	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE
Count to TC once, then disarm	X	X	X									
Count to TC twice, then disarm							X	X	X			
Count to TC repeatedly without disarming				X	X	X				X	X	X
Gate input does not gate counter input	X			X			X			X		
Count only during active gate level		X			X			X			X	
Start count on active gate edge and stop count on next TC			X			X						
Start count on active gate edge and stop count on second TC									X			X
No hardware retriggering	X	X	X	X	X	X	X	X	X	X	X	X
Reload counter from Load Register on TC	X	X	X	X	X	X						
Reload counter on each TC alternating reload source between Load and Hold Registers							X	X	X	X	X	X
Transfer Load Register into counter on each TC that gate is LOW, transfer Hold Register into counter on each TC that gate is HIGH.												
On active gate edge transfer counter into HOLD Register and then reload counter from Load register												

FIGURE 3. Function table.

Counter Mode	M	N	O	P	Q	R	S	T	U	V	W	X
Special Gate (CM7)	1	1	1	1	1	1	1	1	1	1	1	1
Reload Source (CM6)	0	0	0	0	0	0	1	1	1	1	1	1
Repetition (CM5)	0	0	0	1	1	1	0	0	0	1	1	1
Gate Control (CM15-CM13)	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE
Count to TC once, then disarm		X	X									
Count to TC twice, then disarm							X					
Count to TC repeatedly without disarming					X	X				X		X
Gate input does not gate counter input							X			X		
Count only during active gate level		X			X							
Start count on active gate edge and stop count on next TC			X			X						X
Start count on active gate edge and stop count on second TC												
No hardware retriggering							X			X		X
Reload counter from Load Register on TC		X	X		X	X						X
Reload counter on each TC alternating reload source between Load and Hold Registers												
Transfer Load Register into counter on each TC that gate is LOW, transfer Hold Register into counter on each TC that gate is HIGH.							X			X		
On active gate edge transfer counter into HOLD Register and then reload counter from Load register		X	X		X	X						
On active gate edge transfer counter into Hold register, but counting continues												X

NOTES:
1. Counter modes M, P, T, U and W are reserved and should not be used.

Counter Mode Operating Summary

FIGURE 3. Function table-Continued.

Counter Mode Operating Summary

Command Code								Command Description
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	E2	E1	G4	G2	G1	Load Data Pointer register with contents of E and fields. (G ≠ 000. G ≠ 110)
0	0	1	S5	S4	S3	S2	S1	Arm counting for all selected counters
0	1	0	S5	S4	S3	S2	S1	Load counters of specified source into all selected
0	1	1	S5	S4	S3	S2	S1	Load and Arm all selected counters
1	0	0	S5	S4	S3	S2	S1	Disarm and Save all selected counters
1	0	1	S5	S4	S3	S2	S1	Save all selected counters in Hold register
1	1	0	S5	S4	S3	S2	S1	Disarm all selected counters in Hold register
1	1	1	0	1	N4	N2	N1	Set Toggle out (High) for counter N (001 ≤ N ≤ 101)
1	1	1	0	0	N4	N2	N1	Clear Toggle out (Low) for counter N (001 ≤ N ≤ 101)
1	1	1	1	0	N4	N2	N1	Step counter N (001 ≤ N ≤ 101)
1	1	1	0	1	0	0	0	Set MM14 (Disable Data Pointer Sequencing)
1	1	1	0	1	1	1	0	Set MM12 (Gate off FOUT)
1	1	1	0	1	1	1	1	Set MM13 (Enter 16-bit bus mode)
1	1	1	0	0	0	0	0	Clear MM14 (Enable Data Pointer Sequencing)
1	1	1	0	0	1	1	0	Clear MM12 (Gate on FOUT)
1	1	1	0	0	1	1	1	Clear MM13 (Enter 8-bit bus mode)
1	1	1	1	1	0	0	0	Enable prefetch for write operations
1	1	1	1	1	0	0	1	Disable prefetch for write operations
1	1	1	1	1	1	1	1	Master reset

*Not to be used for asynchronous operations.

Command Summary

FIGURE 3. Function table-Continued.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
Input low voltage	V_{IL}	V_{CC} = 5 V ±5% All inputs except X2	1,2,3	V_{SS} -0.5	0.8	V
		V_{CC} = 5 V ±5% X2 input		V_{SS} -0.5	0.8	V
Input high voltage	V_{IH}	V_{CC} = 5 V ±5% All inputs except X2	1,2,3	2.2	V_{CC}	V
		V_{CC} = 5 V ±5% X2 input		3.8	V_{CC}	V
Input hysteresis	V_{ITH}	V_{CC} = 5 V ±5% SRC and GATE inputs only	1,2,3	0.2		V
Output low voltage	V_{OL}	V_{CC} = 5 V ±5% I_{OL} = 3.2 mA	1,2,3		0.4	V
Output high voltage	V_{OH}	V_{CC} = 5 V ±5% I_{OH} = -200 µA	1,2,3	2.4		V
Input load current	I_{IX}	Except X2 V_{CC} = 5.25 V V_{IN} = V_{CC} to 0 V	1,2,3		±10	µA
Input load current input X2	I_{IX2}	V_{CC} = 5.25 V V_{IN} = V_{CC} to 0 V	1,2,3		±100	µA
Output leakage current	I_{OZ}	V_{CC} = 5.25 V Except X 1 V_{SS} +0.4 ≤ V_{OUT} ≤ V_{CC} High-impedance state	1,2,3		±25	µA
V_{CC} supply current (steady state)	I_{CC}	V_{CC} = 5.25 V Outputs unloaded dynamic 1/	1,2,3		275	mA
Input capacitance	C_{IN}	f = 1 MHz, T_C = +25°C All pins not under test at 0 V See 4.3.1c	4		20	pF
Output capacitance	C_{OUT}				20	pF
IN/OUT capacitance	C_{IO}				20	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
C/$\overline{D}$ Valid to read low	t_{AVRL}	See figure 4 2/	9,10,11	25		ns
C/$\overline{D}$ Valid to write high	t_{AVWH}		9,10,11	170		ns
X2 High to X2 high (X2 period) 3/	t_{CHCH}		9,10,11	145		ns
X2 High to X2 low (X2 high pulse width) 3/	t_{CHCL}		9,10,11	70		ns
X2 Low to X2 high (X2 low pulse width) 3/	t_{CLCH}		9,10,11	70		ns
Data in valid to write high	t_{DVWH}		9,10,11	80		ns
Count source high to count source high (source cycle time) 4/	t_{EHEH}		9,10,11	145		ns
Count source pulse duration 4/	t_{EHEL} t_{ELEH}		9,10,11	70		ns
Count source high to F_{OUT} valid 4/	t_{EHFV}		9,10,11		500	ns
Count source high to gate valid (level gating hold time) 4/, 5/, 6/	t_{EHGV1}		9,10,11	10		ns
Count source high to read low (set-up time) 4/, 7/	t_{EHRL}		9,10,11	190		ns
Count source high to write high (set-up time) 4/, 8/	t_{EHWH}		9,10,11	-100		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$		Group A subgroups	Limits Min	Limits Max	Unit
Count source high to out valid 4/	t_{EHYV}	See figure 4 2/	T_C output	9,10,11		300	ns
			Immediate or delayed toggle output			300	ns
			Comparator output			350	ns
FN high to FN+1 valid 9/	t_{FN}			9,10,11		75	ns
Gate valid to count source high (level gating set-up time) 4/, 5/, 6/	t_{GVEH1}			9,10,11	100		ns
Gate valid to gate valid (gate pulse duration) 6/, 10/	t_{GVGV}			9,10,11	145		ns
Gate valid to write high 6/, 8/	t_{GVWH}			9,10,11	-100		ns
Read high to C/$\overline{D}$ don't care	t_{RHAX}			9,10,11	0		ns
Read high to count source high 3/, 11/	t_{RHEH}			9,10,11	0		ns
Read high to data out invalid	t_{RHQX}			9,10,11	10		ns
Read high to data out at high-impedance (data bus release time)	t_{RHQZ}			9,10,11		85	ns
Read high to read low (read recovery time)	t_{RHRL}			9,10,11	1000		ns
Read high to $\overline{CS}$ high 12/	t_{RHSH}			9,10,11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
Read high to write low (read recovery time)	t_{RHWL}	See figure 4 2/	9,10,11	1000		ns
Read low to data out valid	t_{RLQV}		9,10,11		110	ns
Read low to data bus driven (data bus drive time)	t_{RLQX}		9,10,11	20		ns
Read low to read high (Read pulse duration) 12/	t_{RLRH}		9,10,11	160		ns
$\overline{CS}$ low to read low 12/	t_{SLRL}		9,10,11	20		ns
$\overline{CS}$ low to write high 12/	t_{SLWH}		9,10,11	170		ns
Write high to C/$\overline{D}$ don't care	t_{WHAX}		9,10,11	20		ns
Write high to data in don't care	t_{WHDX}		9,10,11	20		ns
Write high to count source high 4/, 13/, 14/, 15/	t_{WHEH}		9,10,11	550		ns
Write high to gate valid 6/, 13/, 14/	t_{WHGV}		9,10,11	475		ns
Write high to read low (write recovery time) 16/	t_{WHRL}		9,10,11	1500		ns
Write high to $\overline{CS}$ high 12/	t_{WHSL}		9,10,11	20		ns
Write high to write low (write recovery time) 16/	t_{WHWL}		9,10,11	1500		ns
Write high to out valid 14/, 17/	t_{WHYV}		9,10,11		650	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
Write low to write high (write pulse duration) 12/	t_{WLWH}	See figure 4 2/	9,10,11	150		ns
Gate valid to count source high (special gate) 4/, 6/, 18/	t_{GVEH2}		9,10,11	200		ns
Count source high to gate valid (special gate) 4/, 6/, 19/	t_{EHGV2}		9,10,11	80		ns

1/ I_{CC} is measured while running a functional pattern with no loads applied.
2/ Test conditions:

V_{CC} = 5 V ±5%, V_{IL} = 0.45 V, V_{IH} = 2.4 V (see figure 6).
V_{OL} = 0.8 V , V_{OH} = 2.0 V, C_L = 100 pF.

3/ This parameter assumes X2 is driven from an external gate with a square wave.
4/ The enabled count source is one of F1-F5, TCN-1 SRC1-SRC5 or GATE1-GATE5, as selected in the applicable counter mode register. The timing diagram assumes the counter counts on rising source edges. The timing specifications are the same for falling-edge counting.
5/ This parameter applies to both edge and level gating (CM15-CM13 = 001 through 111 and CM7 = 0). This parameter represents the minimum setup or hold times to ensure that the gate ouput is seen at the intended level on the active source edge and the counter may be off by one count.
6/ This parameter assumes that the gatena input is unused (16-bit bus mode) or is tied high. In cases where the gatena input is used, this timing specification must be met by both the gate and gatena inputs.
7/ Any input transition that occurs before this minimum set-up requirement will be reflected in the contents read from the status register.
8/ Any input transition that occurs before this minimum set-up requirement will act on the counter before the execution of the operation initiated by the write and the counter may be off by one count.
9/ Signals F1-F5 cannot be directly monitored by the user. The phase difference between these signals will manifest itself by causing counters using two different F signals to count at different times on nominally simultaneous transitions in the F signals. F1 = X2.
10/ This parameter applies to edge gating (CM15-CM13 = 110 or 111) and gating when both CM7 = 1 and CM15 - CM13 < > 000. This parameter represents the minimum gate pulse width needed to ensure that the pulse initiates counting or counter reloading.
11/ Any input transition that occurs after this minimum hold time is guaranteed to not influence the contents read from the status register on the current read operation.
12/ This timing specification assumes that $\overline{CS}$ is active whenever $\overline{RD}$ or $\overline{WR}$ are active. $\overline{CS}$ may be held active indefintely.
13/ Any input transition that occurs after this minimum hold time is guaranteed to be seen by the counter as occurring after the action initiated by the write operation and the counter may be off by one count.
14/ This parameter assumes that the write operation is to be the command register.

15/ This timing specification applies to single action commands only (LOAD, ARM, SAVE, etc.). For double action commands such as LOAD and ARM and DISARM and SAVE, t_{WHEH} minmum = 700 ns.
16/ In short data write mode, t_{WHRL} and t_{WHWL} minimum = 1000 ns.
17/ This parameter applies to cases where the write operation causes a change in the output bit.
18/ This parameter applies to the hardware retrigger/save modes N, O, Q, R and X (CM7 = 1 and CM15 - CM13 < > 000). This parameter ensure that the gating pulse initiates a hardware retrigger/save operation.
19/ This parameter applies to hardware load source select modes S and V (CM7 = 1 and CM15 - CM13 = 000). This parameter represents the minimum hold time to ensure that the GATE input selects the correct load source on the active source edge.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

BUS TRANSFER SWITCHING WAVEFORMS

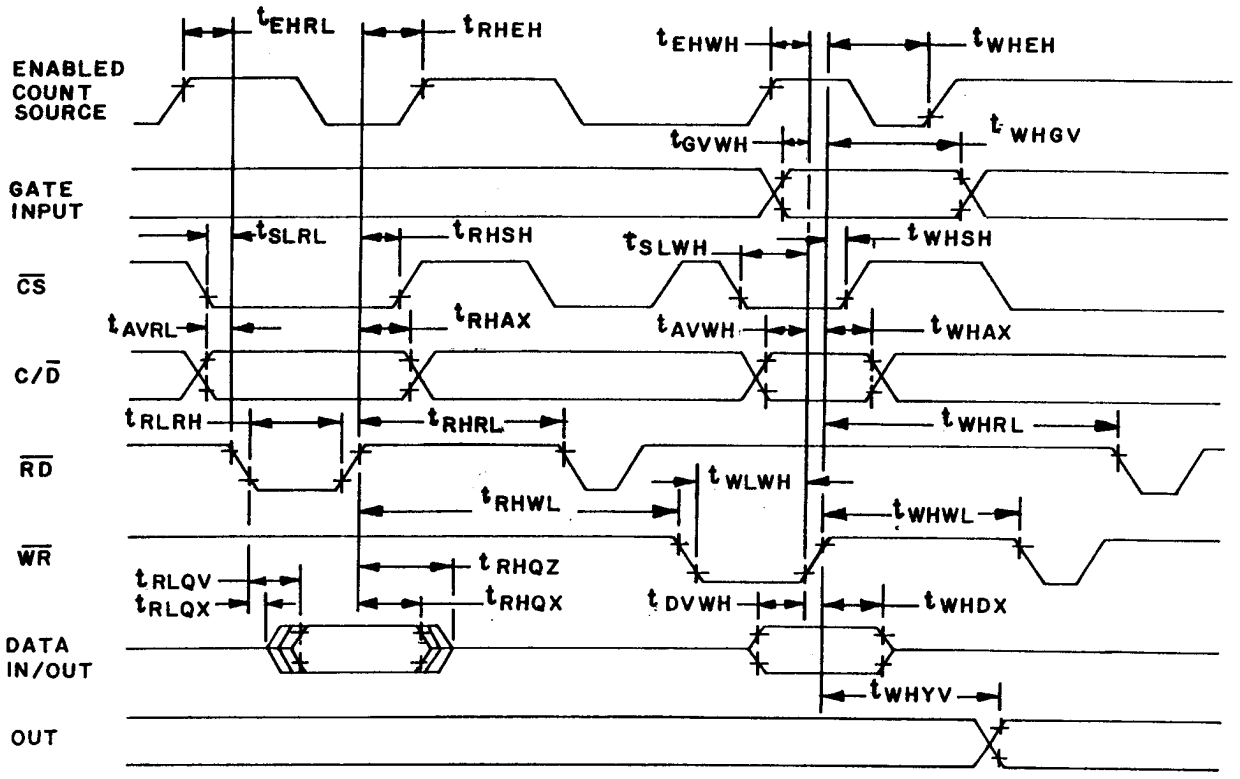

FIGURE 4. Switching waveforms.

COUNTER SWITCHING WAVEFORMS

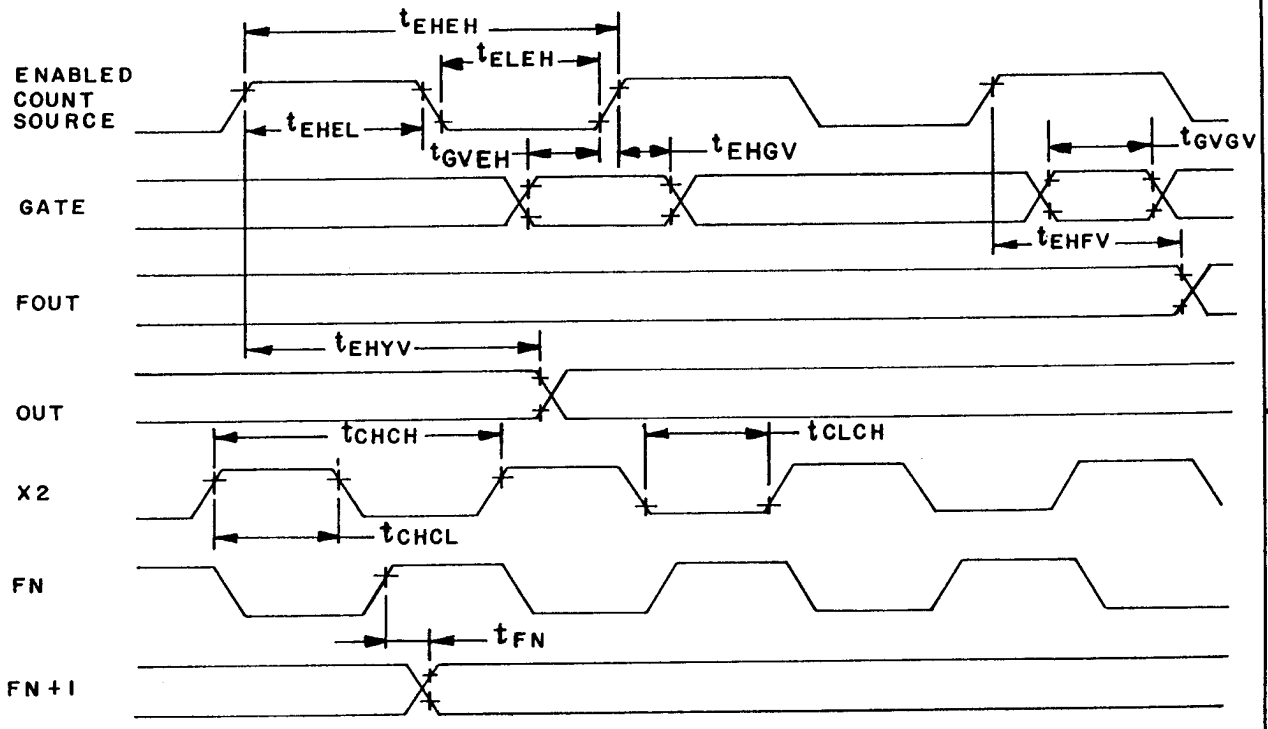

FIGURE 4. Switching waveforms - Continued.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT} and C_{IO} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 sufficient to verify the function table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9
Group A test requirements (method 5005)	1,2,3,7,8,9, 10**,11**
Groups C and D end-point electrical parameters (method 5005)	1,2,3
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin descriptions.

Pin no.	Name	I/O	Description
1	V_{CC}		+5 V Power supply.
21	V_{SS}		Ground.
5,6	X1, X2	O, I	(Crystal). X1 and X2 are the connections for an external crystal used to determine the frequency of the internal oscillator. The crystal should be a parallel-resonant, fundamental-mode type. An RC or LC or other reactive network may be used instead of a crystal. For driving from an external frequency source, X1 should be left open and X2 should be connected to a TTL source and a pull-up resistor.
7	f_{OUT}	O	(Frequency out). The f_{OUT} output is derived from a 4-bit counter that may be programmed to divide its input by an integer value from 1 through 16 inclusive. The input to the counter is selected from any of 15 sources, including the internal scaled oscillator frequencies. F_{OUT} may be gated on and off under software control and when off will exhibit a low impedance to ground. Control over the various f_{OUT} options resides in the master mode register. After power-up, f_{OUT} provides a frequency that is 1/16 that of the oscillator. The input source on power-up is F1.
4, 39 36-34	GATE 1- GATE 5	I	(Gate). The gate inputs may be used to control the operations of individual counters by determining when counting may proceed. The same gate input may control up to three counters. Gate pins may also be selected as count sources for any of the counters and for the F_{OUT} divider. The active polarity for a selected gate input is programmed at each counter. Gating function options allow level-sensitive gating or edge-initiated gating. Other gating modes are available including one that allows the gate input to select between two counter output frequencies. All gating functions may also be disabled. The active gate input is conditioned by an auxiliary input when the unit is operating with an external 8-bit data bus. Schmitt-trigger circuitry on the gate inputs allows slow transition times to be used.

Pin no.	Name	I/O	Description
39-29	SRC1-SRC5	I	(Source). The source inputs provide external signals that may be counted by any of the counters. Any source line may be routed to any or all of the counters and the f_{OUT} divider. The active polarity for a selected SRC input is programmed at each counter. Any duty cycle waveform will be accepted as long as the minimum pulse width is at least half the period of the maximum specified counting frequency for the part. Schmitt-trigger circuitry on the SRC inputs allows slow transition times to be used.
3, 2, 40, 38, 37	OUT1-OUT5	O	(Counter). Each 3-state OUT signal is directly associated with a corresponding individual counter. Depending on the counter configuration, the OUT signal may be a pulse, a square wave, or a complex duty cycle waveform. OUT pulse polarities are individually programmable. The output circuitry detects the counter state that would have been all bits zero in the absence of a reinitialization. That information is used to generate the selected waveform type. An optional output mode for counters 1 and 2 overrides the normal output mode and provides a true OUT signal when the counter contents match the contents of an alarm register.
12-19, 20, 22-28	DB0-DB7, DB8-DB15	I/O	(Data bus). The 16 bidirectional data bus lines are used for information exchanges with the host processor. High on a data bus line corresponds to one and low corresponds to zero. These lines act as inputs when $\overline{WR}$ and $\overline{CS}$ area active and as outputs when $\overline{RD}$ and $\overline{CS}$ are active. When $\overline{CS}$ is inactive, these pins are placed in a high-impedance state. After power-up or reset, the data bus will be configured for a 8-bit width and will use only DB0 through DB7. DB0 is the least significant and DB7 is the most significant bit position. The data bus may be reconfigured for 16-bit width by changing a control bit in the master mode register. This is accomplished by writing an 8-bit command into the low-order DB lines while holding the DB13-DB15 lines at a logic high level. Thereafter, all 16 lines can be used, with DB0 as the least significant and DB15 as the most significant bit position. When operating in the 8-bit data bus environment, DB8-DB15 will never be driven active by the device. DB8 through DB12 may optionally be used as additional gate inputs (see figure 1-3). If unused, they should be held high. When pulled low, a gatena signal will disable the action of the corresponding counter N gating. DB13-DB15 should be held high in 8-bit bus mode whenever $\overline{CS}$ and $\overline{WR}$ are simultaneously active.

Pin no.	Name	I/O	Description
10	$\overline{CS}$	I	(Chip select). The active-low chip select input enables read and write operations on the data bus. When chip select is high, the read and write inputs are ignored. The first chip select signal after power-up is used to clear the power-on reset circuitry. If chip select is tied to ground permanently, the power-on reset circuitry may not function. In such a configuration, the software reset command must be issued following power-up to reset the device.
11	$\overline{RD}$	I	(Read). The active-low read signal is conditioned by chip select and indicates that internal information is to be transferred to the data bus. The source will be determined by the port being addressed and , for data port reads, by the contents of the data pointer register. $\overline{WR}$ and $\overline{RD}$ should be mutually exclusive.
9	$\overline{WR}$	I	(Write). The active-low write signal is conditioned by chip select and indicates that data bus information is to be transferred to an internal location. The destination will be determined by the port being addressed and, for data port writes, by the contents of the data pointer register. $\overline{WR}$ and $\overline{RD}$ should be mutually exclusive.
8	C/$\overline{D}$	I	(Control/data). The control/data signal selects source and destination locations for the read and write operations on the data bus. Control write operations load the command register and the data pointer. Control read operations output the status register. Data read and data write transfers communicate with all other internal registers. Indirect addressing at the data port is controlled internally by the data pointer register.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor FSCM number	Vendor similar part number 1/
5962-8552301QX	34335	AM9513A/BQA
5962-8552301XX	34335	AM9513A/BUC

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor FSCM number	Vendor name and address
34335	Advanced Micro Devices, Inc. 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088