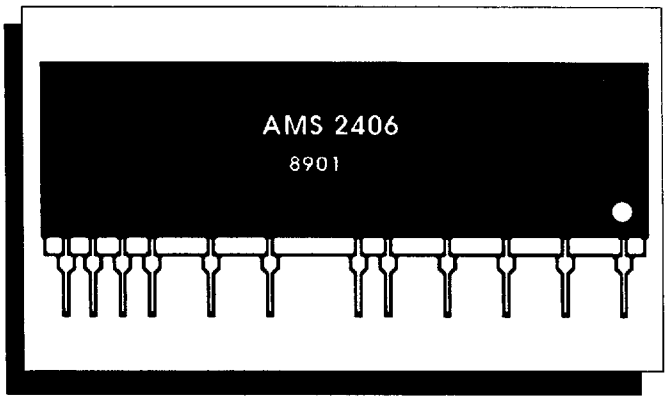
aptek microsystems

# AMS 2406
# STATION LINE INTERFACE CIRCUIT

## DESCRIPTION

The AMS 2406 SLIC is a thick film hybrid station line interface circuit in a single-in-line package which performs all of the line interface requirements for a Private Automatic Branch Exchange (PABX).

The 2406 addresses the need for an economical alternative to transformer line circuits in 24 volt telephone systems.




## FEATURES

- Minimum component count
- Hybrid (2 wire - 4 wire) function
- Off-hook detection/dial pulse monitoring
- Ring relay control - automatic ring trip
- Internal battery feed resistors
- Internal 600 Ohm balance network

## FUNCTION AND PINOUTS

| NAME | FUNCTION | | I/O | A/D | PIN |
|---|---|---|---|---|---|
| Ring | R | Ring (A) side of loop | * | A | 3 |
| Tip | T | Tip (A) side of loop | * | A | 5 |
| Receive | RX | 4-wire receive port | I | A | 13 |
| Transmit | TX | 4-wire transmit port | O | A | 15 |
| Switch Hook Detect | SHD- | Off-hook indicator (low true) | O | D | 19 |
| Ring Control | RC+ | Engage ring relay (high true) | I | D | 17 |
| Relay Drive | RD+ | Output to relay driver (high = engage relay) | O | D | 18 |
| Positive Supply | $V_A$ | $+5V_{DC}$ | --- | --- | 7 |
| Negative Supply | $V_B$ | -24V "Battery" | --- | ---- | 9 |
| Ground | GND | Supply and signal reference | ---- | ---- | 1, 10, 20 |
| * Bi-directional (simultaneous input and output) pin. | | | | | |

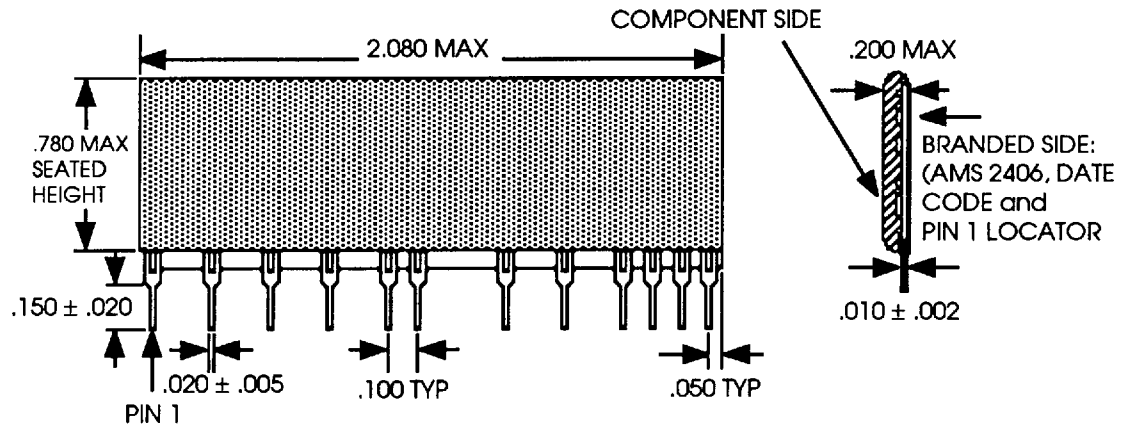



***Figure 1.*** **2406 PACKAGE DRAWING WITH COMPONENT SIDE SHOWN**

## ABSOLUTE MAXIMUM RATING

| PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|
| $V_A$ | -0.5 | +7 | $V_{DC}$ |
| $V_B$ | -28 | +0.5 | $V_{DC}$ |
| Logic Inputs | -0.5 | +7 | $V_{DC}$ |
| Analog Inputs | | 3.5 | $V_{RMS}$ |
| Storage Temperature | -40 | +85 | °C |
| Storage Humidity | | 95 | % RH |
| Power Dissipation | | 2.0 | W |
| Output Short Circuit Duration (any one output) | | ∞ | Sec |
| Soldering | | 5 | Sec @ 270°C |

**NOTE:** The device will withstand any one parameter at its absolute maximum rating provided that all other parameters are within their normal operating limits.

## POWER REQUIREMENTS (Voltages are relative to GROUND)

| NAME | MIN | NOM | MAX | UNIT | NOTES |
|---|---|---|---|---|---|
| $V_A$ | +4.7 | +5 | +5.3 | $V_{DC}$ | Positive supply voltage |
| $I_A$ | | +4.0 | +9.0 | mA | Plus loop current |
| $V_B$ | -21.6 | -24 | -26.4 | $V_{DC}$ | Negative supply voltage |
| $I_B$ | | -3.0 | - 9.0 | mA | Plus loop current |

## ENVIRONMENTAL REQUIREMENTS

| PARAMETER | MIN | MAX | UNIT | NOTES |
|---|---|---|---|---|
| Operating Temperature | 0 | +70 | °C | |

## DC & SUPERVISION CHARACTERISTICS

$V_A$ = +5.0 V, $V_B$ = -24. 0 V, Temp = 25° C

| NAME | MIN | NOM | MAX | UNIT | NOTES |
|---|---|---|---|---|---|
| SHD | | 9.0 | | mA | Loop current threshold for switch hook detect |
| $V_{RING}$ | | 24 | | V | Source resistance = 300 Ohms, $I_{LOOP}$ = 0 |
| $V_{TIP}$ | -0.1 | 0 | +0.1 | V | Source resistance = 300 Ohms, $I_{LOOP}$ = 0 |
| $I_{LOOP}$MAX | | | 42 | mA | $R_{LOOP}$ = 0 |
| $R_{LOOP}$MAX | | | 600 | Ohms | $I_{LOOP} \geq$ 19 mA |
| $I_{RING}$MAX | | | 81 | mA | Ring to ground short |
| $I_{TIP}$MAX | | | 2 | mA | Tip to ground short |

## LOGIC LEVELS AND CURRENTS

The SHD- output and RC+ input are compatible with industry standard LS TTL and CMOS logic families.

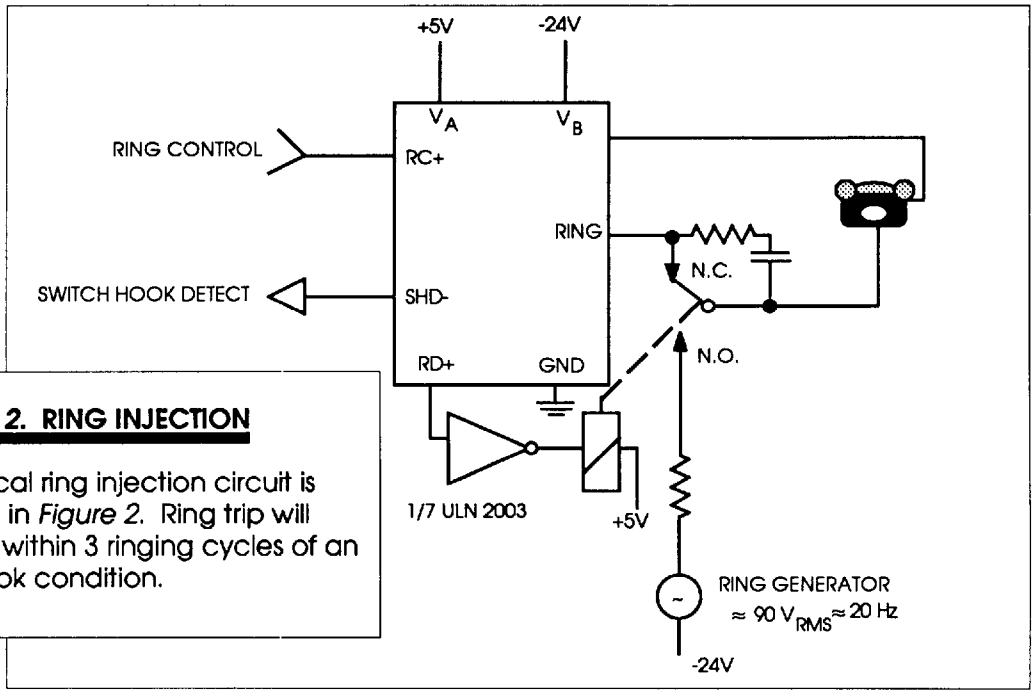



***Figure 2.* RING INJECTION**

A typical ring injection circuit is shown in *Figure 2.* Ring trip will occur within 3 ringing cycles of an off-hook condition.

## TRANSMISSION CHARACTERISTICS

VA = +5.0 V, VB = -24.0 , Temp = 25°C

| PARAMETER | CONDITIONS | MIN | MAX | UNIT | NOTES |
|---|---|---|---|---|---|
| Receive Insertion Loss | $V_{IN}$ = 0 dBm<br>f = Hz | -0.3 | +0.3 | dB | |
| Receive Frequency Response | $V_{IN}$ = 0 dBm<br>200 Hz ≤ f ≤ 3400 Hz | -.25 | +0.1 | dB | 1 |
| Transmit Insertion Loss | $V_{IN}$ = 0 dBm<br>f = 1KHz | -0.3 | +0.3 | dB | |
| Transmit Frequency Response | $V_{IN}$ = 0 dBm<br>200 Hz ≤ f ≤ 3400 Hz | -.25 | +0.1 | dB | 1 |
| Receive Idle Channel Noise | Loop Termination = 600 Ohms, $V_{RX}$ = 0V | | 8 | dBrnC | |
| Transmit Idle Channel Noise | Loop termination = 600 Ohms<br>$V_{LOOP}$ = 0V, $V_{RX}$ =0V | | 8 | dBrnC | |
| Two Wire Return Loss (ERL) | | 30 | | dB | 2 |
| Two Wire Return Loss (Single Frequency) | 200Hz ≤ f ≤ 3400 Hz | 20 | | dB | 2 |
| Trans-Hybrid Loss | Loop termination =600Ω<br>300 Hz ≤ f ≤ 3000 Hz | 25 | | dB | |
| Longitudinal to Metallic Balance | Per IEEE Std. 455-1976,<br>VS = 1.0 $V_{RMS}$<br><br>50 Hz ≤ f ≤ 1500 Hz | 60 | | dB | |

**NOTES :**
1. Relative to response at 1.0 kHz
2. Reference impedance = 600 Ohms

## APPLICATION INFORMATION

### LOSS PLAN

The SLIC has nominally zero insertion loss in each direction. However, the input and output impedances (ZRX and ZTX, respectively) are such that when two SLIC's are interconnected through a FET switching matrix (RDS on typ. 80 Ohms), the system insertion loss is nominally 5 dBm in each direction. This allows analog systems to meet the loss requirements of EIA RS—464, Paragraph 4.9.2.2.1 with a minimum of external parts — See *Figure 3.* Also, the positive DC offset at TX allows the FET switch to operate in its linear region without a pull-up resistor.

### TRANSMISSION TEST SET CONTROL SETTING:

- Send (Left)
- Receive Bridge (Right)
- Receive = Tone (Normal)
- Send Level = 0 dBm
- Frequency = 1 kHz

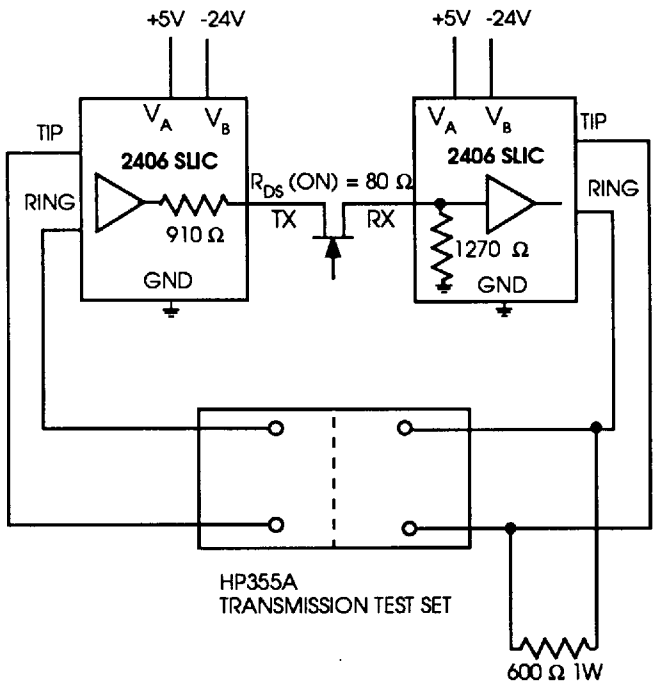



***Figure 3.*** **MINIMAL ANALOG INTERCONNECTION**
INSERTION LOSS = 5.0 dB NOM.