

OCTA BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LS TTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT540 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$. A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The "540" is identical to the "541" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	9	11	ns
C_I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	39	44	pF

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1, \overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}_0$ to $\overline{Y}_7$	bus outputs
20	V_{CC}	positive supply voltage

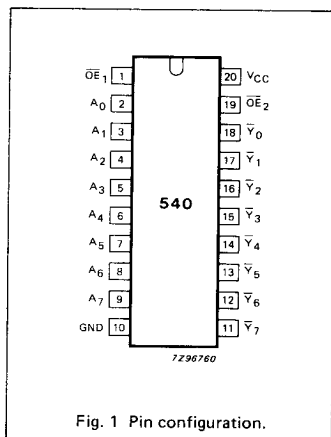


Fig. 1 Pin configuration.

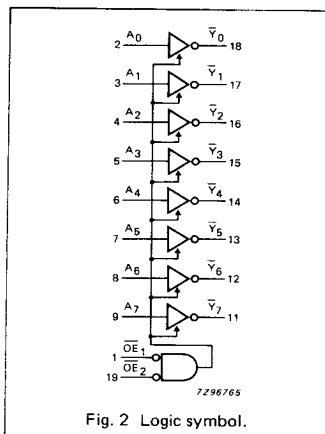


Fig. 2 Logic symbol.

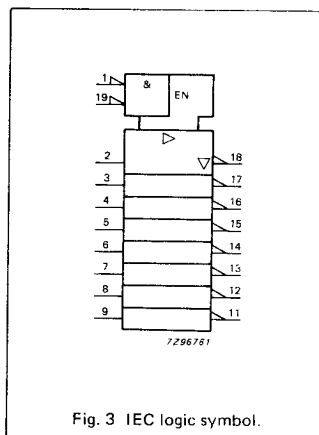


Fig. 3 IEC logic symbol.

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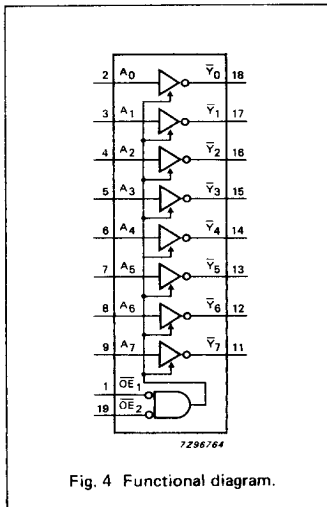


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	A_n	$\overline{Y}_n$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

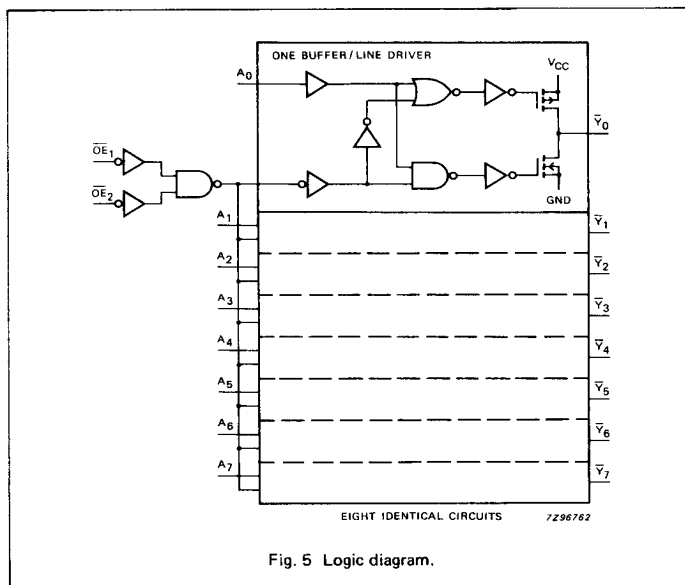


Fig. 5 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to Y _n		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t _{PZH} / t _{PZL}	3-state output enable time OE _n to Y _n		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t _{PHZ} / t _{PLZ}	3-state output disable time OE _n to Y _n		61 22 18	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

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For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$	1.50
$\overline{OE}_2$	1.00
A_n	1.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to $\overline{Y}_n$		13	24		30		36	ns	4.5	Fig. 6
t _{PZH} / t _{PZL}	3-state output enable time $\overline{OE}_n$ to $\overline{Y}_n$		22	35		44		53	ns	4.5	Fig. 7
t _{PHZ} / t _{PLZ}	3-state output disable time $\overline{OE}_n$ to $\overline{Y}_n$		23	35		44		53	ns	4.5	Fig. 7
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

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AC WAVEFORMS

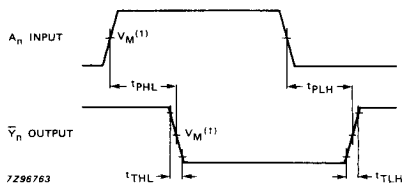


Fig. 6 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

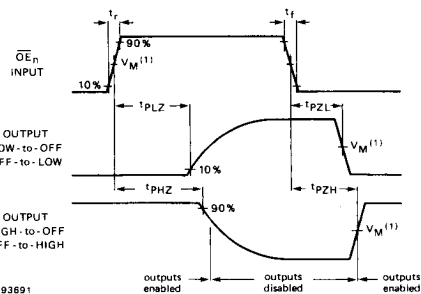


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.