Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS TRANSCEIVERS

IDT54/74FCT861A/B
IDT54/74FCT863A/B

FEATURES:

- Equivalent to AMD's Am29861-64 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT861A/863A equivalent to FAST™ speed
- **IDT54/74FCT861B/863B 25% faster than FAST**
- High-speed symmetrical bidirectional transceivers
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

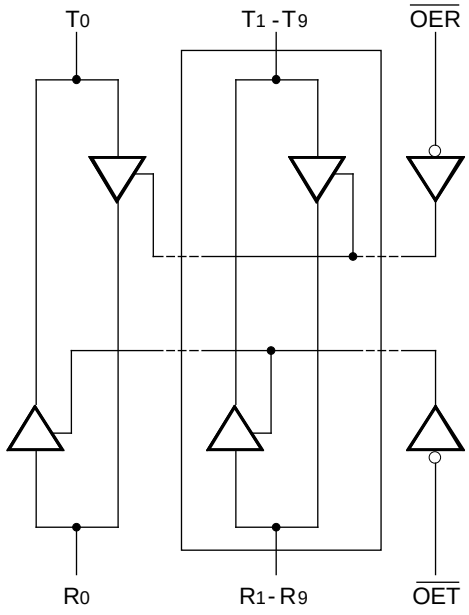
The IDT54/74FCT800 series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT860 series bus transceivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The IDT54/74FCT863 9-bit transceivers have NAND-ed output enables for maximum control flexibility.

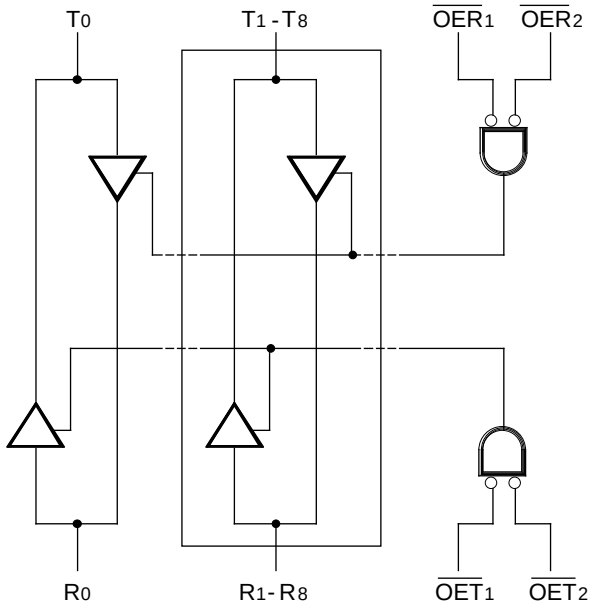
All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high- impedance state.

FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT861



IDT54/74FCT863



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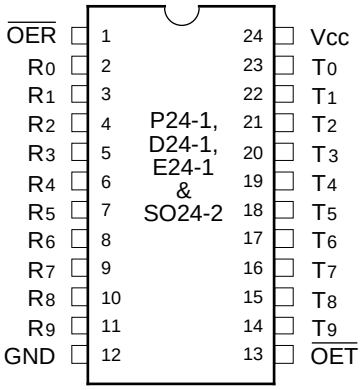
PRODUCT SELECTOR GUIDE

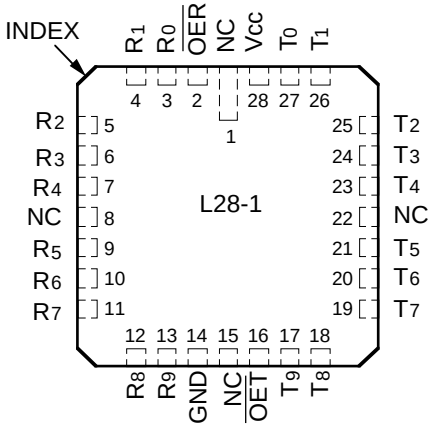
	Device	
	10-Bit	**9-Bit**
Non-inverting	IDT54/74FCT861	IDT54/74FCT863

PIN CONFIGURATIONS

IDT54/74FCT861 10-BIT TRANSCEIVERS

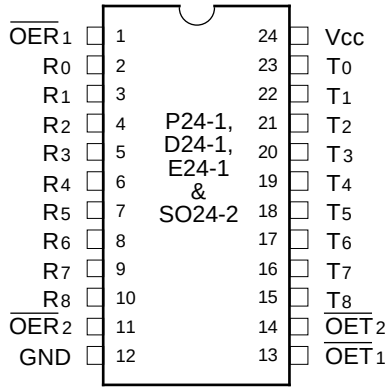


DIP/CERPACK/SOIC
TOP VIEW

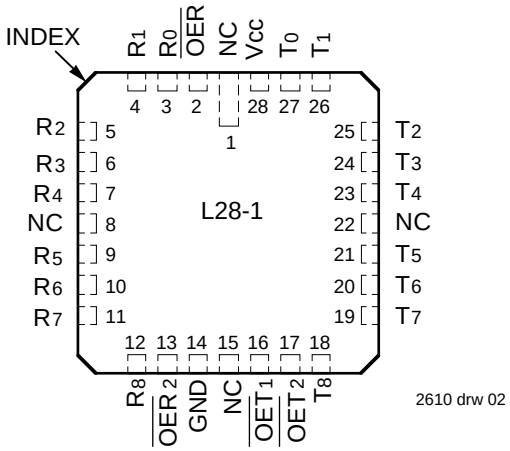


LCC
TOP VIEW

IDT54/74FCT863 9-BIT TRANSCEIVERS



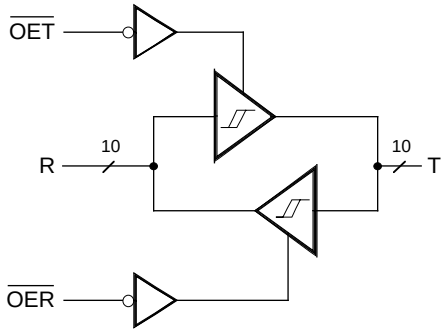
DIP/CERPACK/SOIC
TOP VIEW



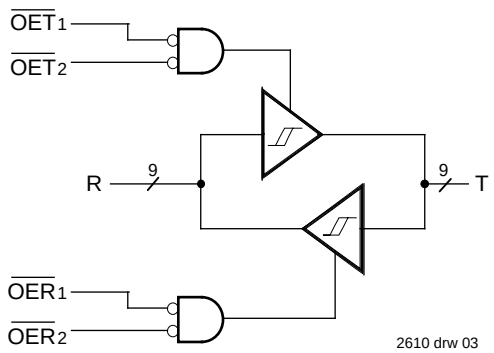
LCC
TOP VIEW

LOGIC SYMBOLS

IDT54/74FCT861



IDT54/74FCT863



PIN DESCRIPTION

Name	I/O	Description
IDT54/74FCT861		
$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$ HIGH activates the RECEIVE mode.
$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$ HIGH activates the TRANSMIT mode.
R_I	I/O	10-bit RECEIVE input/output.
T_I	I/O	10-bit TRANSMIT input/output.
IDT54/74FCT863		
$\overline{OER}_I$	I	When LOW in conjunction with $\overline{OET}_I$ HIGH activates the RECEIVE mode.
$\overline{OET}_I$	I	When LOW in conjunction with $\overline{OER}_I$ HIGH activates the TRANSMIT mode.
R_I	I/O	9-bit RECEIVE input/output.
T_I	I/O	9-bit TRANSMIT input/output.

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FUNCTION TABLE(1)

IDT54/74FCT861/863 (Non-inverting)

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_I	T_I	R_I	T_I	Function
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE: 2610 tbl 02

1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2610 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2610 tbl 04

1. This parameter is guaranteed by characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	–5[4]	µA
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O pins Only)		V_I = 0.5V	—	—	–15[4]	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –15mA MIL.	2.4	4.3	—	
			I_{OH} = –24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.[5]	—	0.3	0.5	
			I_{OL} = 48mA COM'L.[5]	—	0.3	0.5	

2610 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 10 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 480mA for commercial and 320mA for military. Derate I_{OL} for number of outputs exceeding 10 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OER}$ or $\overline{OET}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$\overline{OER}$ or $\overline{OET}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		$\overline{OER}$ or $\overline{OET}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2610 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

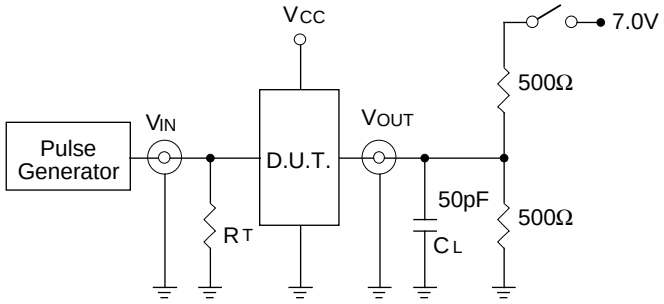
Symbol	Parameter	Condition[1]	FCT861A/863A Com'l. Min.[2]	FCT861A/863A Com'l. Max.	FCT861A/863A Mil. Min.[2]	FCT861A/863A Mil. Max.	FCT861B/863B Com'l. Min.[2]	FCT861B/863B Com'l. Max.	FCT861B/863B Mil. Min.[2]	FCT861B/863B Mil. Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay R_I to T_I or T_I to R_I FCT861/863	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OET}$ to T_I or $\overline{OER}$ to R_I	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	20.0	1.5	22.0	1.5	15.0	1.5	16.0	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OET}$ to T_I or $\overline{OER}$ to R_I	C_L = 5pF[3] R_L = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This condition guaranteed but not tested.

2610 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

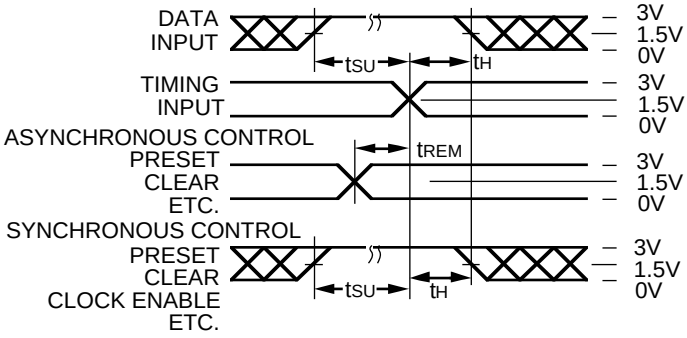
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2610 tbl 08

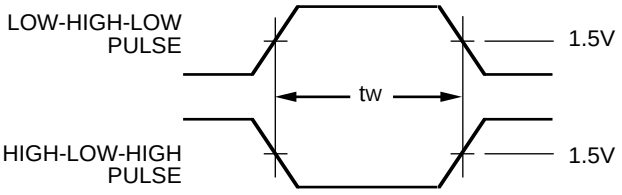
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



PULSE WIDTH



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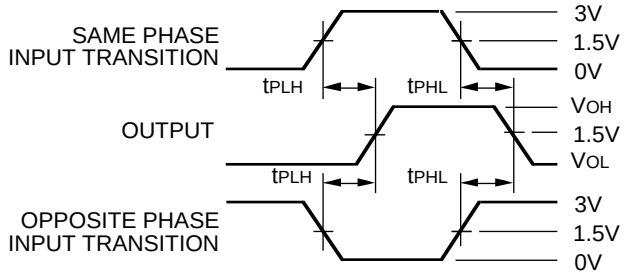
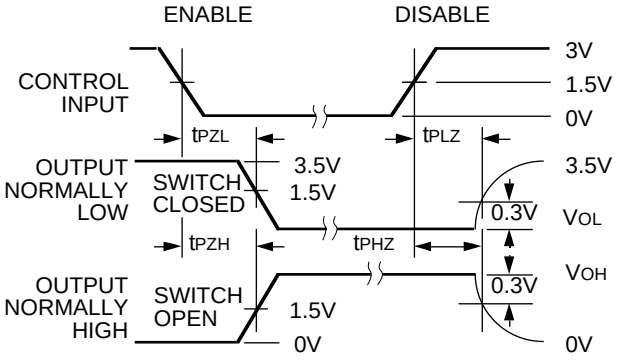


ENABLE AND DISABLE TIMES



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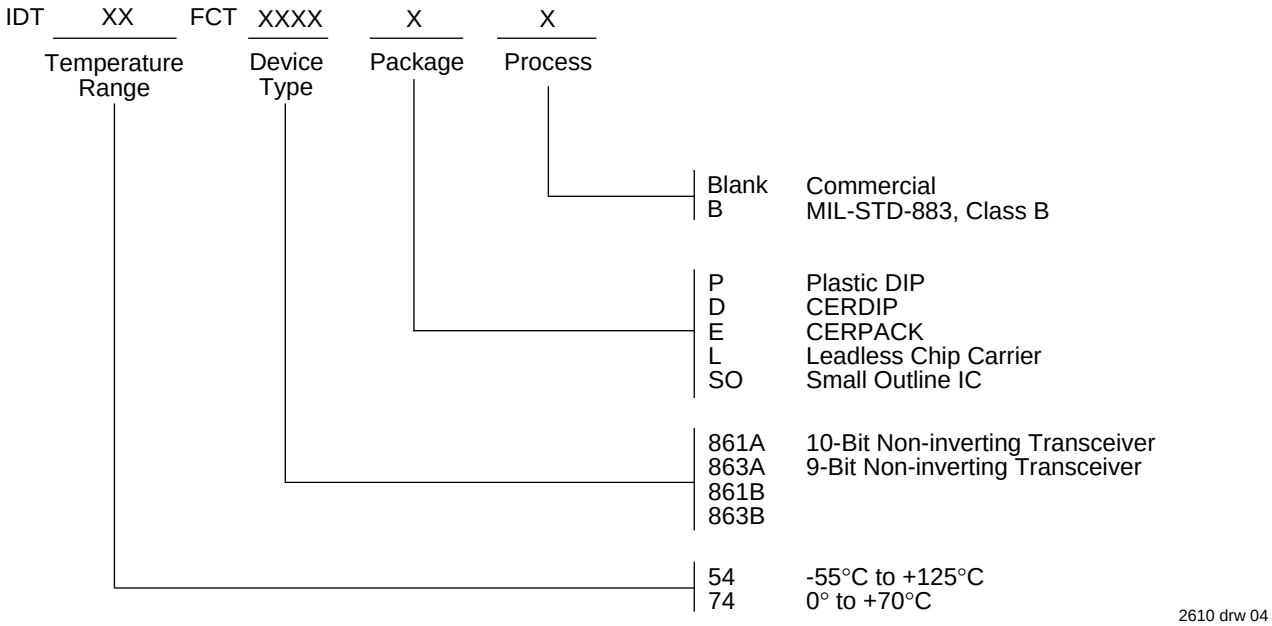
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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