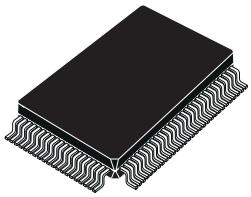
L6452

Dual 13x16 Matrix Head Ink Jet Driver

Features

- DRIVES TWO 13X16 MATRIX HEADS
- HEAD TEMPERATURE SENSING
- POWER UP SYSTEM
- ELECTRICAL NOZZLE CHECK
- 8 BIT A/D
- 5 BIT D/A
- ± 4KV ESD PROTECTED OUTPUTS



PQFP100

Description

L6452 is a device designed to drive two 13x16 matrix ink jet print heads in printer applications.

The output stage is able to source simultaneously 400 mA on each of the 16 power lines (columns) with a duty cycle of 33% in normal printing and 66% in head pre-heating. On the address lines (rows), the load is only capacitive (MOS FET driving capability). The driver can control two print heads, but only one is active at a time. The address scanning counter is included and can be disabled to allow a different scanning scheme.

In order to avoid output activation during the supply transient, an internal power-up system is implemented.

As supporting function, L6452 is capable of sensing the head silicon temperature and to electrically check each nozzle.

The device is also integrating a thermal protection.

Order codes

Part number	Op. Temp range, °C	Package	Packing
E-L6452	0 to 70	PQFP100	Tray
L6452DIE8	0 to 70	DIE	--

Contents

1 Block diagrams

Figure 1. Block diagram

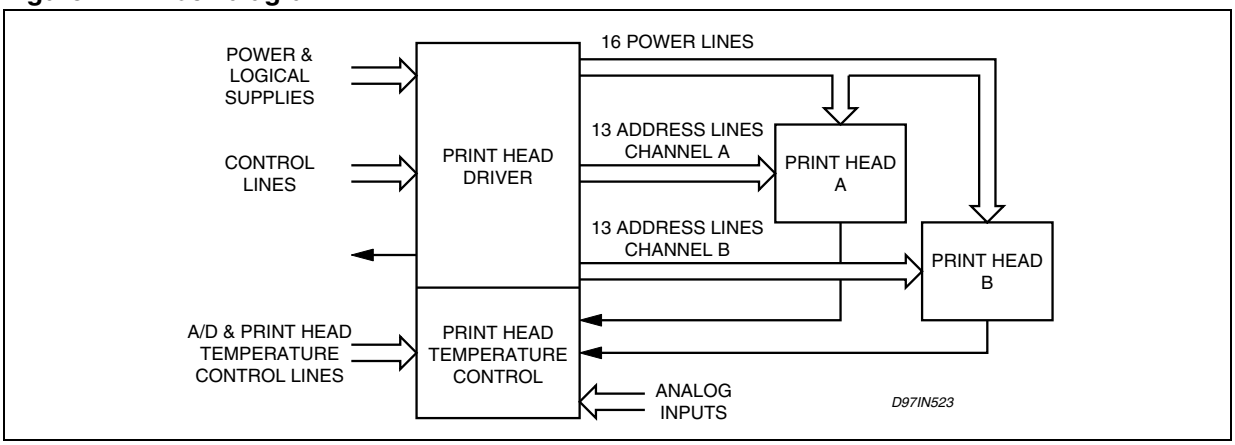


Figure 2. Block Diagram: Power Line Output Stage.

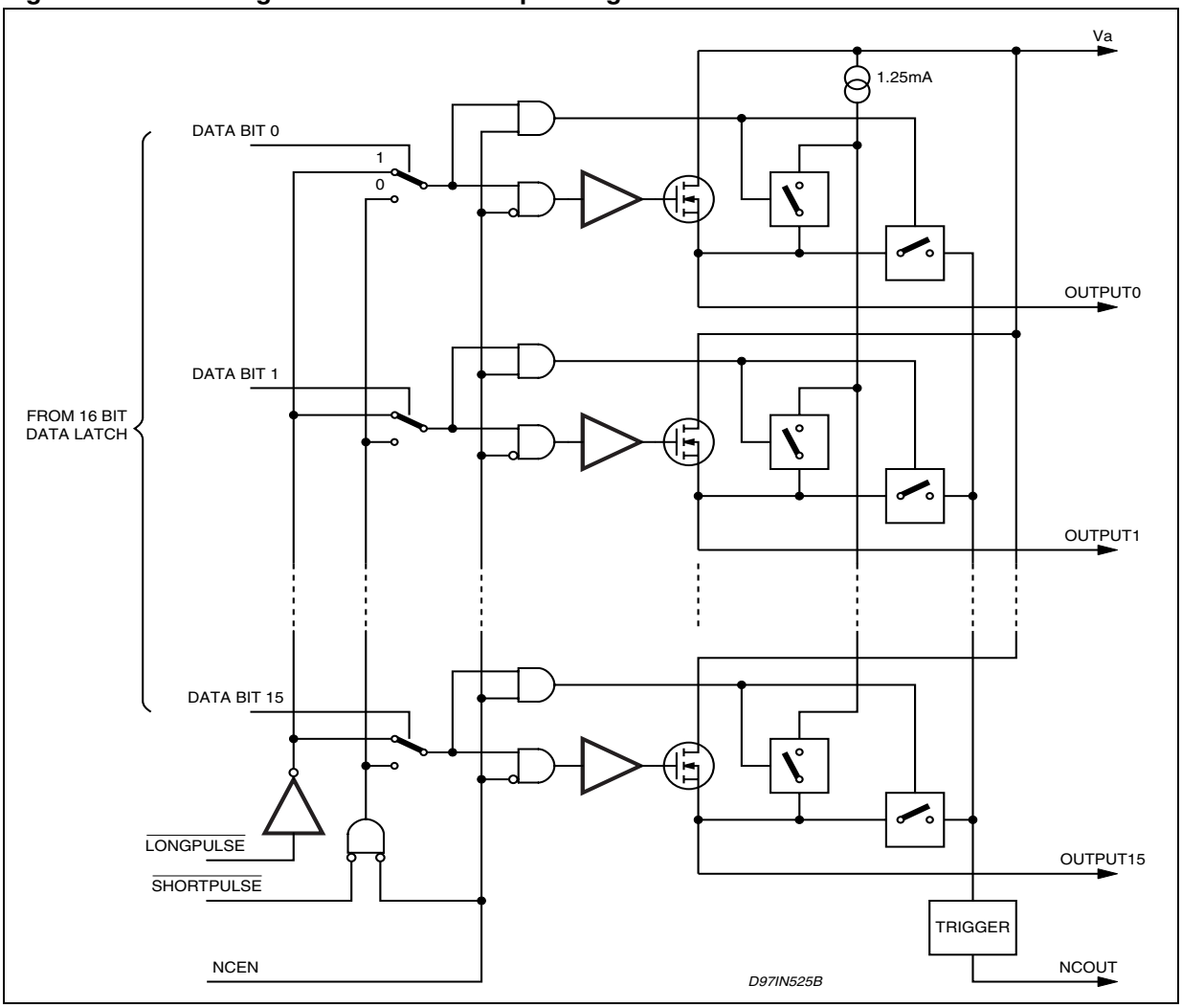
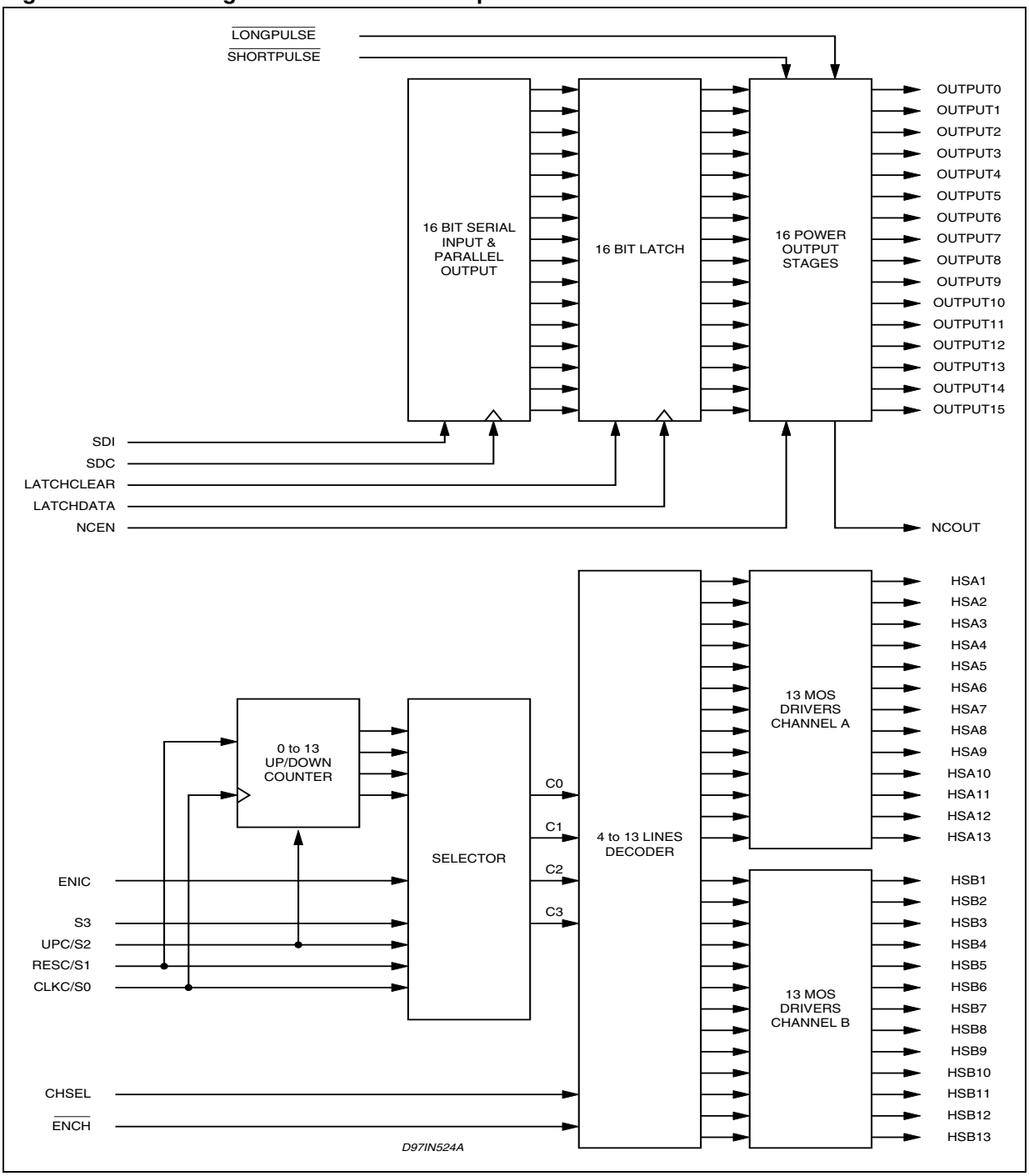


Figure 3. Block Diagram: Nozzle activation part



2 Pin description

Figure 4. Pin connection (Top view)

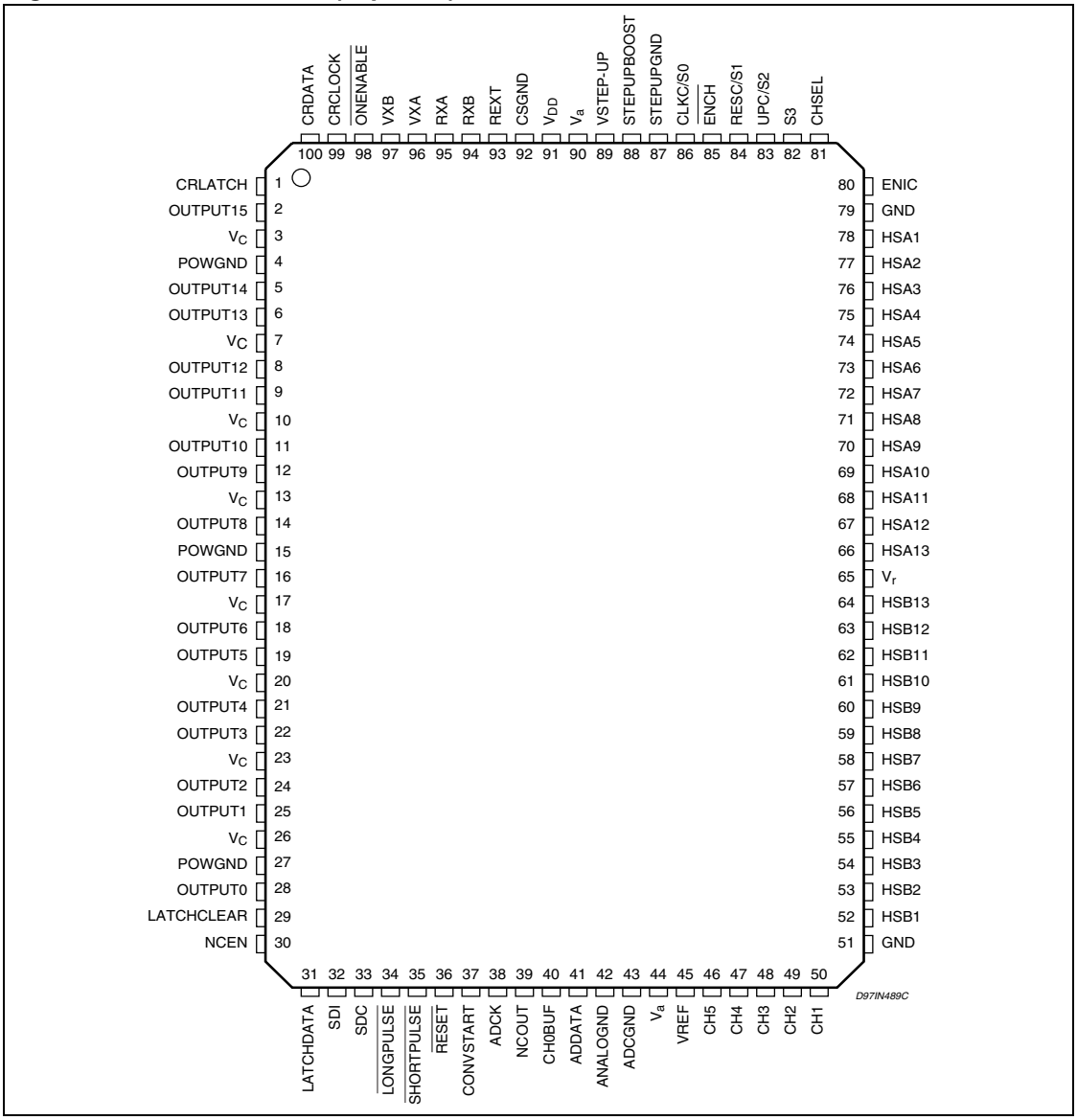


Table 1. Pin function

Pin #	Name	Function
1	CRlatch	A rising edge transfer the information from CR shift register into the control register latching the data on the falling edge
2, 5, 6, 8, 9, 11, 12, 14, 16, 18, 19, 21, 22, 24, 25, 28	Output15...0	High side DMOS outputs. To be active, $\overline{\text{ShortPulse}}$ and/or $\overline{\text{LongPulse}}$ and NcEn must have a low level

Table 1. Pin function - continued

Pin #	Name	Function
3, 7, 10, 13, 17, 20, 23, 26	Vc	Outputs Power Supply
4, 15, 27, 51, 79, 92	GND	logic and power ground
29	LatchClear	A high level resets all bit in the latch
30	NcEn	A high level enables the internal current sources and disables all DMOS outputs. To be active, the internal current sources must have their corresponding bit set in the 16 bit latch and $\overline{\text{LongPulse}}$ must be set to low level. This function is called Nozzle Check Enable.
31	LatchData	A rising edge latches the 16 bit stored in the shift register in the 16 bit latch
32	SDI	Serial data input of the shift register
33	SDC	The data bit presented to the SDI pin is stored into the register on the rising edge of this pin
34	$\overline{\text{LongPulse}}$	A low level activates all outputs having their corresponding bit in the 16 bit latch set (this pin has an internal pull-up resistor)
35	$\overline{\text{ShortPulse}}$	A low level activates all outputs having their corresponding bit in the 16 bit latch reset (this pin has an internal pull-up resistor)
36	$\overline{\text{Reset}}$	A low level disables all functions and clears all registers
37	ConvStart	A high level enables the A/D to start the new conversion
38	ADCK	A/D clock signal; the ADDATA signal are valid on the falling edge of this pin
39	NCOut	If NcEn is high this output provides a high level when the open load is detected on the output. If NcEn is low this output provides a high level when a short circuit is detected on HSA/B output
40	CH0buf	Analog output signal (CH0 buffered)
41	ADDATA	A/D serial data output
42	AnalogGND	Analog ground connection
43	ADCGND	Ground of internal ADC
44, 90	Va	Power supply
45	Vref	Reference voltage generator
46 to 50	CH5..CH1	A/D input signals
52 to 64	HSB1..HSB13	Head selector address output channel B
65	Vr	Head Select Power Supply
66 to 78	HSA13..HSA1	Head selector address output channel A
80	EnIC	Enable Internal Counter: A high level enables the counter and the internal decoder will activate of the HSx outputs according to the counter's outputs. Signal S0 becomes ClkC and S1 becomes ResC

Table 1. Pin function - continued

Pin #	Name	Function
81	ChSel	Channel Select: A low level enables channel A and a high level enables channel B
82	S3	Decoder input signals when EnIC is low
83	UpC/S2	UpCount/S2: A high level enables the internal counter to up counting. A low level enables down counting depending on EnIC value it becomes S2.
84	ResC/S1	Reset Count/S1: A low level resets the internal counter depending on EnIC value it becomes S1.
85	$\overline{\text{EnCh}}$	Enable Channel: A low level enables the selected channel (this input has an internal pull up resistor)
86	ClkC/S0	A high level clocks the internal counter depending on EnIC value it becomes S0.
87	StepUpGND	Ground of step up block
88	StepUpBoost	Boost voltage
89	VstepUp	Driving voltage of power DMOS stage
91	VDD	5V logic supply
93	Rext	An external resistor connected to ground fixes the internal current source value
94, 95	RxB, RxA	Current source outputs
96, 97	VxA, VxB	RxA, RxB voltage after an optional external filter
98	$\overline{\text{OnEnable}}$	A low level enables the current source generator according the $\overline{\text{A}}$/B and ON/$\overline{\text{O}}$FF control register bit
99	CRclock	Data on pin CRdata are stored into the register on the rising edge of this pin
100	CRdata	Control register serial data input

3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_c	Power line supply voltage	14	V
V_r	Address line supply voltage	14	V
Va	Analog supply voltage	14	V
V_{dd}	Logic supply voltage	6	V
V_{step_up}	Driving voltage of power DMOS stage	28	V
ESD	In accordance with IEC 1000-4-2 (1)	±4	kV
V_{in}	Logic input voltage range	-0.3 to V_{dd} + 0.3	V
I_{out}	Output continuous current	0.5	A
T_j	Junction temperature	150	°C
T_{amb}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-55 to 150	°C

(1) All the pins connected to the pen passed ESD Contact Electrostatic Discharge @ ±4kV (150pF, 330Ohm source).

3.2 DC Electrical characteristics

Table 3. DC Electrical characteristics (T_j = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_c	Power Line Supply voltage	(1)	10.5 (2)	11.5	12.5	V
V_r	Address line supply voltage	*(1)*	10.5	11.5	12.5	V
V_a	Analog supply voltage	*(1)*	10.5	11.5	12.5	V
V_{dd}	Logic supply voltage		4.5	5	5.5	V
I_{cs}	V_c sleep supply current	$\overline{OnEnable}$ = 1 $\overline{Reset}$ = 0			1	mA
I_{rs}	V_r sleep supply current				0.3	mA
I_{as}	V_a sleep supply current				3	mA
I_c	V_c supply current				1.5	mA
I_r	V_r supply current				0.6	mA
I_a	V_a supply current	I_{Rext}= 3mA			13	mA

Table 3. DC Electrical characteristics (T_j = 25°C) - continued

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{dd}	V_{dd} supply current	sleep or normal condition			5	mA
V_{ref}	Reference Voltage	T_{amb}= 5 to 55°C	4.85	5	5.15	V
I_{refext}	Reference current (external)				7	mA
I_{ccs}	Programmed constant current	$I_{ccs} = \frac{V_{ref}}{2R_{ext}} \cdot 4$		12	13.5	mA
$\Delta I_{ccs}/I_{ccs}$	Constant current regulation	V_a=11V T_{amb} = 5 to 55°C		0.33		%
V_{ampout}	Output voltage of integrated		e (3)		Va-1	V
	amplifier					
V_{cm}	Operating input voltage at pins	V_{ref}= 5V g1=1.2 g2 = 3			7	V
	Vxa and Vxb					
g1	Amp. A1 Voltage gain		1.188	1.2	1.212	
g2	Amp.A2 Voltage gain		2.95	3.02	3.10	
$V_{step-up}$	Driving Voltage of power DMOS			Vc +11		V
A/D CONVERTER						
$V_{A/D\ in}$	A/D input voltage	Selected Channel: CH1 to CH5 Selected Ch=CH0	0 e (3)		Vref Vref	V V
I_{exch}	A/D input current	Input CH1 to CH5 selected or not			±1	µA
OFFSET VOLTAGE GENERATION / DAC						
V_{offset}	Offset Voltage	V_{ref} = 5V	2.5 + e (3)		7.34	V
V_{step}	Voltage increment (1LSB)	V_{ref}= 5V		156		mV
K_{dac}	Voffset/Vref	Any step N ≥ 4			±3	%
A/D CONVERTER TIMINGS						
T_{cscks}	ConvStart set up time		200			ns
T_{csckh}	ConvStart hold time		200			ns
T_{ckout}	Falling edge of clock to data out valid delay	C_{load} ≤ 20pF			200	ns
T_{csz}	ConvStart falling edge to output in Hi-Z delay				200	ns
F_{adck}	Clock frequency				250	KHz
T_{cslow}	Conv. Start low level time		5.6			µs

Table 3. DC Electrical characteristics (T_j = 25°C) - continued

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{acqth}	Theoretical acquisition time	f_{adck}= 250 kHz	32.4			µs
T_{acqpr}	Real acquisition time	f_{adck}= 250 kHz	36			µs
DIGITAL INTERFACE INPUT						
V_{inp}	Schmitt Trigger positive-going Threshold				$2/3V_{dd}$	V
V_{inm}	Schmitt Trigger negative-going Threshold		$1/3V_{dd}$			V
V_{hys}	Schmitt Trigger Hysteresis		0.1	0.3	1	V
I_{in}	Input Current (Vin=0; V_{dd}=5) (4)		50	150	300	µA
CR LATCH TIMINGS						
T_{ls}	Latch set up time		100			ns
T_{lhigh}	Latch high time		100			ns
T_{lconv}	Latch data valid to A/D input valid delay	Selected channel: CH1..CH5 CH0	 4 7			 µs µs
t_{store}	Latching data time		200			ns
Note:	*The control register (driving signals CRdata, CRclock) is accessed with the same timing specifications as the data 16 bit shift register (signals SDI, SDC)*					
SHIFT REGISTER AND LATCH TIMING						
T_a	Set up time		35			ns
T_b	Hold time		35			ns
T_c	Serial clock low time		35			ns
T_d	Serial clock high time		35			ns
T_e	Serial clock period		125			ns
T_f	Latch set up time		100			ns
T_g	Latch data high time		100			ns
T_{set}	NcEn setup time with respect to $\overline{\text{LongPulse}}$ (or $\overline{\text{ShortPulse}}$) Asserted		160			ns
T_{hold}	NcEn hold time with respect to $\overline{\text{LongPulse}}$ (or $\overline{\text{ShortPulse}}$) Asserted		0			ns
T_{lp}	Set-up time from latch to Pulse (short and long)		125			ns
T_{pl}	Time from Pulse deassertion to new data latching		125			ns

Table 3. DC Electrical characteristics (T_j = 25°C) - continued

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OUTPUTS ELECTRICAL CHARACTERISTICS						
I_{out}	Output Current (outputs 0..15)	DC=33%; preheating DC=66%		400		mA
$R_{ds(ON)}$	On Resistance	T_j= 25°C			1.3	Ω
T_{pdr}	Power output Turn on Time	From 50% $\overline{\text{LongPulse}}$ to 90% power output rising edge Load = 30 Ohm in parallel with 1.5nF			160	ns
T_{pd}	Toff delay time	From 50% $\overline{\text{LongPulse}}$ to 90% power output falling edge Load = 30 Ohm in parallel with 1.5nF			100	ns
R_{pon}	Open Nozzle Check		0.5	1	2	kΩ
HEAD ADDRESS SELECTOR OUTPUT						
T_h	UpC/S2, ResC/S1, ChSel, ClkC/S0 and EnIC set-up time with respect to $\overline{\text{EnCh}}$		150			ns
T_k	UpC/S2, ResC/S1, ChSel, ClkC/S0 and EnIC hold time with respect to $\overline{\text{EnCh}}$		50			ns
T_j	UpC/S2 with respect to hold time ClkC/S0		200			ns
T_i	UpC/S2 with respect to setup time ClkC/S0		100			ns
T_m	Enable input to active output delay time				100	ns
T_n	Clock to active output delay time				150	ns
T_o	Disable input to inactive output delay time				100	ns
$f_{clk\text{-}counter}$	Counter Clock Frequency				1	MHz
Clk_{dc}	Clock duty cycle		10		90	%
T_{on}	Address Turn on time	From 50% ClkC/S0 or selector signal to 90% of the address output variation Load: see *Figure 11.*			325	ns
T_{off}	Address Turn off time				325	ns

(1) The three supply voltage are independent inside the specified value;

(2) The Min. value for V_c power line has been verified down to 4V in application lab.; nevertheless the parameters are guaranteed within spec limit of the above DC ELECTRICAL CHARACTERISTICS table.

(3) $e = 2 \cdot V_{step}$

(4) This applies to input pins having an internal pull-up (ENCH, $\overline{\text{LONGPULSE}}$, $\overline{\text{SHORTPULSE}}$)

3.3 Counter Truth Table

EnIC = 1
UpC/S2 = 1
ResC/S1 = 1

Clock Counter	C3	C2	C1	C0
0	0	0	0	0
⎍	0	0	0	1
⎍	0	0	1	1
⎍	0	0	1	0
⎍	0	1	1	0
⎍	0	1	1	1
⎍	0	1	0	1
⎍	0	1	0	0
⎍	1	1	0	0
⎍	1	1	0	1
⎍	1	1	1	1
⎍	1	1	1	0
⎍	1	0	1	0
⎍	1	0	0	0
⎍	0	0	0	0

EnIC = 1
UpC/S2 = 0
ResC/S1 = 1

Clock Counter	C3	C2	C1	C0
0	0	0	0	0
⎍	1	0	0	0
⎍	1	0	1	0
⎍	1	1	1	0
⎍	1	1	1	1
⎍	1	1	0	1
⎍	1	1	0	0
⎍	0	1	0	0
⎍	0	1	0	1
⎍	0	1	1	1
⎍	0	1	1	0
⎍	0	0	1	0
⎍	0	0	1	1
⎍	0	0	0	1
⎍	0	0	0	0

3.4 Decoder Truth Table

OUTPUTS (HS) ACTIVE	C3*	C2*	C1*	C0*
All inactive	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	0	1	0
4	0	1	1	0
5	0	1	1	1
6	0	1	0	1
7	0	1	0	0
8	1	1	0	0
9	1	1	0	1
10	1	1	1	1
11	1	1	1	0
12	1	0	1	0
13	1	0	0	0
All inactive	1	0	0	1
All inactive	1	0	1	1

* C3 = S3, C2 = S2, C1 = S1, C0 = S0, when EnIC = 0

This table is valid for both Channel A and Channel B and when $\overline{\text{EnCh}}$ is set to low level.

4 Print Head Temperature Control Part

4.1 Introduction

For quality printing, it is necessary to know and control the temperature of the print head. Thus, the latter has a built - in aluminium resistor, whose value changes slightly with the temperature. The temperature determination is done by injecting a constant current in the resistor, and measuring the voltage drop across it. Since high - end printers have two heads, it must also be possible to switch quickly the measurement process from one to the other. The function is foreseen to be integrated into the head driver, and is described hereafter.

4.2 Print Head Block Diagram (*Figure 5.*)

At first we have a constant current source, which can be disabled by an external pin ($\overline{\text{OnEnable}}$) or by a control register, described later. The value of the current can be programmed by an external resistor, and is given by:

$$I_{CCS} = \frac{V_{ref} \cdot 4}{2 \cdot R_{ext}}$$

This current is injected either into the resistor of the head A (Ralu. A) or B (Ralu. B), depending of the switch SW3. The resistors are grounded, and the voltage at their << hot >> side (Vx) is re-entered via the pins VxA and VxB. Using separate pins from RxA and RxB permits to be more flexible, and a filter can eventually be added as shown in the drawing.

The voltage Vx is amplified by A1 and A2, and then converted in a digital value. To be compatible with the input range of the A/D converter, it is necessary to subtract an offset voltage Voffset from Vx. Moreover, as the initial value of the aluminum resistor is very imprecise. Voffset must be adjustable; this is done by means of a 5 bit - D/A converter, giving 32 different values. Finally, the voltage at the input of the A/D converter is:

$$V_{CH0} = g1 \cdot g2 \cdot VX - g2 \times V_{OFFSET}$$

or

$$V_{CH0} = g1 \cdot g2 \cdot Ralu \cdot I_{CCS} - g2 \cdot V_{OFFSET};$$

$$V_{OFFSET} = V_{REF}/2 + N \cdot V_{REF}/32 \; N = 0, 1, ...31$$

The reference voltage generator (V_{REF}) is integrated, and used for the current source and both the A/D and D/A converters. In this way, the system performance is independent from the precision of V_{REF}; this one should, however, be stable. Vref is also available on pin #45, and can be used for low consumption purposes. (The external sinked current has to be a DC current).

The system is under control of a 10 bit register, CR. CR is accessed serially and has a transparent latch, which can be used or not (by trying the latch signal CR latch to V_{CC}).

Figure 5. Print Head Block Diagram

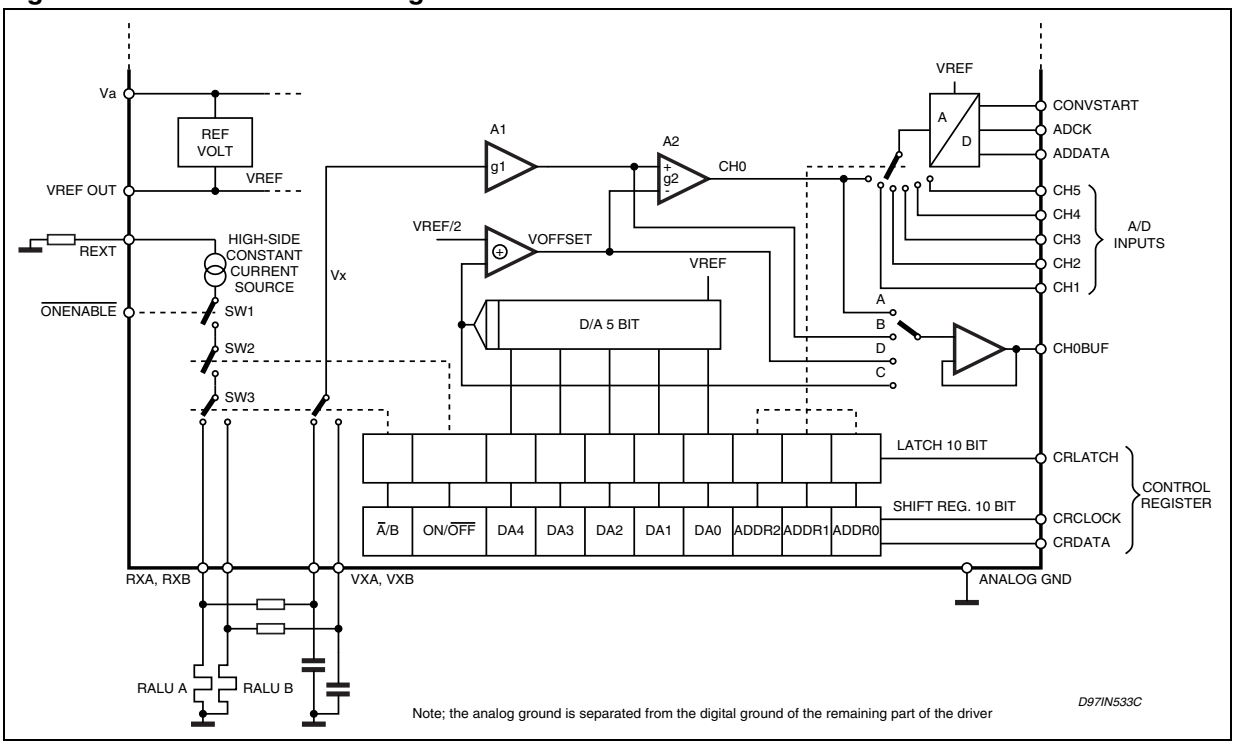
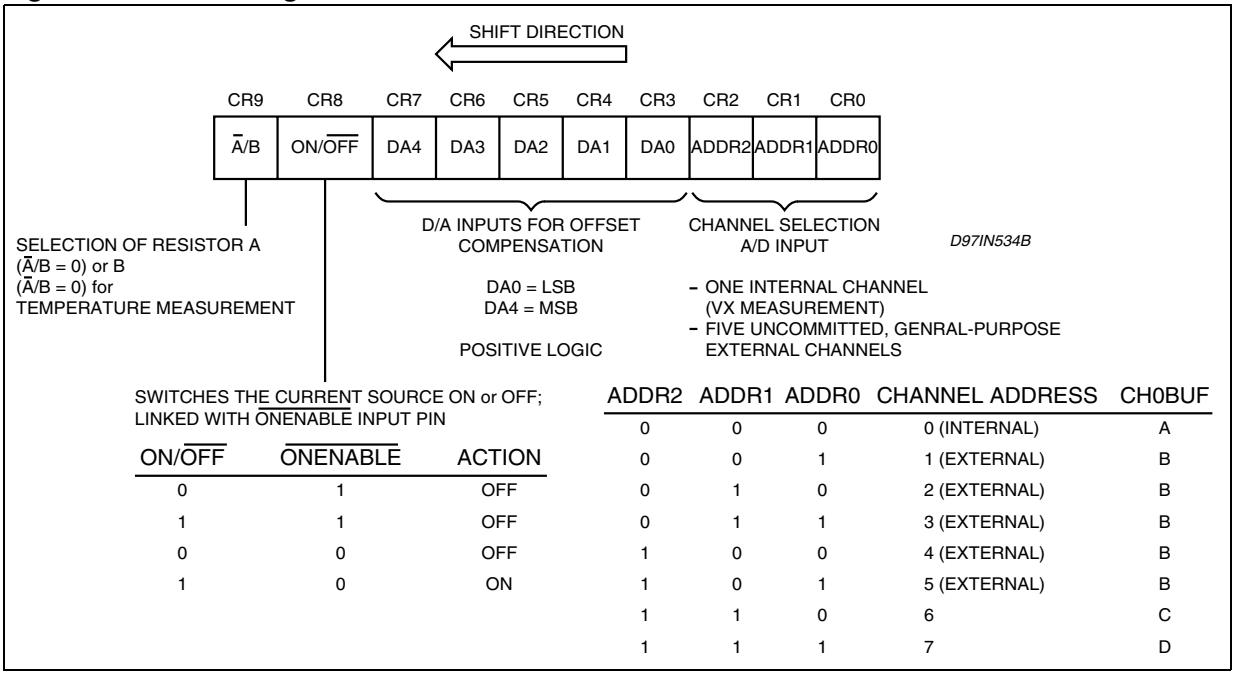


Figure 6. Control Register details.



SWITCHES THE CURRENT SOURCE ON or OFF; LINKED WITH $\overline{\text{ONENABLE}}$ INPUT PIN

ON/$\overline{\text{OFF}}$	$\overline{\text{ONENABLE}}$	ACTION
0	1	OFF
1	1	OFF
0	0	OFF
1	0	ON

ADDR2	ADDR1	ADDR0	CHANNEL ADDRESS	CH0BUF
0	0	0	0 (INTERNAL)	A
0	0	1	1 (EXTERNAL)	B
0	1	0	2 (EXTERNAL)	B
0	1	1	3 (EXTERNAL)	B
1	0	0	4 (EXTERNAL)	B
1	0	1	5 (EXTERNAL)	B
1	1	0	6	C
1	1	1	7	D

Figure 7. CR Latch Timings

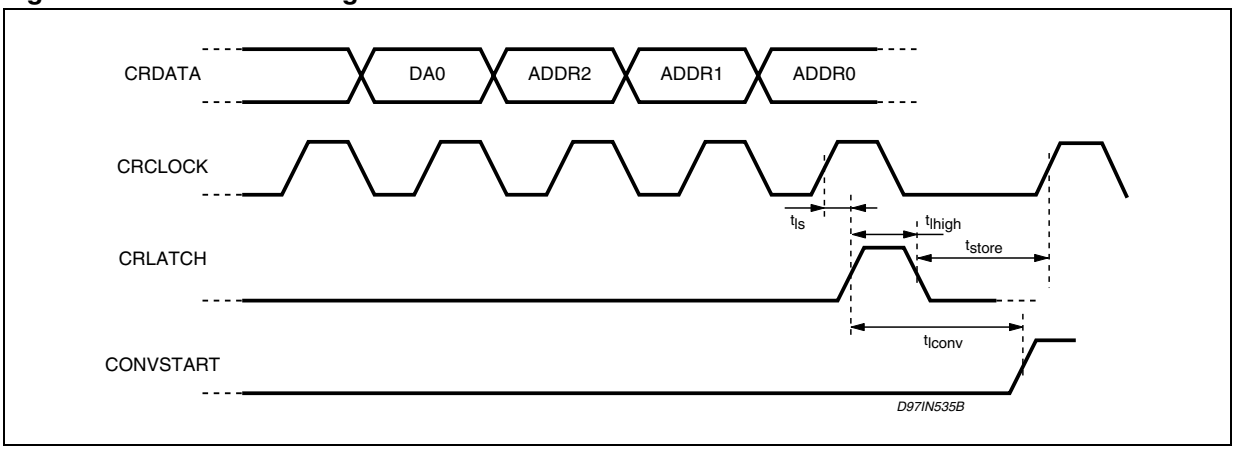


Figure 8. A/D Converter Timings

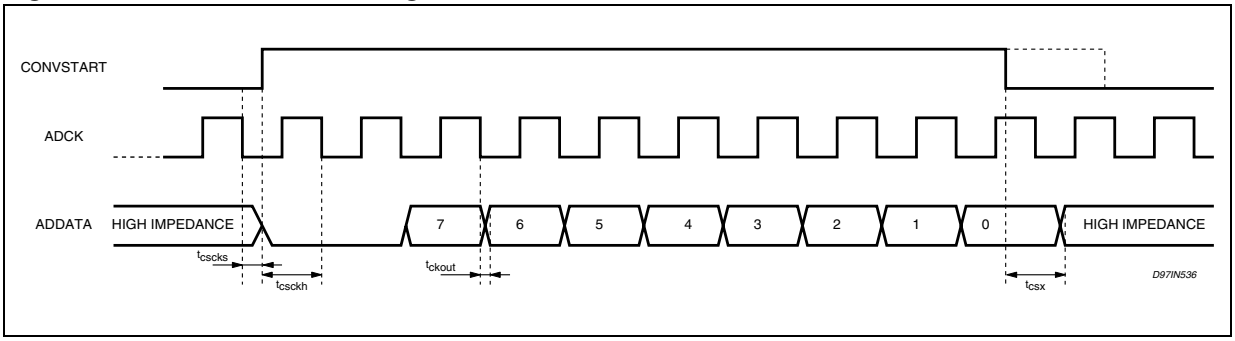
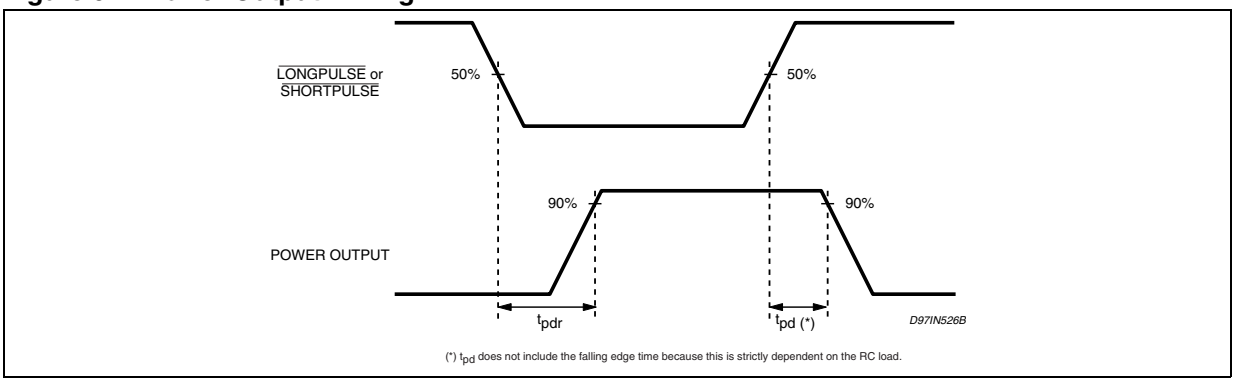


Figure 9. Power Output Timing



(*) t_{pd} does not include the falling edge time because this is strictly dependent on the RC load.

Figure 10. Trigger of Nozzle Check Signal

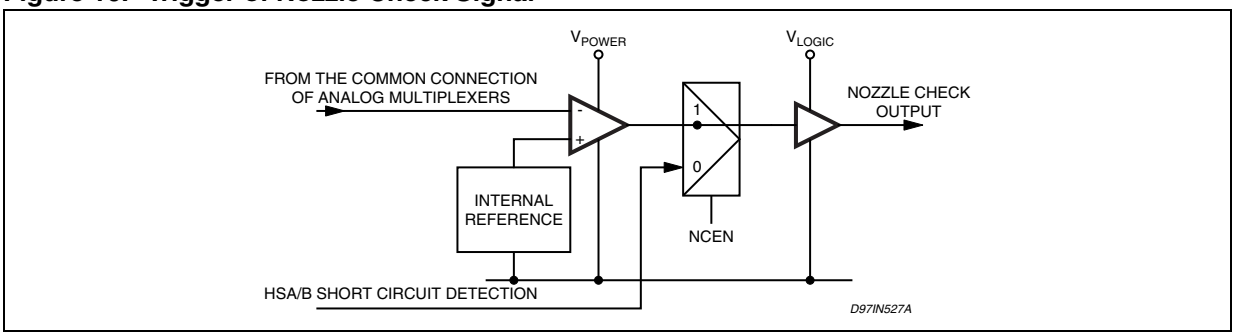


Figure 11. Address load reference

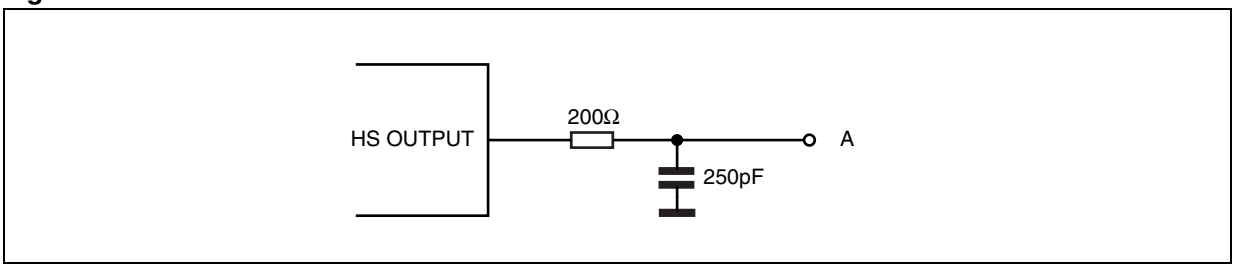


Figure 12. Mode Counter

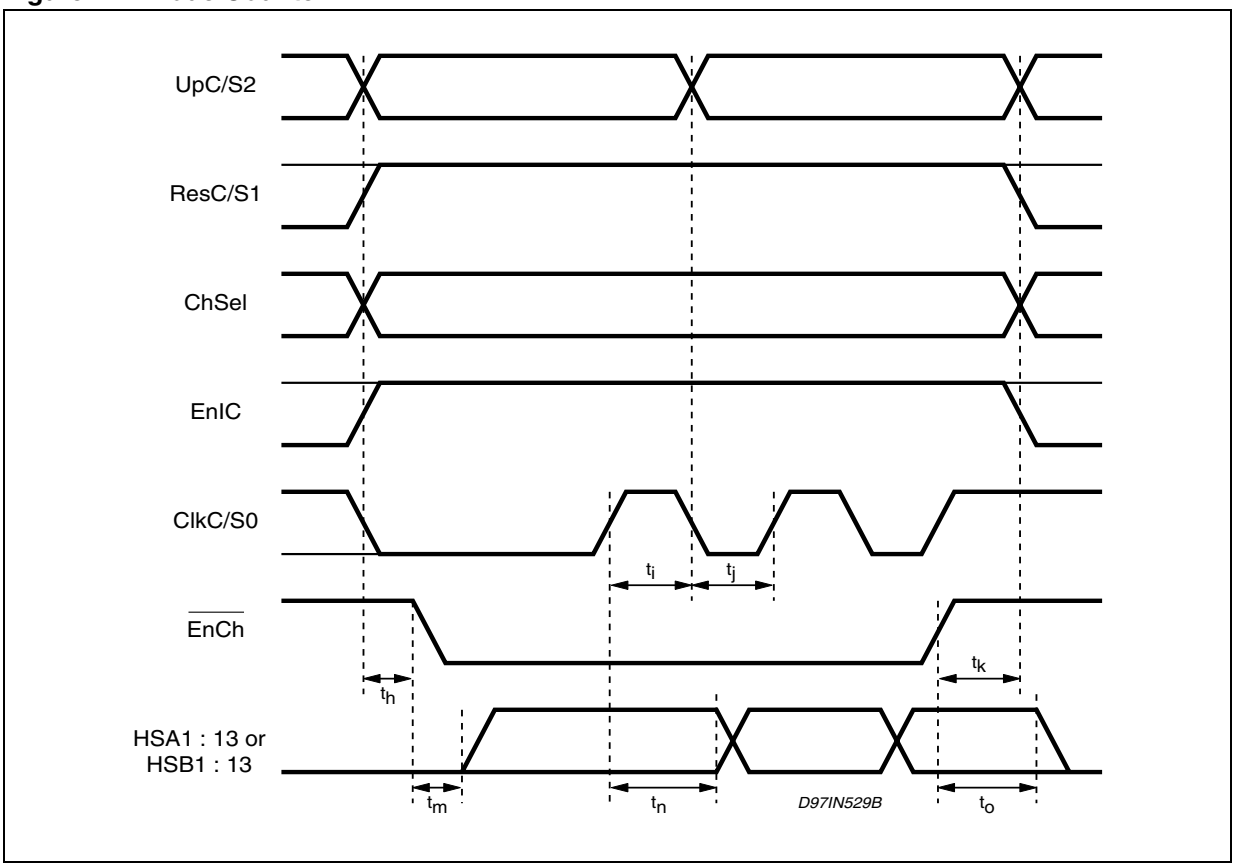


Figure 13. Mode Selelector

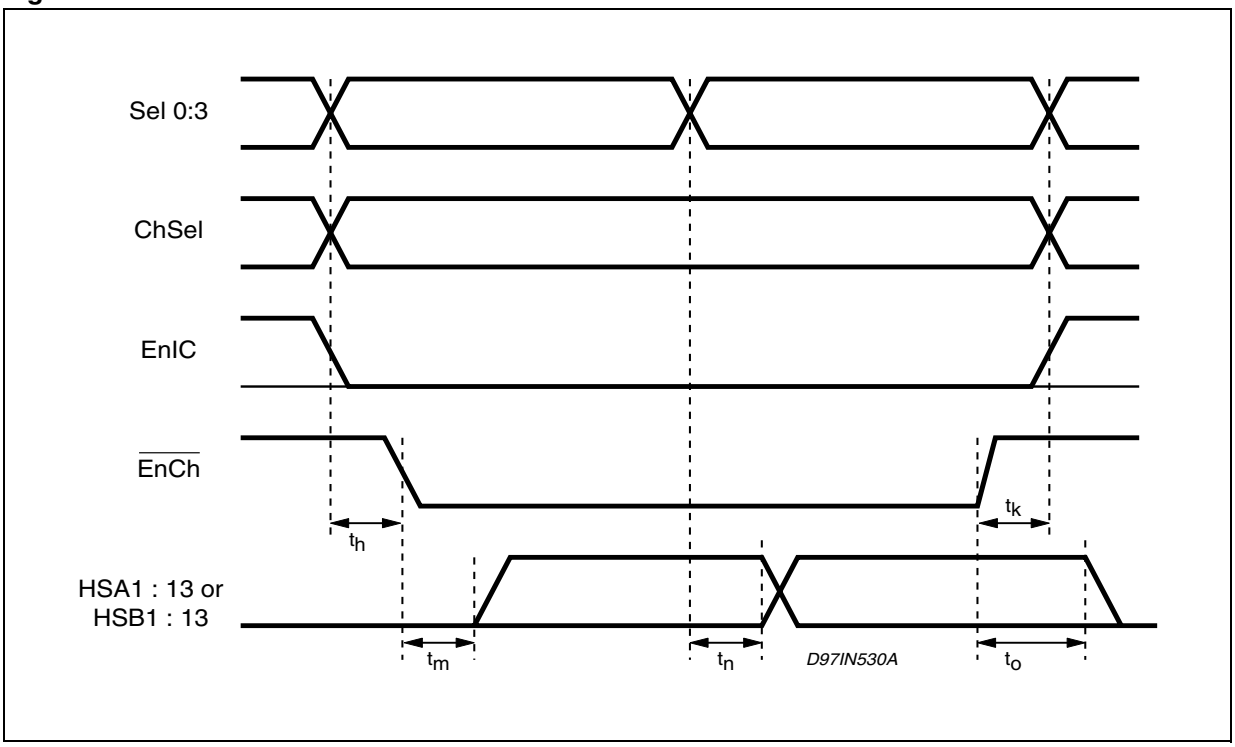


Figure 14. Sequence of Shift Register Data Loading

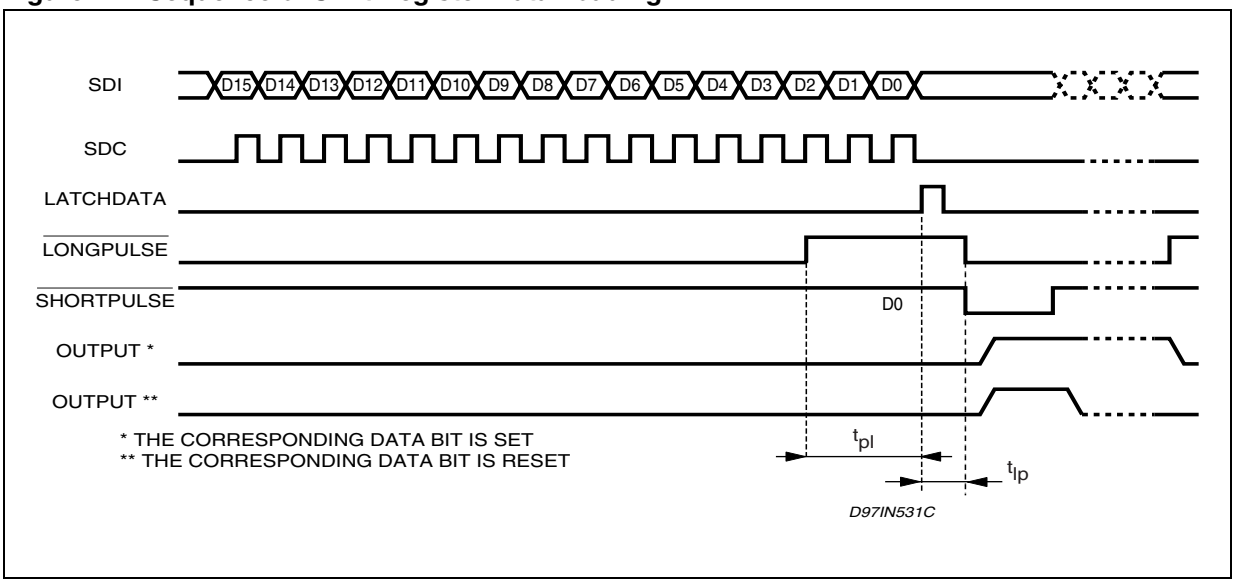
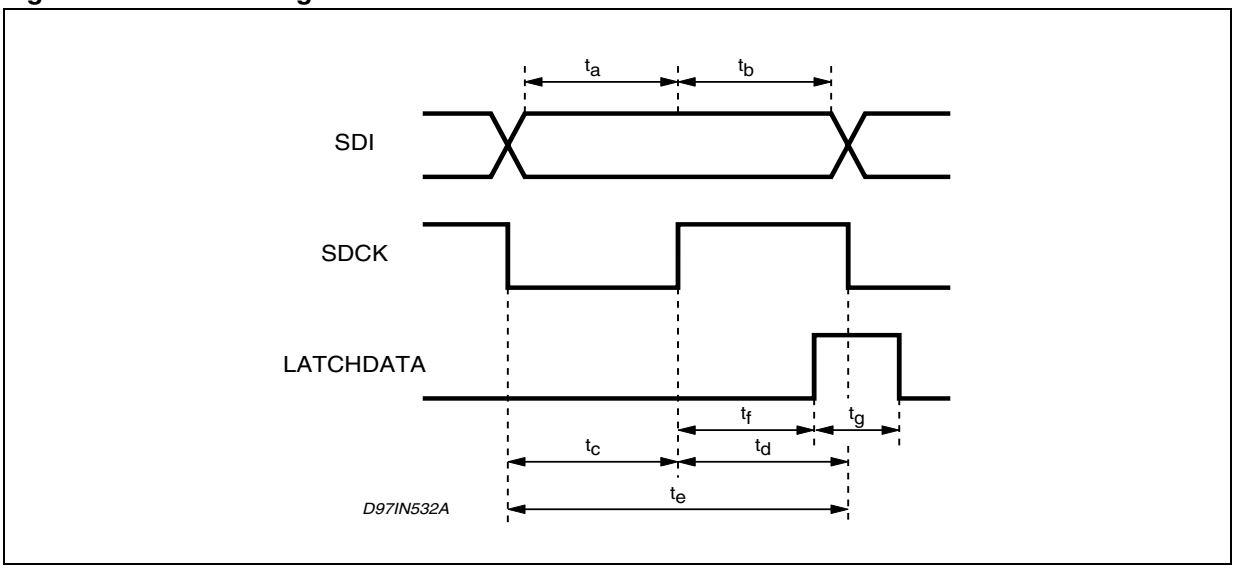


Figure 15. Latch Timing



5 Package information

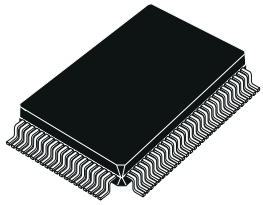
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

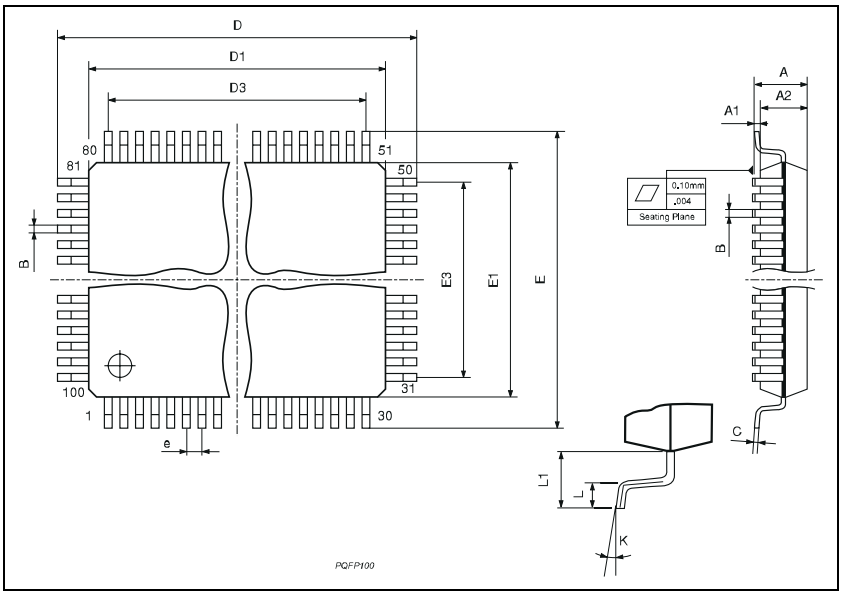
Figure 16. PQFP100 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.22		0.38	0.0087		0.015
C	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.903	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.85			0.742	
e		0.65			0.026	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.35			0.486	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



PQFP100



6 Revision history

Date	Revision	Changes
15-Mar-1999	1	Initial release.
06-Feb-2006	2	Modified Electrical Specification and any Time Diagrams. Modified pin and signal names through out the spec. Modified *Table 1* Pin function pins 83, 84 & 86. Added ESD parameter in the *Table 2* Absolute maximum ratings. Modified *Table 3*: T_{set}, T_{hold} and R_{pon} parameters. Modified *Figure 14*.

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