

Power MOSFET

20 Amps, 30 Volts, N-Channel DPAK

This logic level vertical power MOSFET is a general purpose part that provides the “best of design” available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain-to-source diode has a ideal fast but soft recovery.

Features

- Ultra-Low $R_{DS(on)}$, Single Base, Advanced Technology
- SPICE Parameters Available
- Diode is Characterized for use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperatures
- High Avalanche Energy Specified
- ESD JEDAC rated HBM Class 1, MM Class A, CDM Class 0
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTD20N03L in many Applications

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	30	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	30	Vdc
Gate-to-Source Voltage	V_{GS}	± 20	Vdc
– Continuous	V_{GS}	± 24	
– Non-Repetitive ($t_p \leq 10\text{ ms}$)			
Drain Current	I_D	20	Adc
– Continuous @ $T_A = 25^\circ\text{C}$	I_D	16	
– Continuous @ $T_A = 100^\circ\text{C}$	I_{DM}	60	Apk
– Single Pulse ($t_p \leq 10\text{ }\mu\text{s}$)			
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	74	W
Derate above 25°C		0.6	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1)		1.75	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 30\text{ Vdc}$, $V_{GS} = 5\text{ Vdc}$, $L = 1.0\text{ mH}$, $I_{L(pk)} = 24\text{ A}$, $V_{DS} = 34\text{ Vdc}$)	E_{AS}	288	mJ
Thermal Resistance	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
– Junction-to-Case	$R_{\theta JA}$	100	
– Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

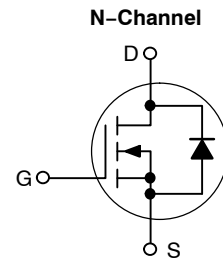
1. When surface mounted to an FR4 board using the minimum recommended pad size and repetitive rating; pulse width limited by maximum junction temperature.



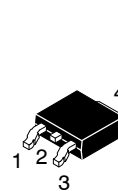
ON Semiconductor®

<http://onsemi.com>

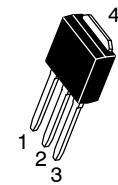
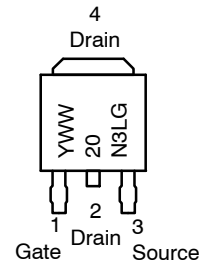
20 A, 30 V, $R_{DS(on)} = 27\text{ m}\Omega$



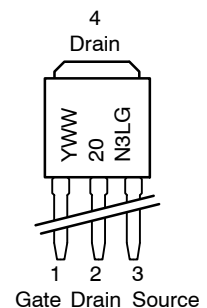
MARKING DIAGRAMS



**DPAK
CASE 369C
STYLE 2**



**DPAK-3
CASE 369D
STYLE 2**



20N3L = Device Code
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NTD20N03L27

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 2) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	30 –	– 43	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 30 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 30 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	10 100	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage (Note 2) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.6 5.0	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 2) (V _{GS} = 4.0 Vdc, I _D = 10 Adc) (V _{GS} = 5.0 Vdc, I _D = 10 Adc)	R _{DS(on)}	– –	28 23	31 27	mΩ
Static Drain-to-Source On-Voltage (Note 2) (V _{GS} = 5.0 Vdc, I _D = 20 Adc) (V _{GS} = 5.0 Vdc, I _D = 10 Adc, T _J = 150°C)	V _{DS(on)}	– –	0.48 0.40	0.54 –	Vdc
Forward Transconductance (Note 2) (V _{DS} = 5.0 Vdc, I _D = 10 Adc)	g _{FS}	–	21	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	1005	1260	pF
Output Capacitance		C _{oss}	–	271	420	
Transfer Capacitance		C _{rss}	–	87	112	

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	(V _{DD} = 20 Vdc, I _D = 20 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω) (Note 2)	t _{d(on)}	–	17	25	ns
Rise Time		t _r	–	137	160	
Turn-Off Delay Time		t _{d(off)}	–	38	45	
Fall Time		t _f	–	31	40	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 15 Adc, V _{GS} = 10 Vdc) (Note 2)	Q _T	–	13.8	18.9	nC
		Q ₁	–	2.8	–	
		Q ₂	–	6.6	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 20 Adc, V _{GS} = 0 Vdc) (Note 2) (I _S = 20 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	– –	1.0 0.9	1.15 –	Vdc
Reverse Recovery Time	(I _S = 15 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs) (Note 2)	t _{rr}	–	23	–	ns
		t _a	–	13	–	
		t _b	–	10	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.017	–	μC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

ORDERING INFORMATION

Device	Package	Shipping†
NTD20N03L27G	DPAK (Pb-Free)	75 Units/Rail
NTD20N03L27-1G	DPAK-3 (Pb-Free)	75 Units/Rail
NTD20N03L27T4G	DPAK (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

查询"NTD20N03L27-D"供应商

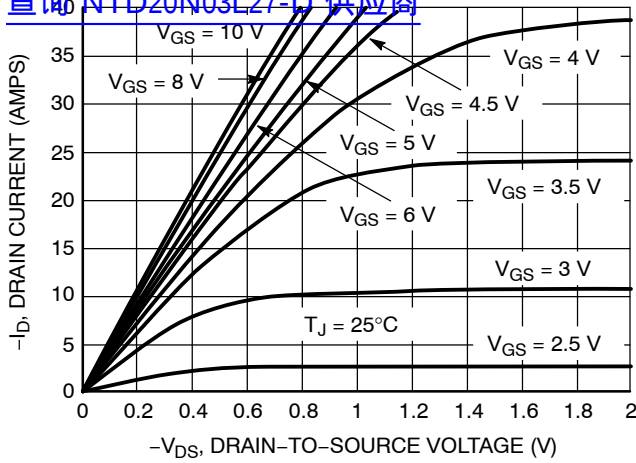


Figure 1. On-Region Characteristics

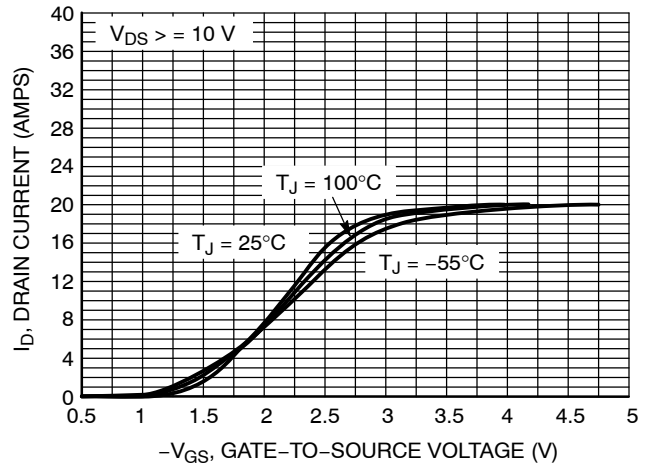


Figure 2. Transfer Characteristics

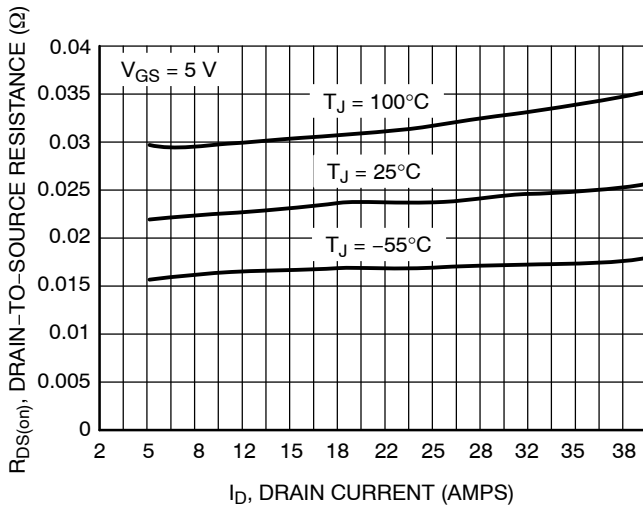


Figure 3. On-Resistance vs. Drain Current and Temperature

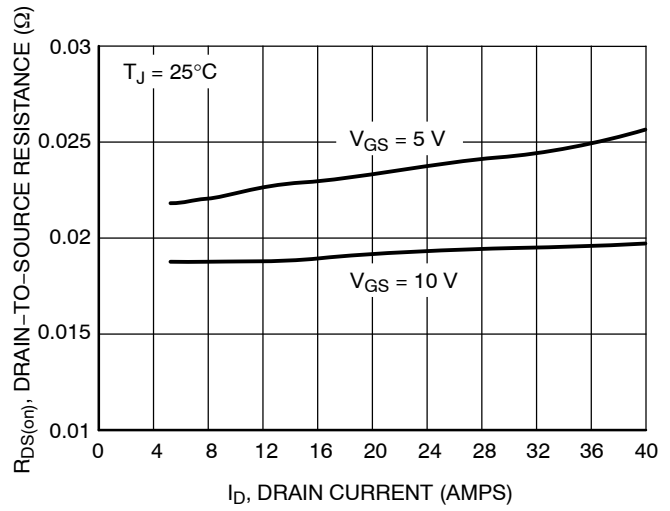


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

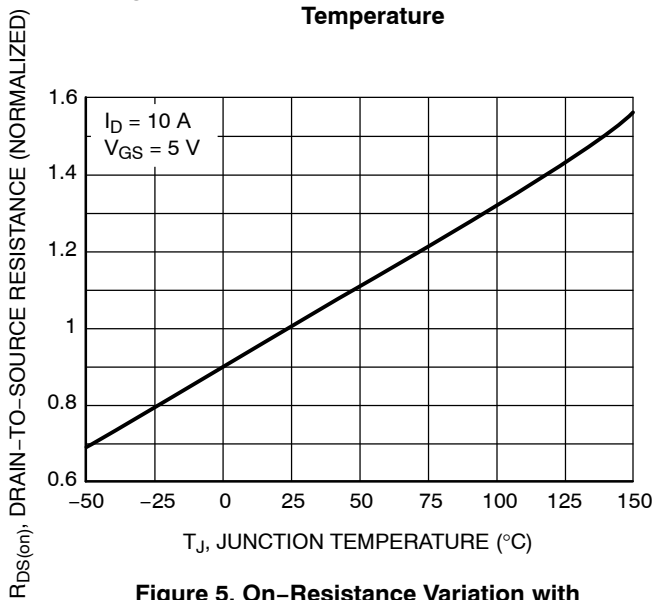


Figure 5. On-Resistance Variation with Temperature

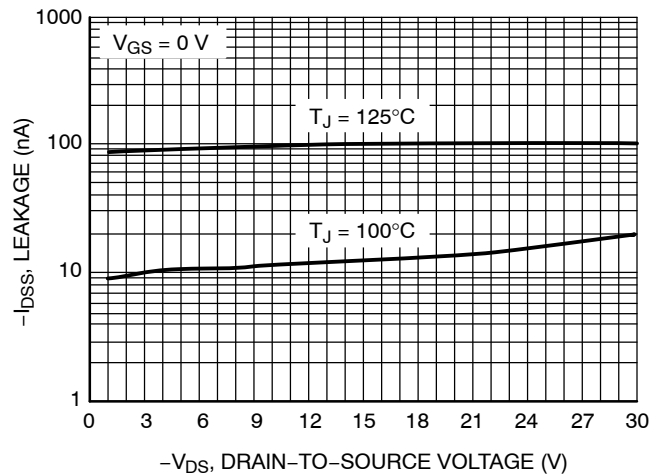


Figure 6. Drain-to-Source Leakage Current vs. Voltage

查询"NTD20N03L27-D"供应商

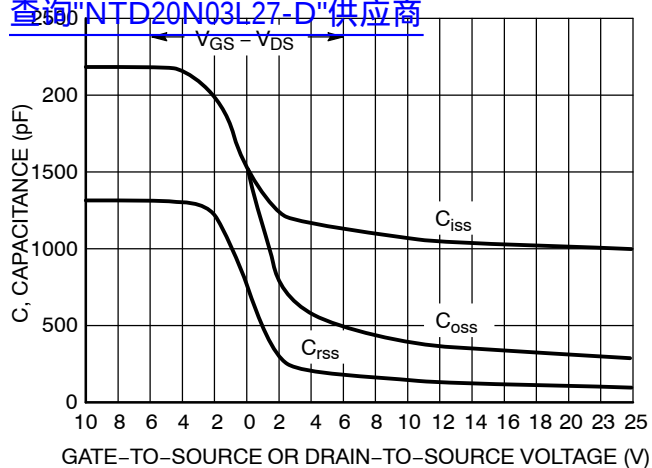


Figure 7. Capacitance Variation

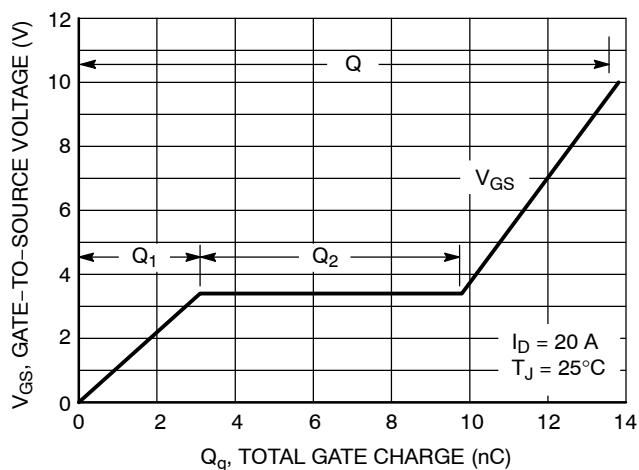


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

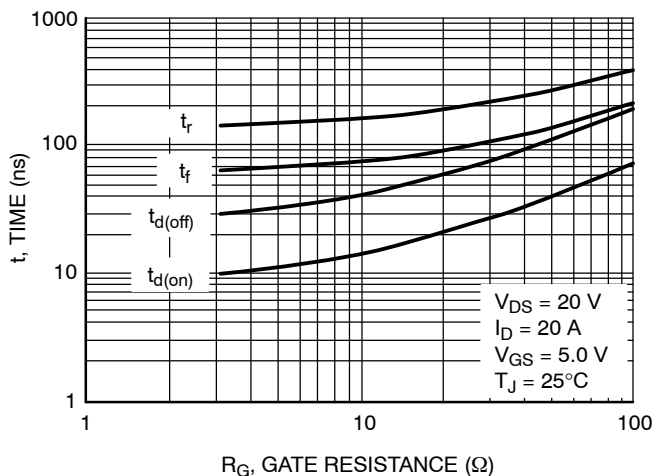


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

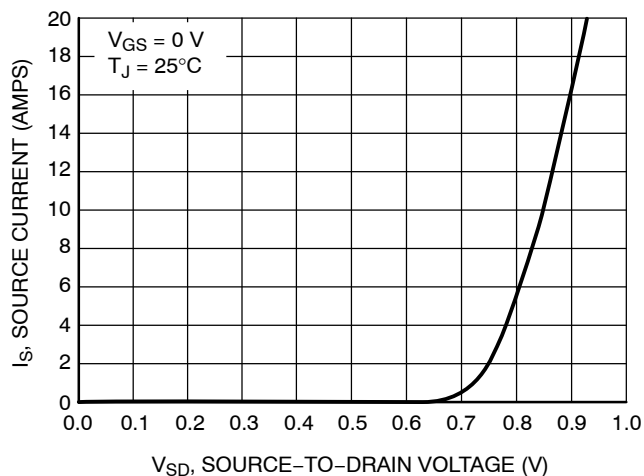


Figure 10. Diode Forward Voltage vs. Current

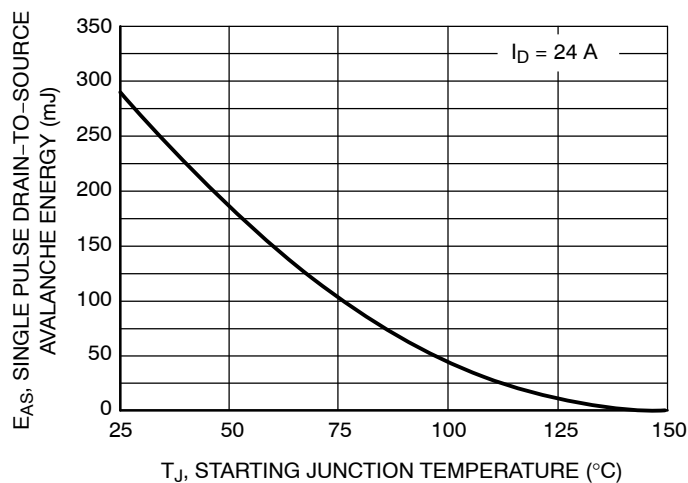


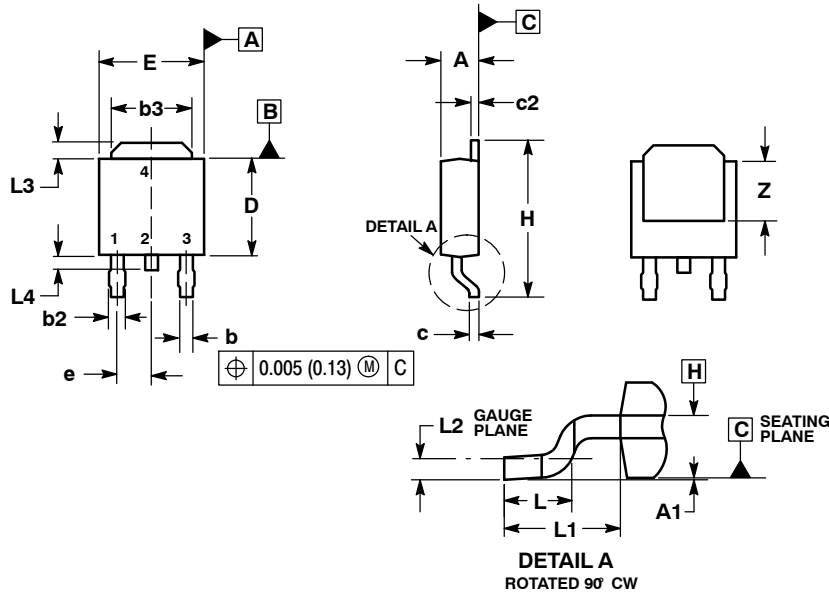
Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

NTD20N03L27

[查询"NTD20N03L27-D"供应商](#)

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C-01 ISSUE D

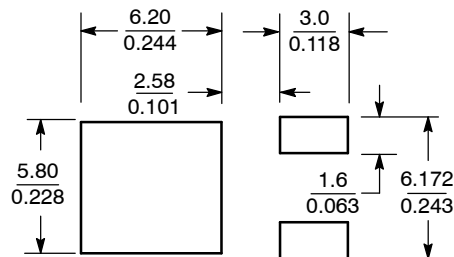


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}} \right)$

STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

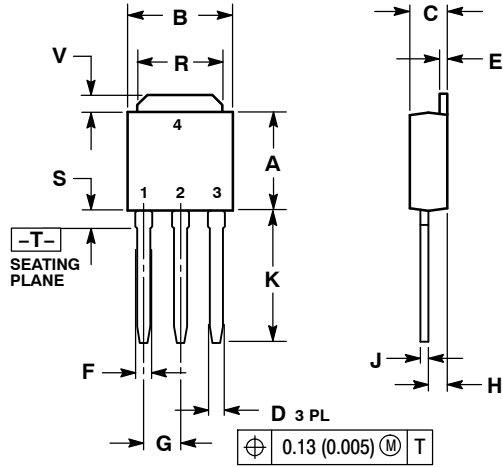
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD20N03L27

查询"NTD20N03L27-D"供应商

PACKAGE DIMENSIONS

DPAK-3
CASE 369D-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

NTD20N03L27/D/D