

### FEATURES

**Ultralow noise: 2.8 nV/ $\sqrt{\text{Hz}}$  at 1 kHz typical**  
**Ultralow distortion: 0.0002% typical**  
**Low supply current: 1.8 mA per amplifier typical**  
**Offset voltage: 1 mV maximum**  
**Bandwidth: 6.5 MHz typical**  
**Slew rate: 12 V/ $\mu\text{s}$  typical**  
**Unity-gain stable**  
**Extended industrial temperature range**  
**SOIC package**

### APPLICATIONS

**Precision instrumentation**  
**Professional audio**  
**Active filters**  
**Low noise amplifier front end**  
**Integrators**

### GENERAL DESCRIPTION

The ADA4075-2 is a dual, high performance, low noise operational amplifier combining excellent dc and ac characteristics on the Analog Devices, Inc., *iPolar*<sup>®</sup> process. The *iPolar* process is an advanced bipolar technology implementing vertical junction isolation with lateral trench isolation. This allows for low noise performance amplifiers in smaller die size at faster speed and lower power. Its high slew rate, low distortion, and ultralow noise make the ADA4075-2 ideal for high fidelity audio and high performance instrumentation applications. It is also especially useful for lower power demands, small enclosures, and high density applications. The ADA4075-2 is specified for the temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and is available in a standard SOIC package.

### PIN CONFIGURATION

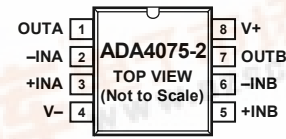


Figure 1. 8-Lead SOIC

Table 1. Low Noise Precision Op Amps

Supply	44 V	36 V	12 V to 16 V	5 V
Single	OP27	AD8671 AD8675 AD797	AD8665 OP162	AD8605 AD8655 AD8691
Dual	OP275	AD8672 AD8676 AD8599	AD8666 OP262	AD8606 AD8656 AD8692
Quad		ADA4004-4 AD8674	AD8668 OP462	AD8608 AD8694

#### Rev. 0

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## REVISION HISTORY

10/08—Revision 0: Initial Version

## SPECIFICATIONS

$V_{SY} = \pm 15\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.2	1	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		30	100	nA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	50	nA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -12.5\text{ V to }+12.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	118		dB
Large-Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = -11\text{ V to }+11\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	106			dB
		$R_L = 600\ \Omega$ , $V_O = -10\text{ V to }+10\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	114	117		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	108			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				$\mu\text{V}/^\circ\text{C}$
Input Resistance	$R_{IN}$			40		M $\Omega$
Input Capacitance, Differential Mode	$C_{INDM}$			2.4		pF
Input Capacitance, Common Mode	$C_{INCM}$			2.1		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	12.8	13		V
		$R_L = 600\ \Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	12.5			V
		$R_L = 600\ \Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	12.4	12.8		V
		$V_{SY} = \pm 18\text{ V}$ , $R_L = 600\ \Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	12			V
		$V_{SY} = \pm 18\text{ V}$ , $R_L = 600\ \Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	15.4	15.8		V
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-14	-13.6	V
		$R_L = 600\ \Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			-13	V
		$R_L = 600\ \Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-13.6	-13	V
		$V_{SY} = \pm 18\text{ V}$ , $R_L = 600\ \Omega$ to GND $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-16.6	-16	V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			-15.5	V
Short-Circuit Current	$I_{SC}$			40		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 100\text{ kHz}$ , $A_V = 1$		0.3		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 4.5\text{ V to } \pm 18\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	106	110		dB
Supply Current per Amplifier	$I_{SY}$	$V_{SY} = \pm 4.5\text{ V to } \pm 18\text{ V}$ , $I_O = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	1.8	2.25	dB
					3.35	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ , $A_V = 1$		12		V/ $\mu\text{s}$
Settling Time	$t_s$	To 0.01%, $V_{IN} = 10\text{ V step}$ , $R_L = 1\text{ k}\Omega$		3		$\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 1\text{ M}\Omega$ , $C_L = 35\text{ pF}$ , $A_V = 1$		6.5		MHz
Phase Margin	$\Phi_M$	$R_L = 1\text{ M}\Omega$ , $C_L = 35\text{ pF}$ , $A_V = 1$		60		Degrees
<b>THD + NOISE</b>						
Total Harmonic Distortion and Noise	THD + N	$R_L = 2\text{ k}\Omega$ , $A_V = 1$ , $V_{IN} = 3\text{ V rms}$ , $f = 20\text{ Hz to } 20\text{ kHz}$		0.0002		%
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ , p-p	$f = 0.1\text{ Hz to } 10\text{ Hz}$		60		nV p-p
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		2.8		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		1.2		pA/ $\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±20 V
Input Voltage	±V <sub>SY</sub>
Input Current <sup>1</sup>	±10 mA
Differential Input Voltage	±1 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

<sup>1</sup>The input pins have clamp diodes to the power supply pins.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 2-layer board.

Table 3. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOIC	158	43	°C/W

## POWER SEQUENCING

The op amp supplies must be established simultaneously with, or before, any input signals are applied. If this is not possible, the input current must be limited to 10 mA.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

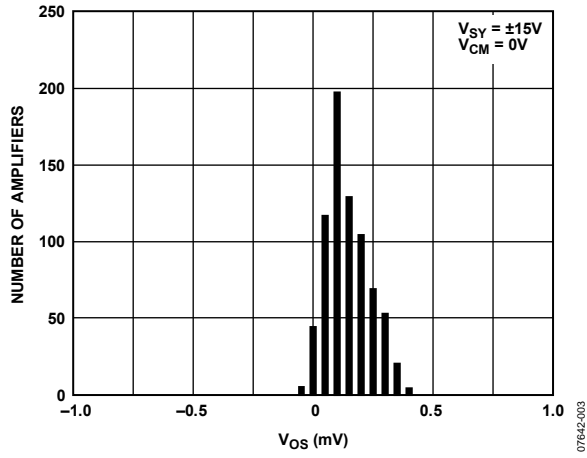


Figure 2. Input Offset Voltage Distribution

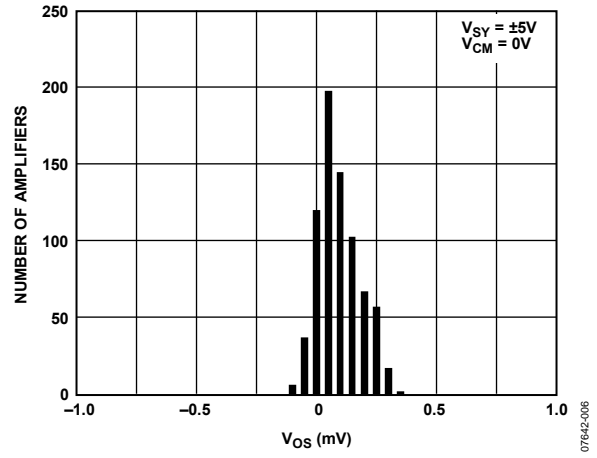


Figure 5. Input Offset Voltage Distribution

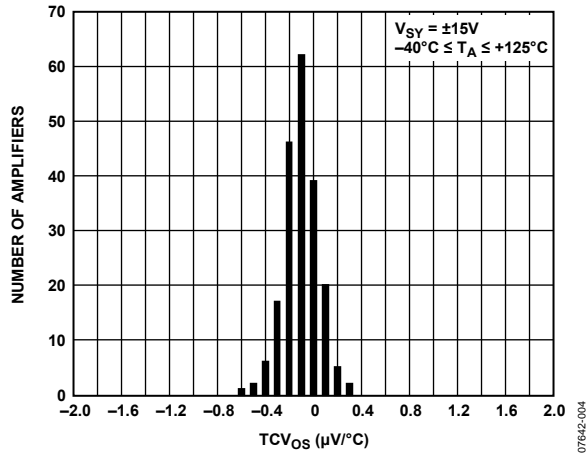


Figure 3. Input Offset Voltage Drift Distribution

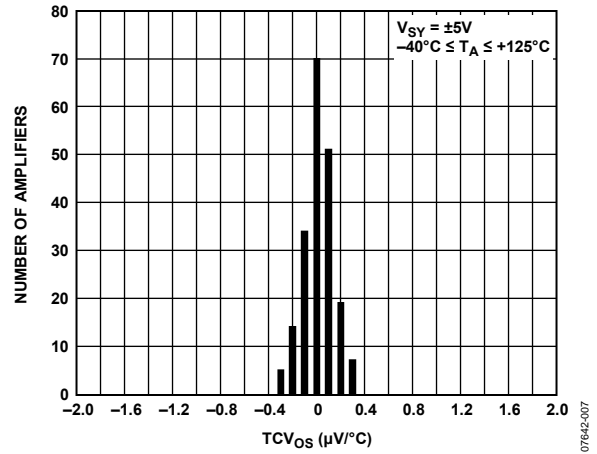


Figure 6. Input Offset Voltage Drift Distribution

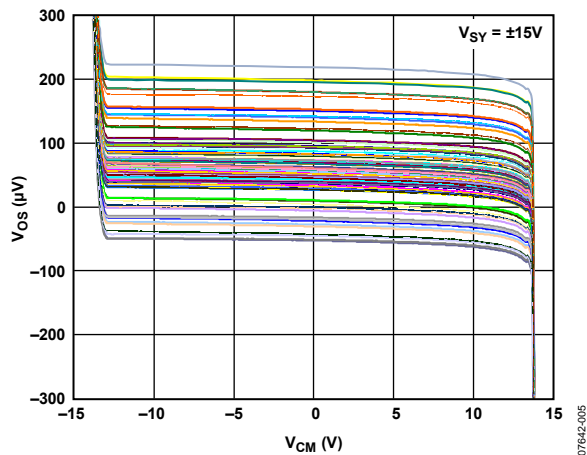


Figure 4. Input Offset Voltage vs. Common-Mode Voltage

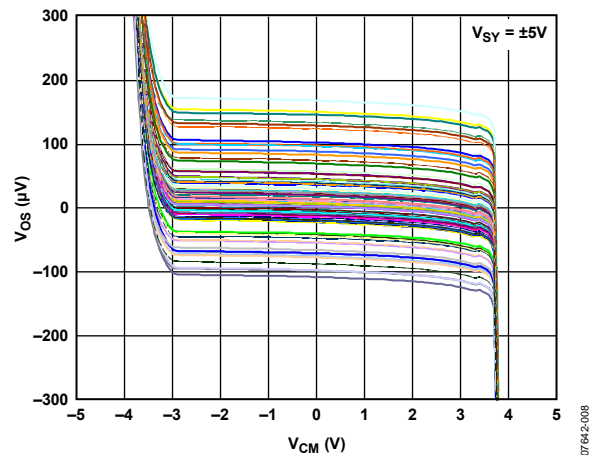


Figure 7. Input Offset Voltage vs. Common-Mode Voltage

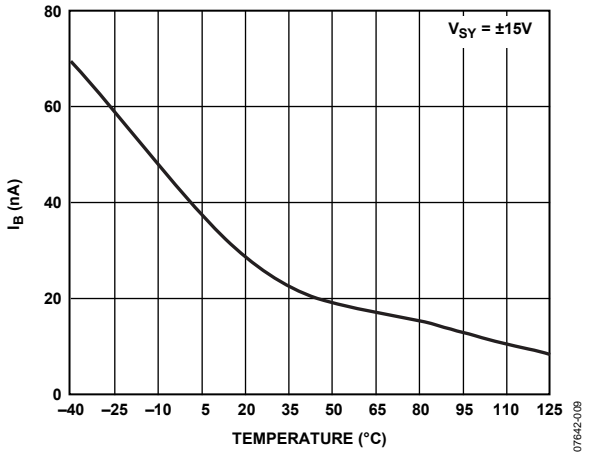


Figure 8. Input Bias Current vs. Temperature

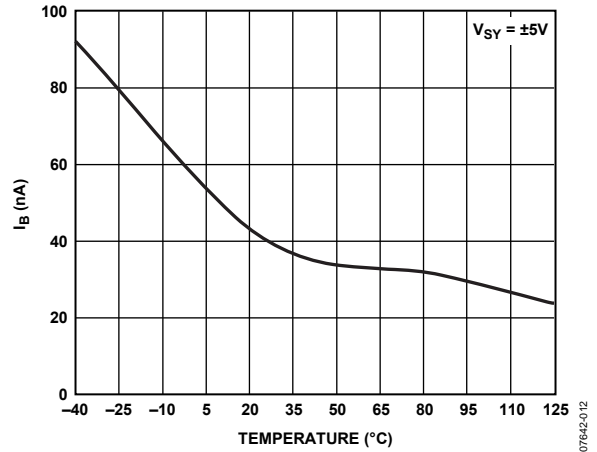


Figure 11. Input Bias Current vs. Temperature

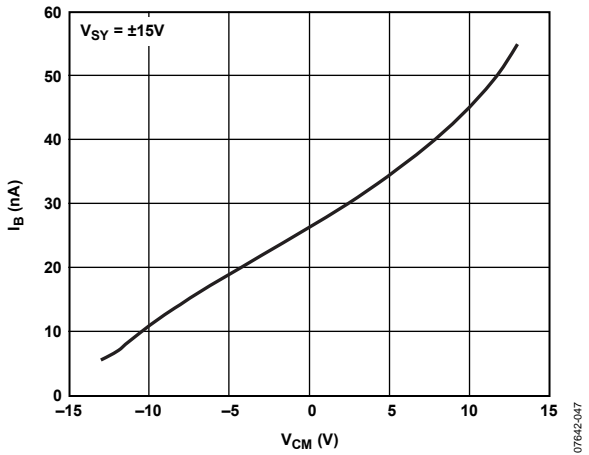


Figure 9. Input Bias Current vs. Input Common-Mode Voltage

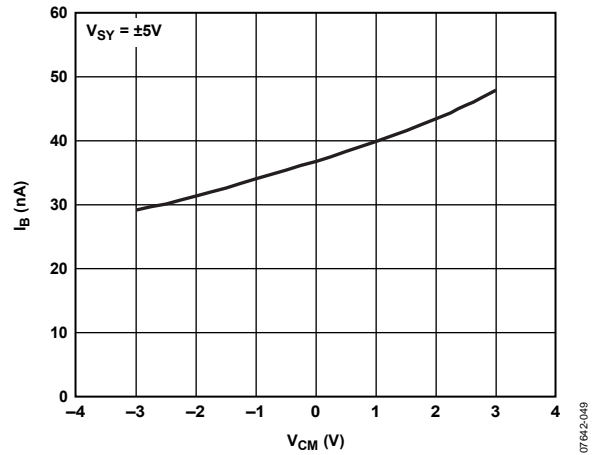


Figure 12. Input Bias Current vs. Input Common-Mode Voltage

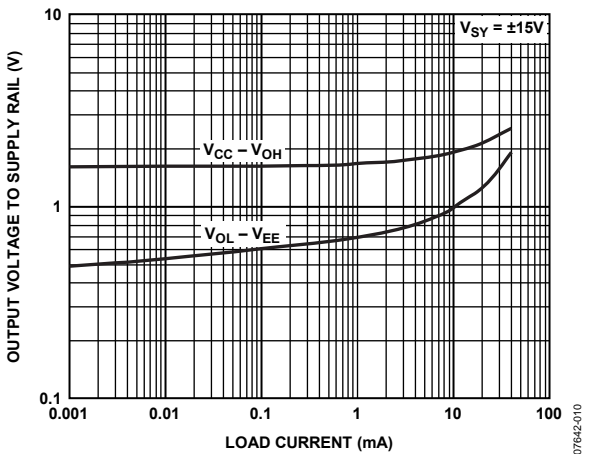


Figure 10. Output Voltage to Supply Rail vs. Load Current

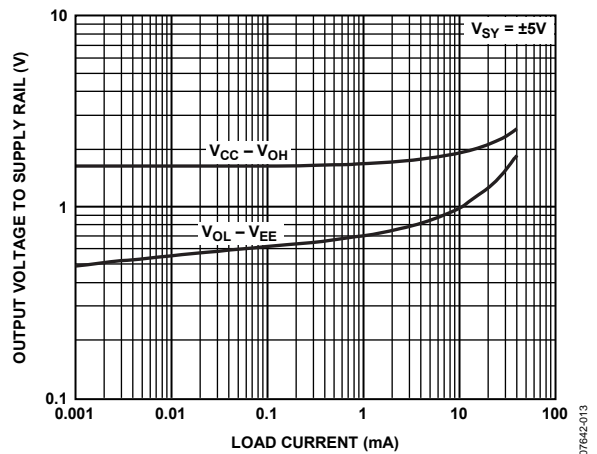


Figure 13. Output Voltage to Supply Rail vs. Load Current

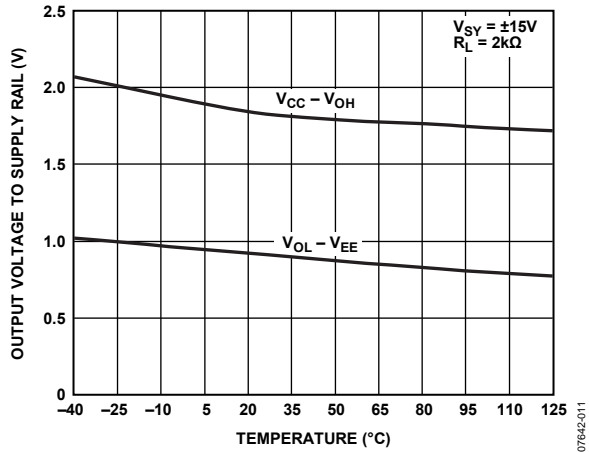


Figure 14. Output Voltage to Supply Rail vs. Temperature

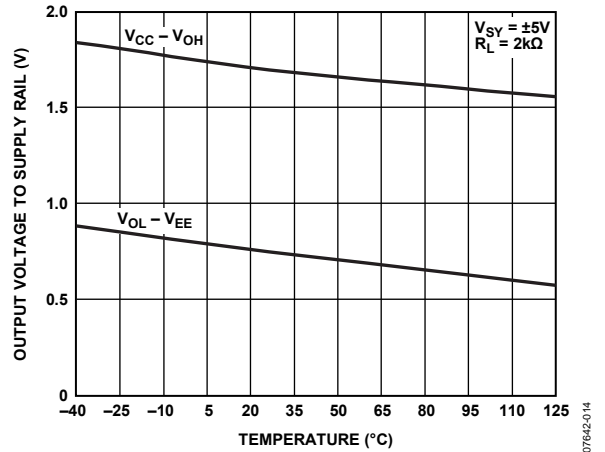


Figure 17. Output Voltage to Supply Rail vs. Temperature

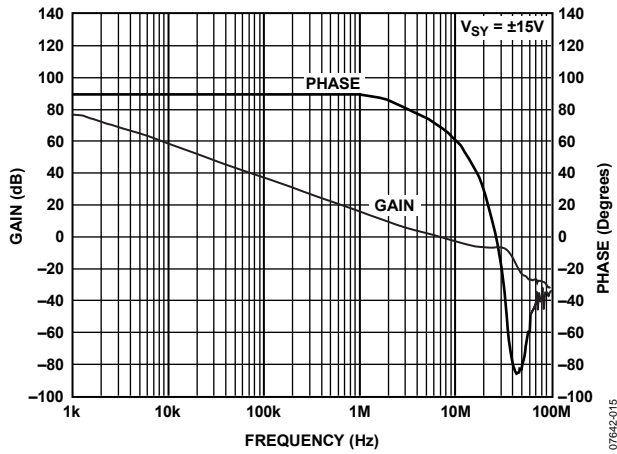


Figure 15. Open-Loop Gain and Phase vs. Frequency

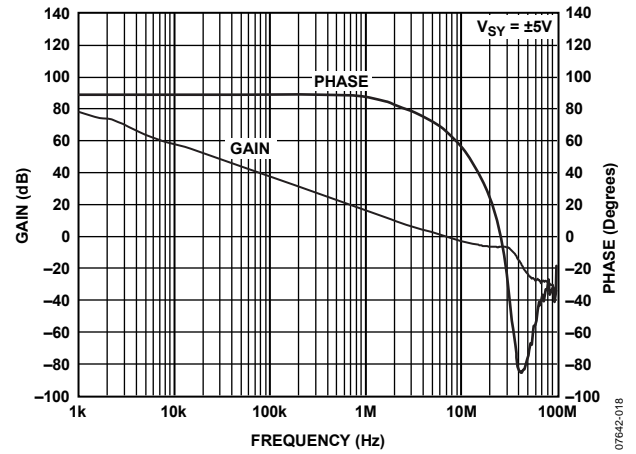


Figure 18. Open-Loop Gain and Phase vs. Frequency

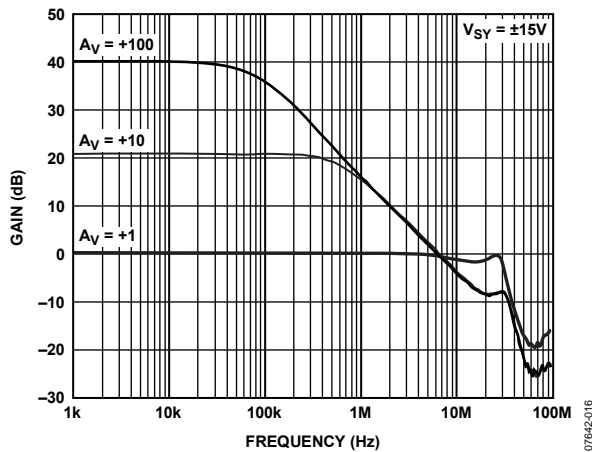


Figure 16. Closed-Loop Gain vs. Frequency

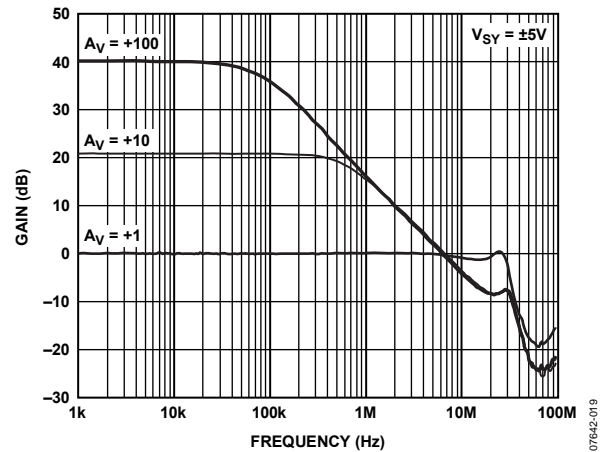


Figure 19. Closed-Loop Gain vs. Frequency

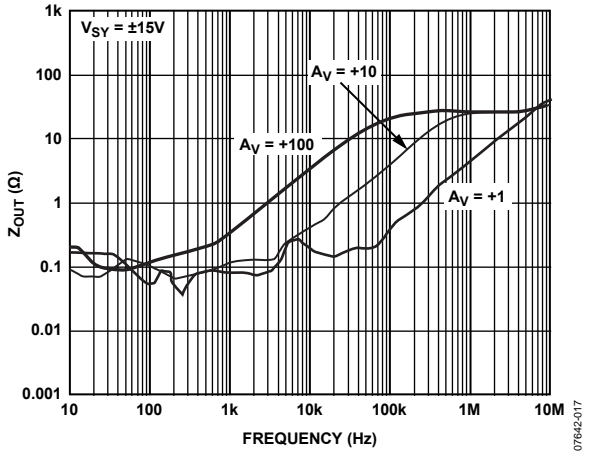


Figure 20. Output Impedance vs. Frequency

07642-017

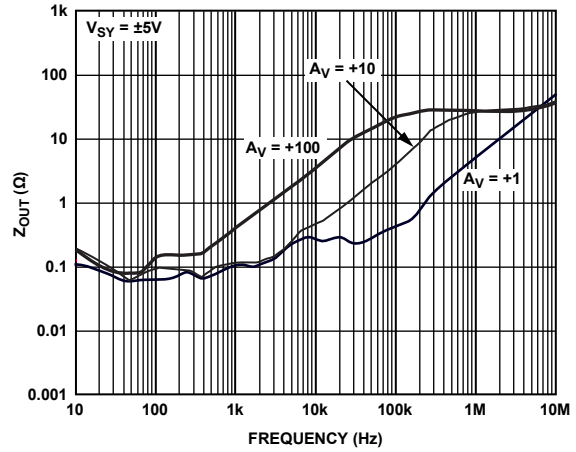


Figure 23. Output Impedance vs. Frequency

07642-020

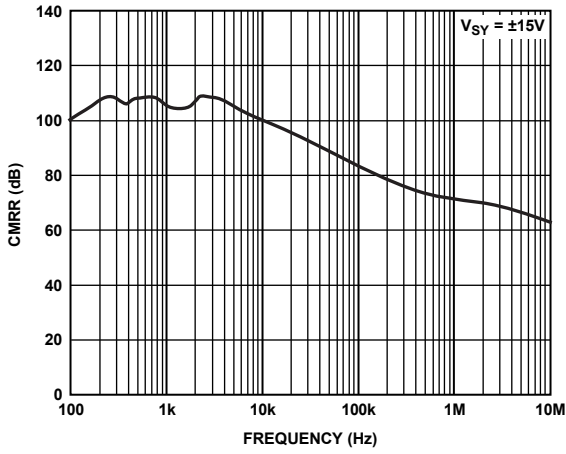


Figure 21. CMRR vs. Frequency

07642-021

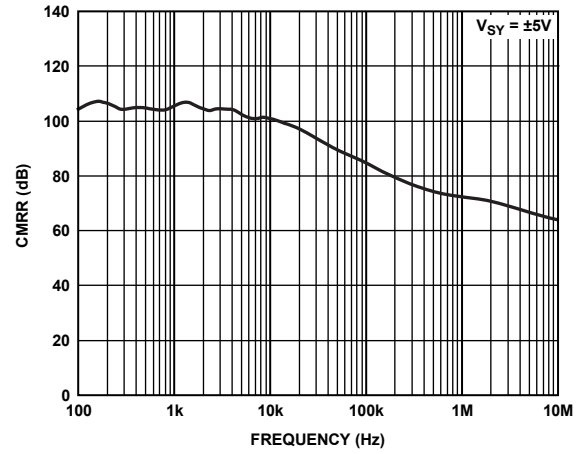


Figure 24. CMRR vs. Frequency

07642-024

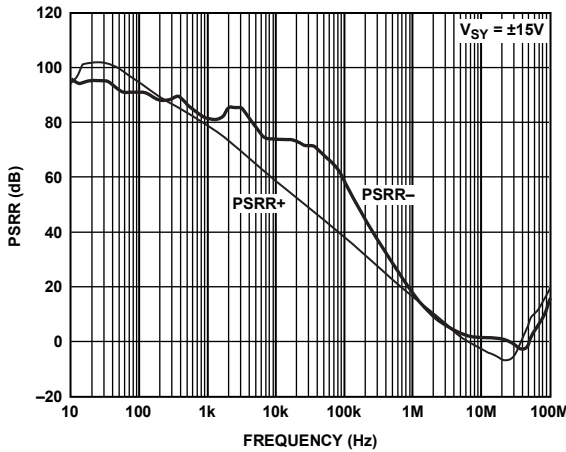


Figure 22. PSRR vs. Frequency

07642-022

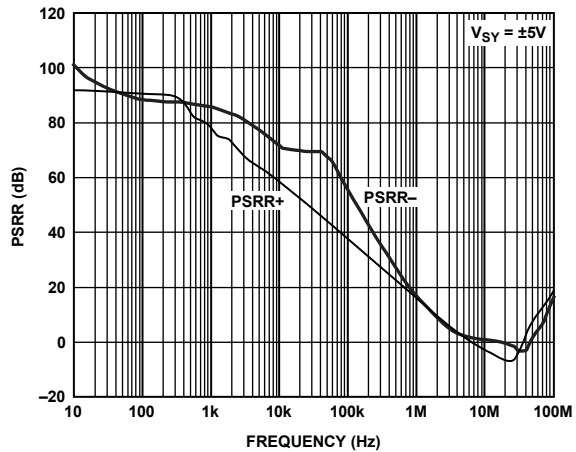


Figure 25. PSRR vs. Frequency

07642-025



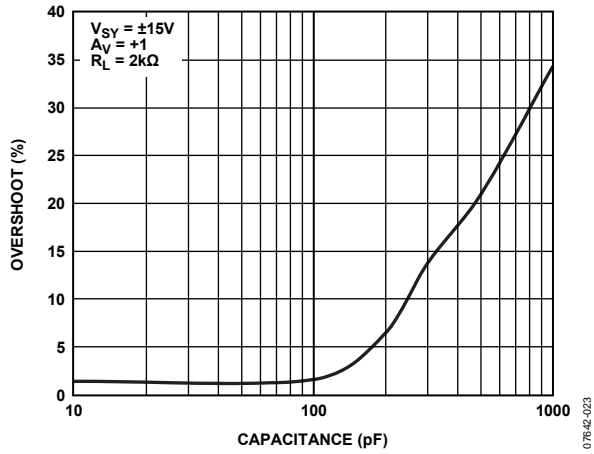


Figure 26. Small-Signal Overshoot vs. Load Capacitance

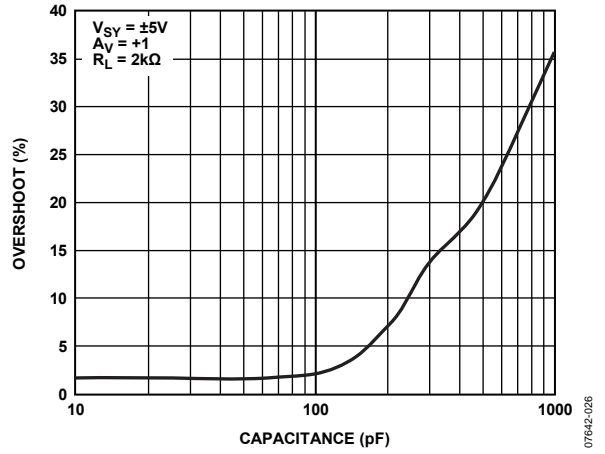


Figure 29. Small-Signal Overshoot vs. Load Capacitance

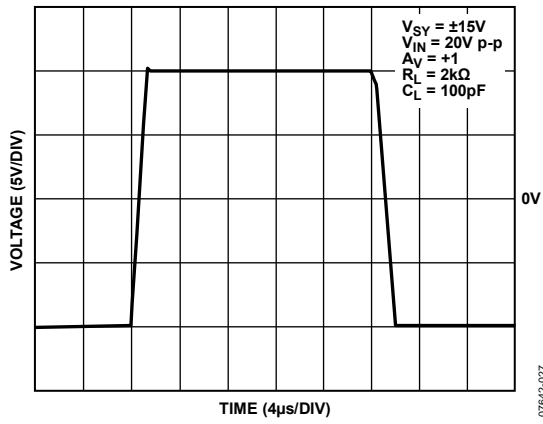


Figure 27. Large-Signal Transient Response

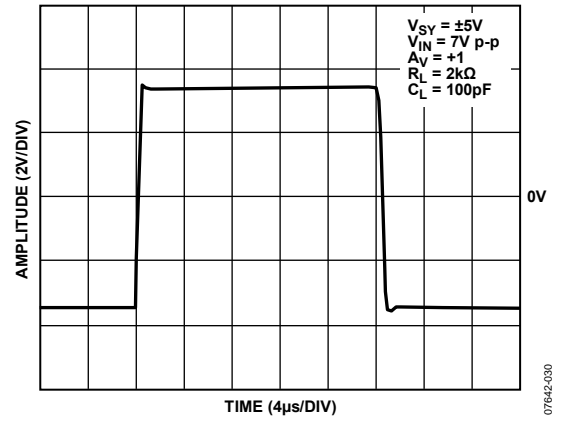


Figure 30. Large-Signal Transient Response

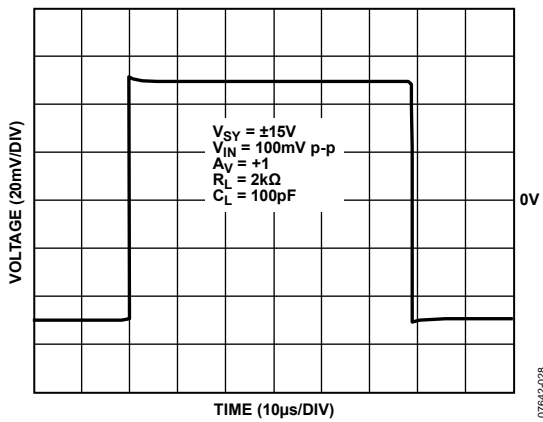


Figure 28. Small-Signal Transient Response

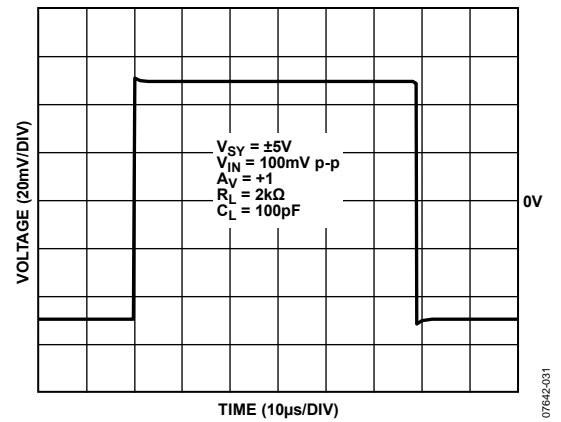


Figure 31. Small-Signal Transient Response

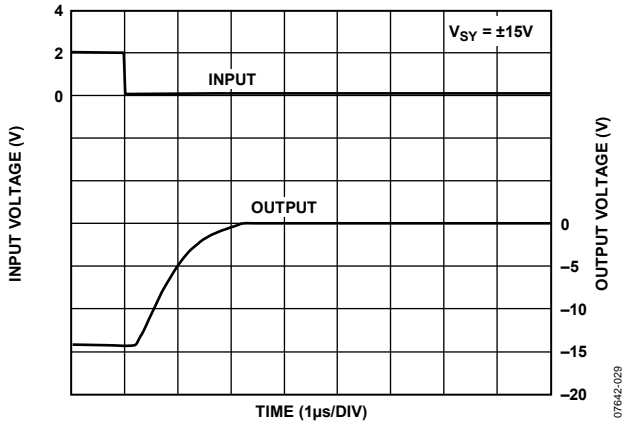


Figure 32. Negative Overload Recovery

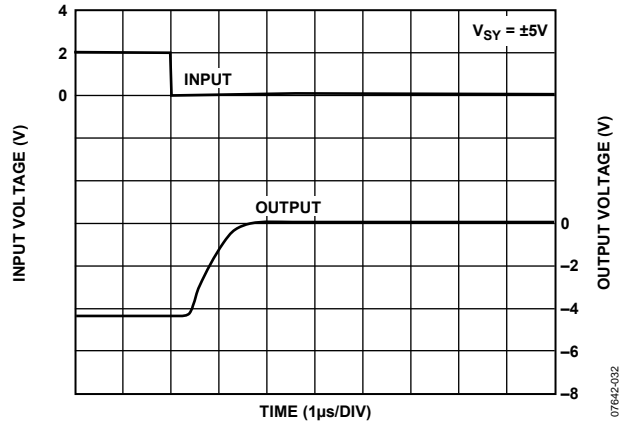


Figure 35. Negative Overload Recovery

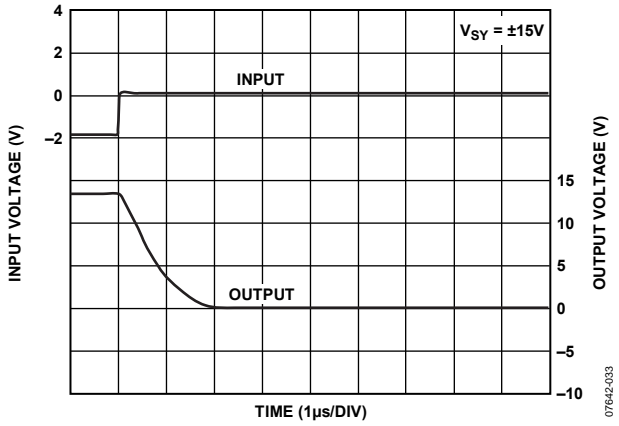


Figure 33. Positive Overload Recovery

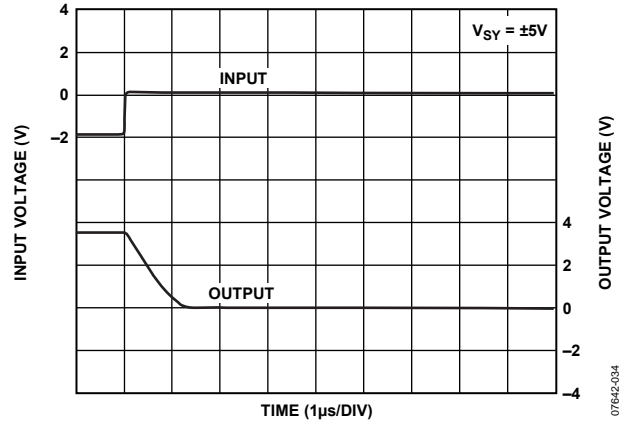


Figure 36. Positive Overload Recovery

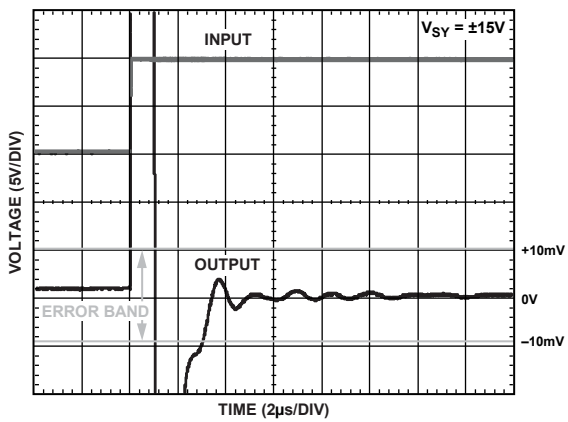


Figure 34. Positive Settling Time to 0.01%

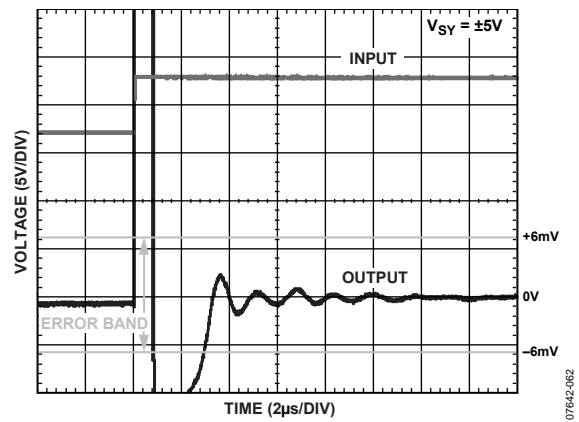


Figure 37. Positive Settling Time to 0.01%

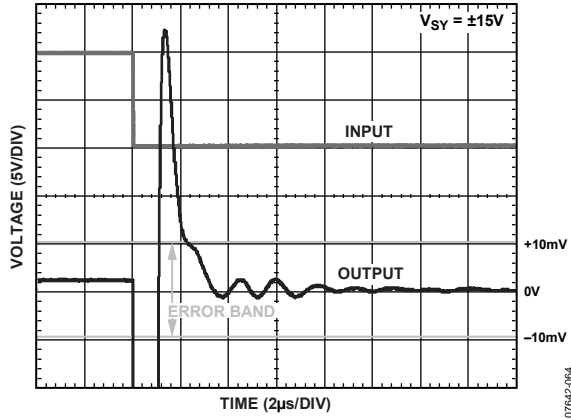


Figure 38. Negative Settling Time to 0.01%

07642-064

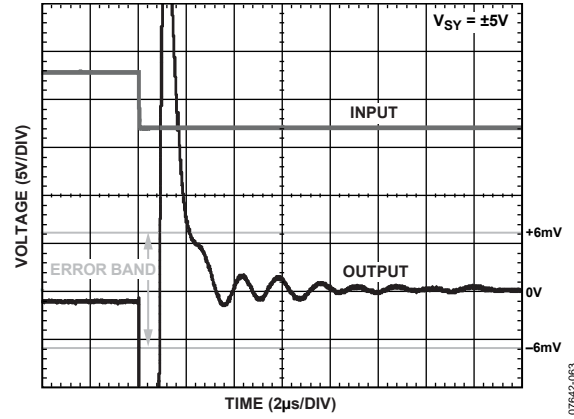


Figure 41. Negative Settling Time to 0.01%

07642-063

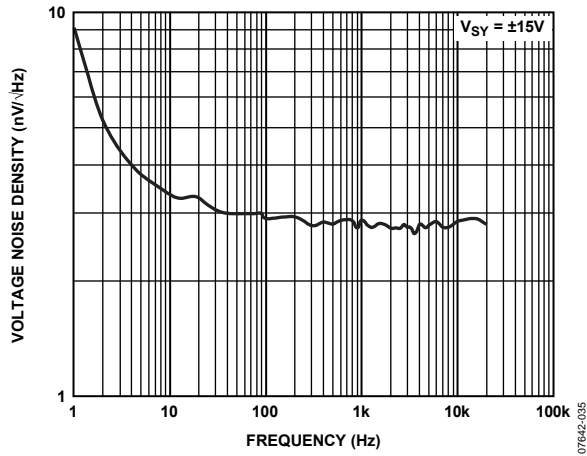


Figure 39. Voltage Noise Density

07642-035

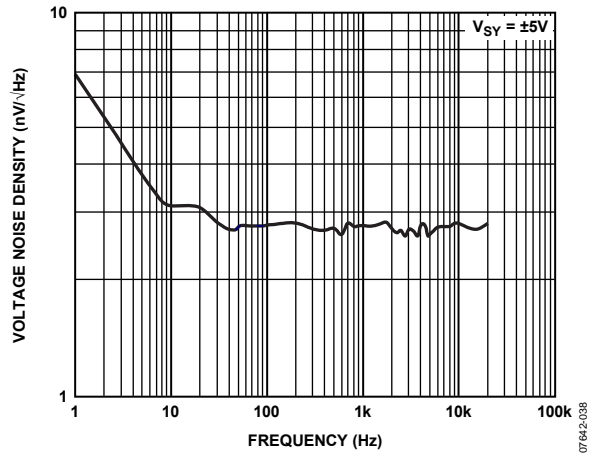


Figure 42. Voltage Noise Density

07642-038

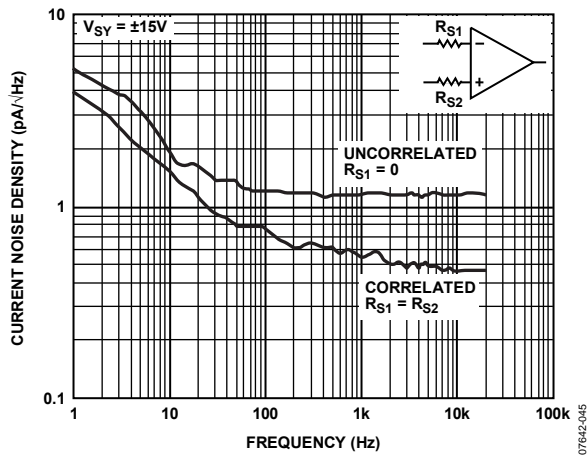


Figure 40. Current Noise Density

07642-045

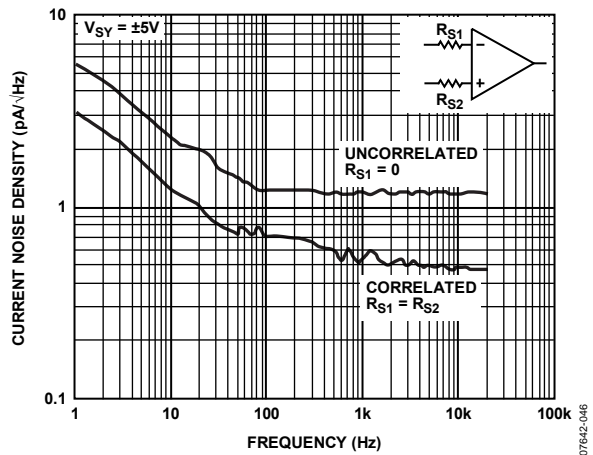


Figure 43. Current Noise Density

07642-046

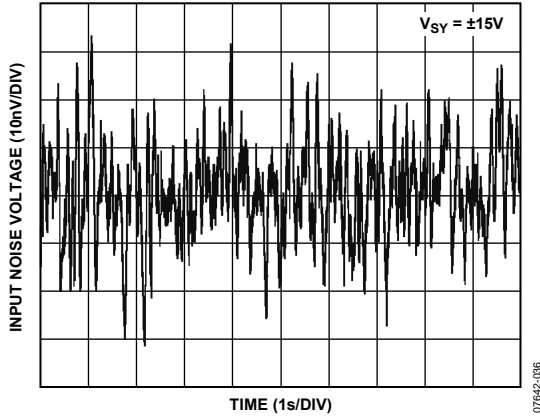


Figure 44. 0.1 Hz to 10 Hz Noise

07642-008

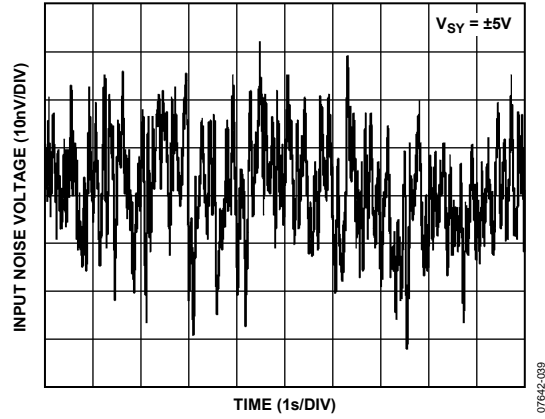


Figure 47. 0.1 Hz to 10 Hz Noise

07642-009

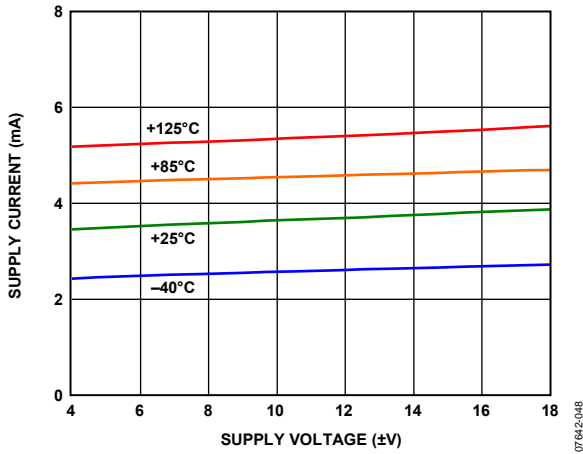


Figure 45. Supply Current vs. Supply Voltage

07642-048

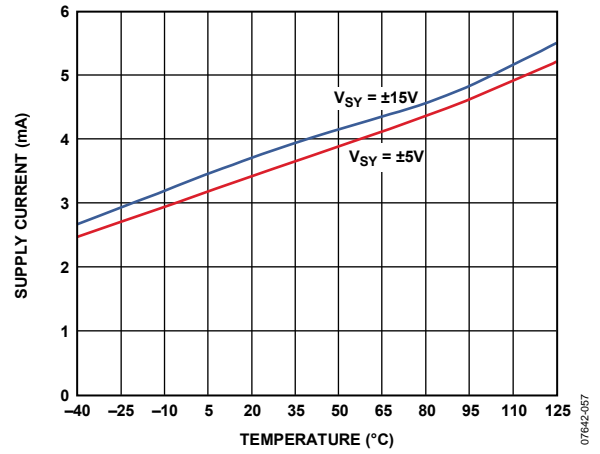


Figure 48. Supply Current vs. Temperature

07642-057

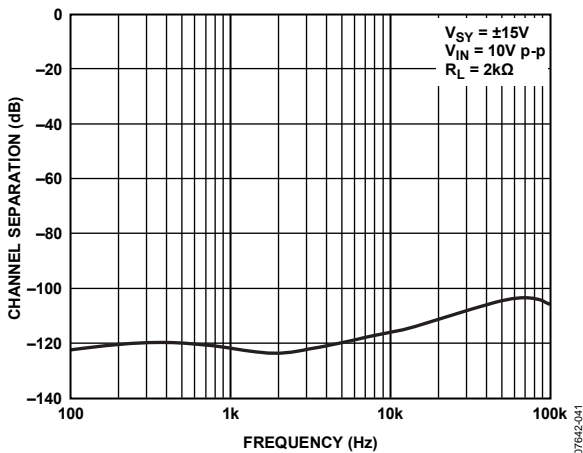


Figure 46. Channel Separation vs. Frequency

07642-041

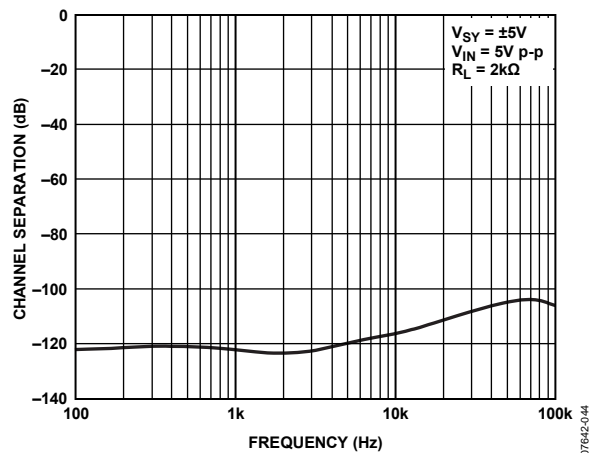


Figure 49. Channel Separation vs. Frequency

07642-044

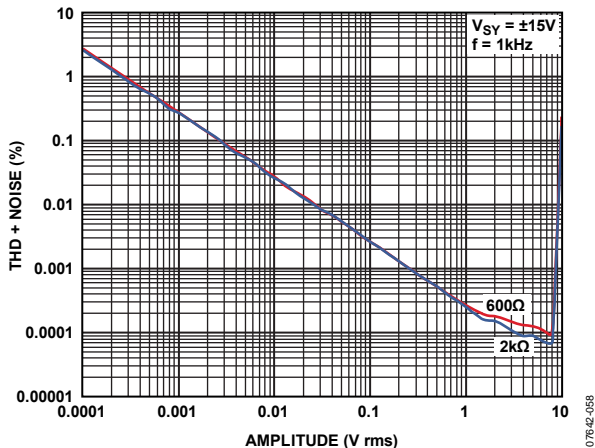


Figure 50. THD + Noise vs. Amplitude

07642-058

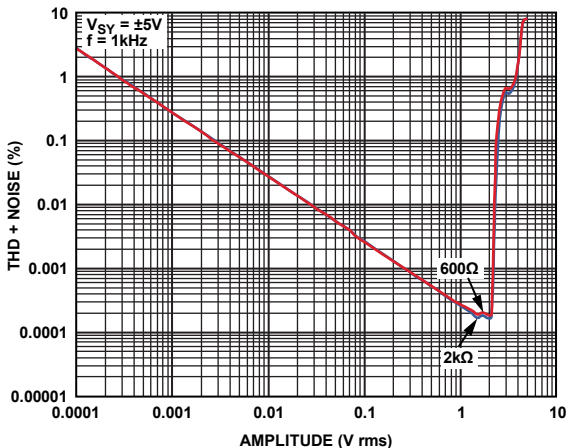


Figure 53. THD + Noise vs. Amplitude

07642-065

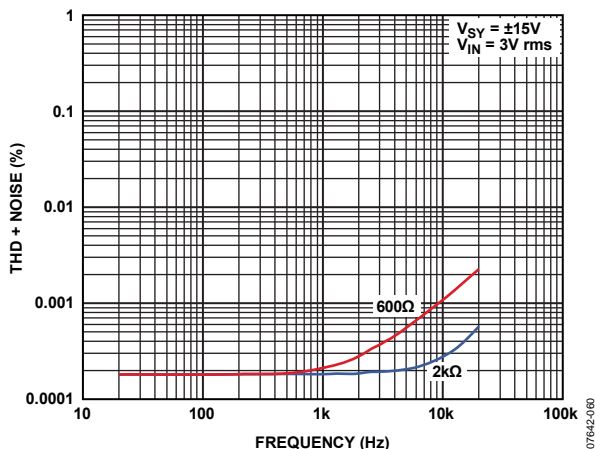


Figure 51. THD + Noise vs. Frequency

07642-060

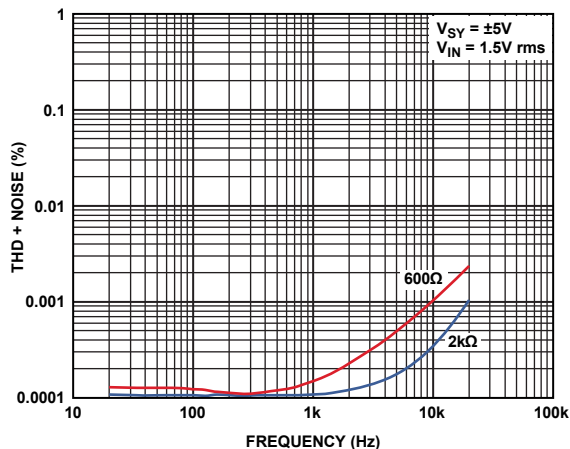


Figure 54. THD + Noise vs. Frequency

07642-067

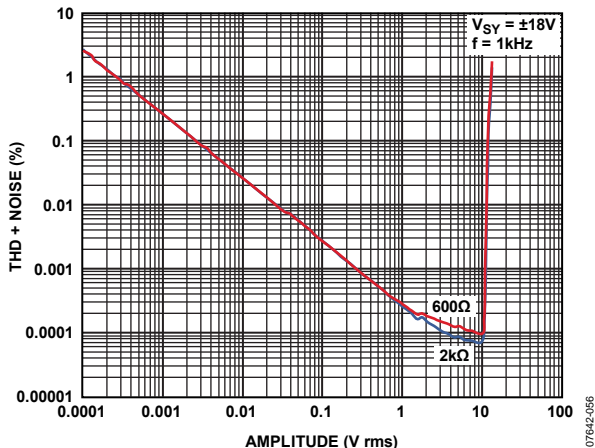


Figure 52. THD + Noise vs. Amplitude

07642-056

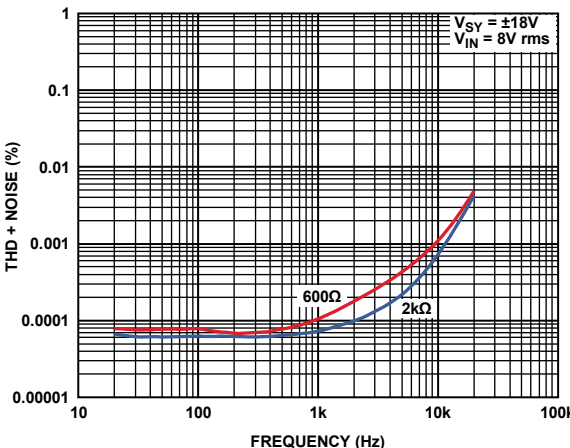


Figure 55. THD + Noise vs. Frequency

07642-069

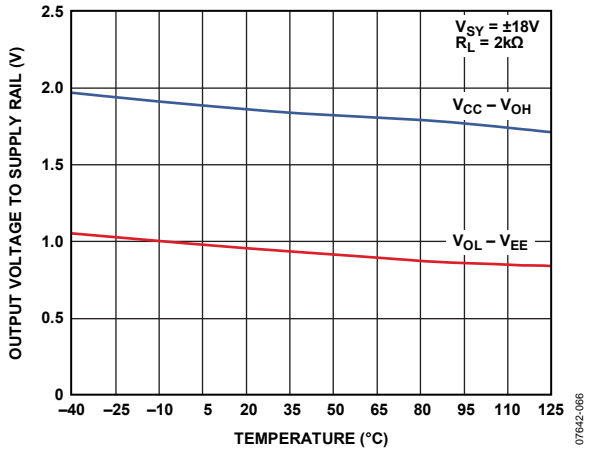


Figure 56. Output Voltage to Supply Rail vs. Temperature

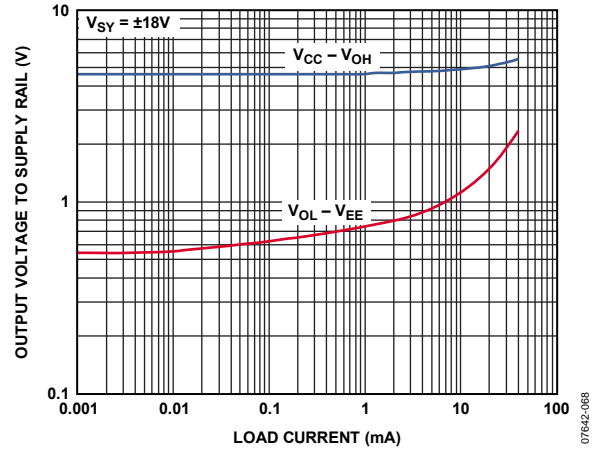


Figure 57. Output Voltage to Supply Rail vs. Load Current

## APPLICATIONS INFORMATION

### INPUT PROTECTION

The maximum differential input voltage that can be applied to the ADA4075-2 is determined by the internal diodes connected across its inputs. These diodes limit the maximum differential input voltage to  $\pm 1$  V and are needed to prevent base-emitter junction breakdown from occurring in the input stage of the ADA4075-2 when very large differential voltages are applied. To make sure that the ultralow voltage noise feature of the ADA4075-2 is preserved, the commonly used internal resistors in series with the inputs were not used to limit the current in the diodes.

In small-signal applications, this is not an issue; however, in applications where large differential voltages can be inadvertently applied to the device, large currents may flow through these diodes. If the differential voltage of the ADA4075-2 exceeds  $\pm 1$  V, external resistors should be used at both inputs of the op amp to limit the input currents to less than  $\pm 10$  mA (see Figure 58). However, when series resistors are added, the total voltage noise degrades because the resistors may have a thermal noise that is greater than the voltage noise of the op amp itself. For example, a 1 k $\Omega$  resistor at room temperature has a thermal noise of 4 nV/ $\sqrt{\text{Hz}}$ , whereas the ADA4075-2 has an ultralow voltage noise of only 2.8 nV/ $\sqrt{\text{Hz}}$  typical.

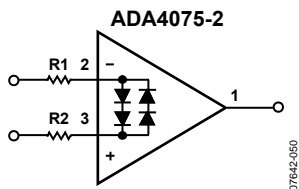


Figure 58. Input Protection

### TOTAL HARMONIC DISTORTION

The total harmonic distortion + noise (THD + N) of the ADA4075-2 is 0.0002% typical with a load resistance of 2 k $\Omega$ . Figure 59 shows the performance of the ADA4075-2 driving a 2 k $\Omega$  load with supply voltages of  $\pm 4$  V and  $\pm 15$  V. Notice that there is more distortion for the supply voltage of  $\pm 4$  V than for a supply voltage of  $\pm 15$  V. Thus, it is very important to operate the ADA4075-2 at a supply voltage greater than  $\pm 5$  V for optimum distortion. The THD + noise graphs for supply voltages of  $\pm 5$  V and  $\pm 18$  V are available in Figure 54 and Figure 55.

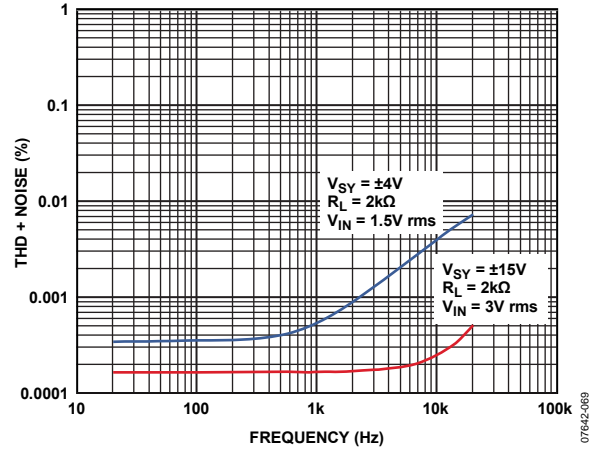


Figure 59. THD + Noise vs. Frequency

### PHASE REVERSAL

Phase reversal occurs in some amplifiers when the input common-mode voltage range is exceeded. When the voltage driving the input to these amplifiers exceeds the maximum input common-mode voltage range, the output of the amplifiers changes polarity. Phase reversal can cause permanent damage to the amplifier as well as system lockups in feedback loops.

The ADA4075-2 amplifiers have been carefully designed to prevent output phase reversal when both inputs are maintained within the specified input voltage range. If one or both inputs exceed the input voltage range but remain within the supply rails, the output is capped at the maximum output that it can swing to. For a supply voltage of  $\pm 15$  V and a load resistance of 2 k $\Omega$ , the output is capped at 13 V typical when the input voltage exceeds the input voltage range but stays within the supply rails. Figure 60 shows the output voltage of the AD4075-2 configured as a unity-gain buffer with a supply voltage of  $\pm 15$  V.

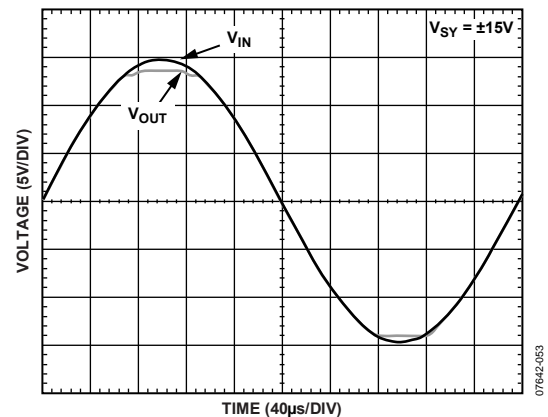


Figure 60. No Phase Reversal

# ADA4075-2

[查询"ADA4075-2ARZ-R7"供应商](#)

## DAC OUTPUT FILTER

The ultralow voltage noise, low distortion, and high slew rate of the ADA4075-2 make it an ideal choice for professional audio signal processing. Figure 61 shows the ADA4075-2 used in a typical audio DAC output filter configuration. The differential outputs of the DAC are fed into the ADA4075-2. The ADA4075-2 is configured as a differential Sallen-key filter. It operates as an external low-pass filter to remove high frequency noise present

on the output pins of the DAC. It also provides differential-to-single-ended conversion from the differential outputs of the DAC.

For a DAC output filter, an op amp with reasonable slew rate and bandwidth is required. The slew rate of the ADA4075-2 is at a high  $12 \text{ V}/\mu\text{s}$ , and the bandwidth is  $6.5 \text{ MHz}$ . The cutoff frequency of the low-pass filter is approximately  $167 \text{ kHz}$ . In addition, the  $100 \text{ k}\Omega$  and  $47 \mu\text{F}$  RC network perform ac coupling to block out the dc components at the output.

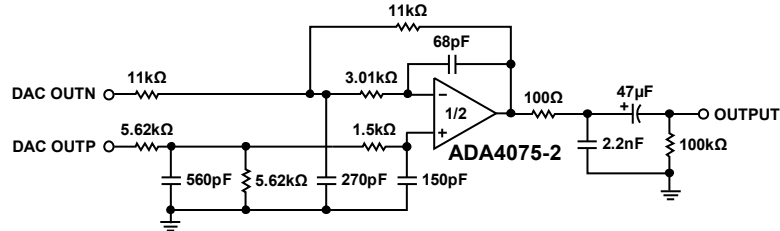


Figure 61. Typical DAC Output Filter Circuit (Differential)

07642-0164





# ADA4075-2

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## BALANCED LINE RECEIVER

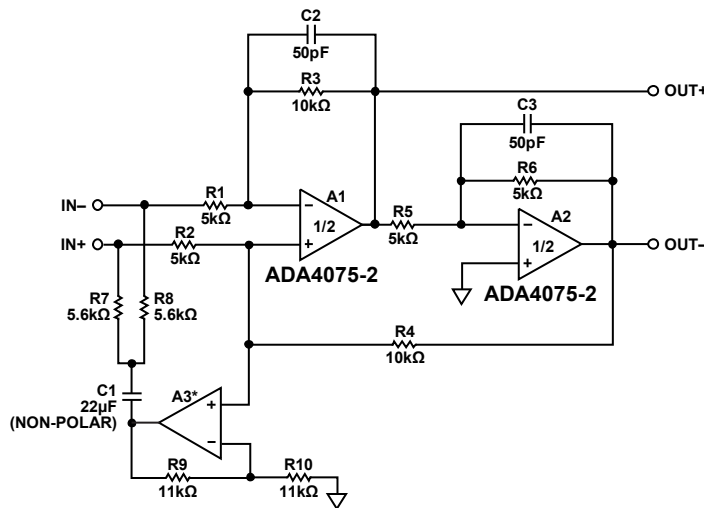
Figure 63 depicts a unity-gain balanced line receiver capable of a high degree of hum rejection. The CMRR is approximately given by

$$20 \log_{10} \left( \frac{R1R4}{R2R3} \right)$$

Therefore, R1 to R4 should be close-tolerance components to obtain the best possible CMRR without adjustment. The presence of A2 ensures that the impedances are symmetric at the two inputs (unlike many other designs), and, as a bonus, A2 also provides a

complementary output. A3 raises the common-mode input impedance from about 7.5 kΩ to about 70 kΩ, reducing the degradation of CMRR due to mismatches in source impedance. It should be noted that A3 is not in the signal path, and almost any op amp will work well here. Although it may seem as though the inverting output should be noisier than the noninverting one, they are in fact symmetric at about -111 dBV (20 kHz bandwidth).

Sometimes an overall gain of ½ is desired to provide an extra 6 dB of differential input headroom. This can be attained by reducing R3 and R4 to 5 kΩ and increasing R9 to 22 kΩ.



\*A3 REDUCES THE DEGRADATION OF CMRR  
(SEE THE BALANCED LINE RECEIVER SECTION FOR MORE DETAILS).

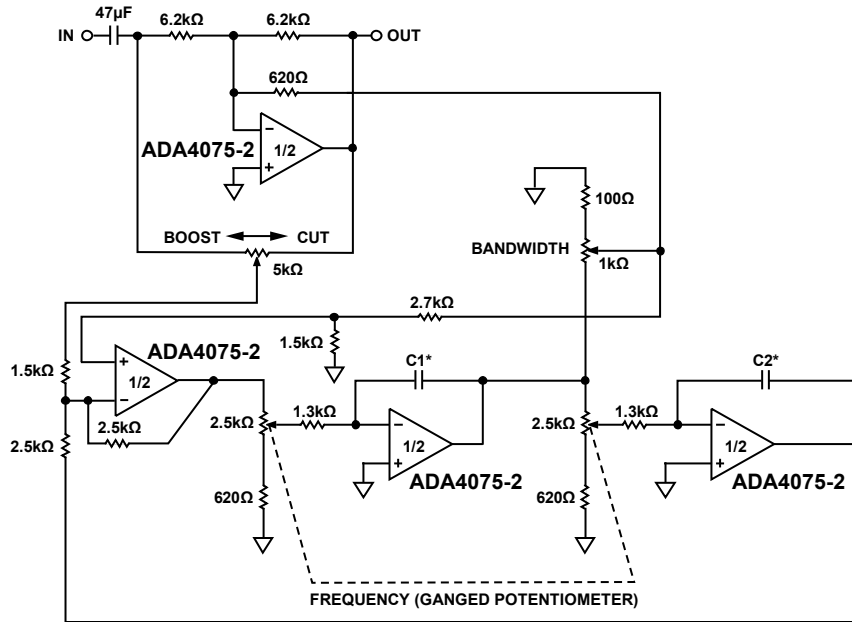
Figure 63. Balanced Line Receiver

07642-071

**LOW NOISE PARAMETRIC EQUALIZER**

The circuit of Figure 64 is a reciprocal parametric equalizer yielding  $\pm 20$  dB of cut or boost with variable bandwidth and frequency. The frequency control range is 6.9:1, with the geometric mean center frequency conveniently occurring at the midpoint of the potentiometer setting. The center frequency is equal to

$48 \text{ Hz}/C_t$ , where  $C_t$  is the value of  $C_1$  and  $C_2$  in microfarads. The bandwidth control adjusts the  $Q$  from 0.9 to about 11. The overall noise is setting dependent, but with all controls centered it is about  $-104 \text{ dBV}$  in a 20 kHz bandwidth. Such a low noise level can obviate the need for a bypass switch in many applications.



\*THE CENTER FREQUENCY IS AFFECTED BY THE VALUE OF  $C_1$  AND  $C_2$  (SEE THE LOW NOISE PARAMETRIC EQUALIZER SECTION FOR MORE DETAILS).

07642-074

Figure 64. Low Noise Parametric Equalizer

SCHEMATIC

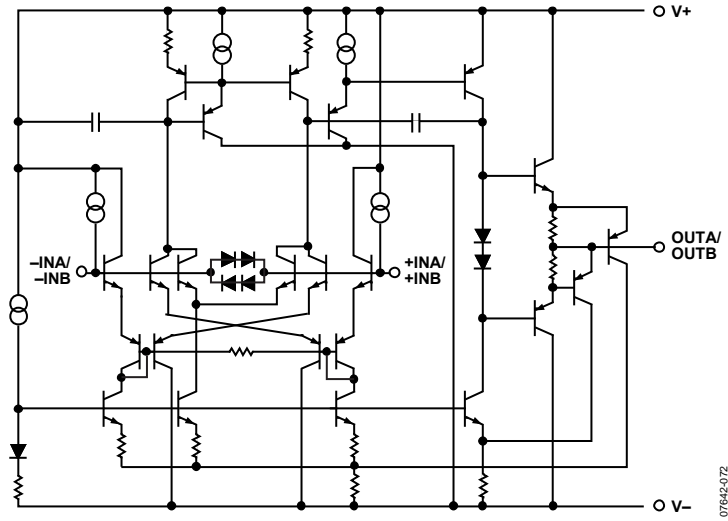
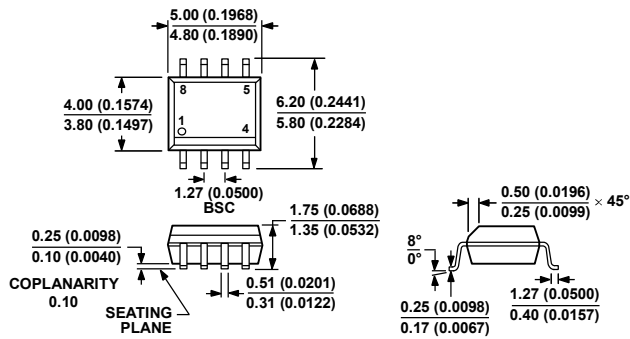


Figure 65. Simplified Schematic

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 66. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

Dimensions shown in millimeters and (inches)

012407-A

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4075-2ARZ <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8
ADA4075-2ARZ-R7 <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8
ADA4075-2ARZ-RL <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8

<sup>1</sup> Z = RoHS Compliant Part.

**ADA4075-2**

[查询"ADA4075-2ARZ-R7"供应商](#)

## NOTES

**NOTES**

**ADA4075-2**

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## NOTES