查询"BD9132MUV"供应商

Single-chip Type with built-in FET Switching Regulator Series

Output 2A or More High Efficiency Step-down Switching Regulator with Built-in Power MOSFET

BD9132MUV

●Description

ROHM's high efficiency step-down switching regulator BD9132MUV is a power supply designed to produce a low voltage including 0.8 volts from 5.5/3.3 volts power supply line. Offers high efficiency with our original pulse skip control technology and synchronous rectifier. Employs a current mode control system to provide faster transient response to sudden change in load.

●Features

1) Offers fast transient response with current mode PWM control system.
2) Offers highly efficiency for all load range with synchronous rectifier (Nch/Nch FET) and SLLM (Simple Light Load Mode)
3) Incorporates soft-start function.
4) Incorporates thermal protection and ULVO functions.
5) Incorporates short-current protection circuit with time delay function.
6) Incorporates shutdown function Icc=0μA(Typ.)
7) Employs small surface mount package : VQFN020V4040

●Use

Power supply for LSI including DSP, Micro computer and ASIC

●Absolute Maximum Rating (Ta=25℃)

Parameter	Symbol	Limits	Unit
		BD9132MUV	
VCC Voltage	VCC	-0.3～+7 *1	V
PVCC Voltage	PVCC	-0.3～+7 *1	V
BST Voltage	VBST	-0.3～+13	V
BST_SW Voltage	VBST-SW	-0.3～+7	V
EN Voltage	VEN	-0.3～+7	V
SW,ITH Voltage	VSW, VITH	-0.3～+7	V
Power Dissipation 1	Pd1	0.34 *2	W
Power Dissipation 2	Pd2	0.70 *3	W
Power Dissipation 3	Pd3	1.21 *4	W
Power Dissipation 4	Pd4	3.56 *5	W
Operating temperature range	Topr	-40～+105	℃
Storage temperature range	Tstg	-55～+150	℃
Maximum junction temperature	Tj	+150	℃

＊1 Pd should not be exceeded.
＊2 IC only
＊3 1-layer. mounted on a 74.2mm×74.2mm×1.6mm glass-epoxy board, occupied area by copper foil : 10.29mm^2
＊4 4-layer. mounted on a 74.2mm×74.2mm×1.6mm glass-epoxy board, occupied area by copper foil : 10.29mm^2 , in each layers
＊5 4-layer. mounted on a 74.2mm×74.2mm×1.6mm glass-epoxy board, occupied area by copper foil : 5505mm^2, in each layers

●Operating Conditions (Ta=-40～+105℃)

Parameter	Symbol	BD9132MUV			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	VCC	2.7	3.3	5.5	V
	PVCC	2.7	3.3	5.5	V
EN Voltage	VEN	0	-	5.5	V
Output voltage Setting Range	VOUT	0.8	-	3.3*6	V
SW average output current	ISW	-	-	3.0*7	A

＊6 In case set output voltage 1.6V or more, VccMin = Vout+1.2V.
＊7 Pd should not be exceeded.

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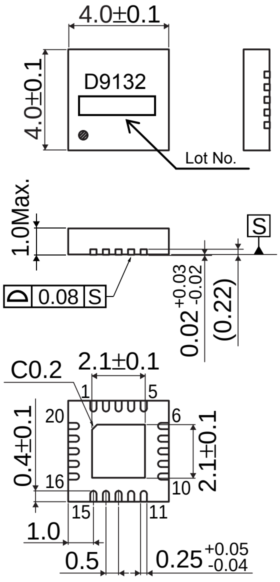
●Electrical Characteristics

◎BD9132MUV (Ta=25℃ VCC=PVCC=3.3V, EN=VCC, R_1=10kΩ, R_2=5kΩ, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Standby current	ISTB	-	0	10	μA	EN=GND
Active current	ICC	-	250	500	μA	
EN Low voltage	VENL	-	GND	0.8	V	Standby mode
EN High voltage	VENH	2.0	Vcc	-	V	Active mode
EN input current	IEN	-	1	10	μA	VEN=3.3V
Oscillation frequency	FOSC	0.8	1	1.2	MHz	
High side FET ON resistance	RONH	-	82	115	mΩ	PVCC=3.3V
Low side FET ON resistance	RONL	-	70	98	mΩ	PVCC=3.3V
ADJ Voltage	VADJ	0.788	0.800	0.812	V	
ITH sink current	ITHSI	10	18	-	μA	VADJ=1V
ITH source current	ITHSO	10	18	-	μA	VADJ=0.6V
UVLO threshold voltage	VUVLO1	2.400	2.500	2.600	V	VCC=3.3V→0V
UVLO release voltage	VUVLO2	2.425	2.550	2.700	V	VCC=0V→3.3V
Soft start time	TSS	2.5	5	10	ms	
Timer latch time	TLATCH	0.5	1	2	ms	
Output Short circuit Threshold Voltage	VSCP	-	0.40	0.56	V	VADJ =0.8V→0V

●Block Diagram, Application Circuit

【BD9132MUV】



(Unit : mm)

Fig.1 BD9132MUV TOP View

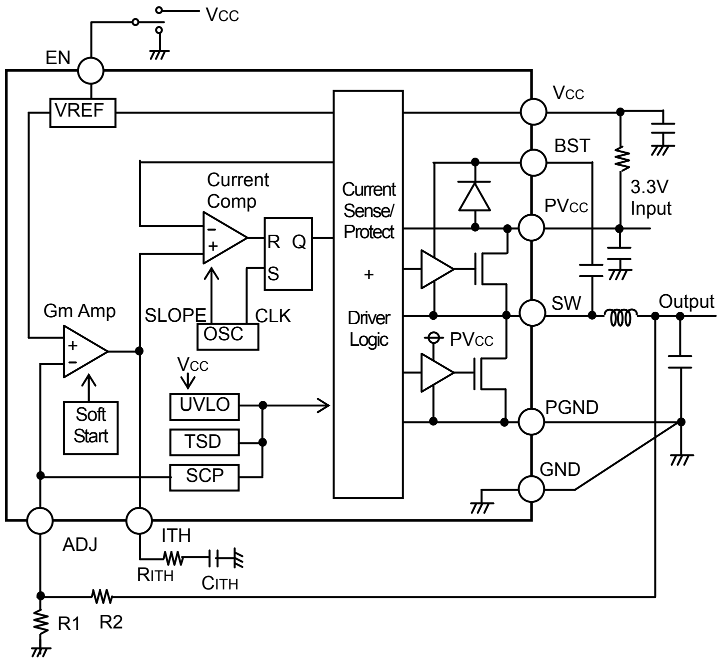


Fig.2 BD9132MUV Block Diagram

●Pin No. & function table

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	SW	SW pin	11	GND	Ground
2	SW	SW pin	12	ADJ	Output voltage detect pin
3	SW	SW pin	13	ITH	GmAmp output pin/Connected phase compensation capacitor
4	SW	SW pin	14	N.C.	Non Connection
5	SW	SW pin	15	N.C.	Non Connection
6	PVCC	Highside FET source pin	16	N.C.	Non Connection
7	PVCC	Highside FET source pin	17	EN	Enable pin(High Active)
8	PVCC	Highside FET source pin	18	PGND	Lowside FET source pin
9	BST	Bootstrapped voltage input pin	19	PGND	Lowside source pin
10	VCC	VCC power supply input pin	20	PGND	Lowside source pin

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●Characteristics data【BD9132MUV】

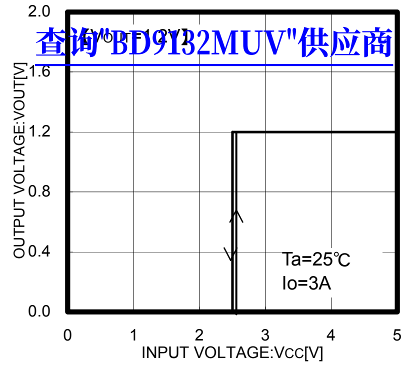

Fig.3 Vcc - VOUT

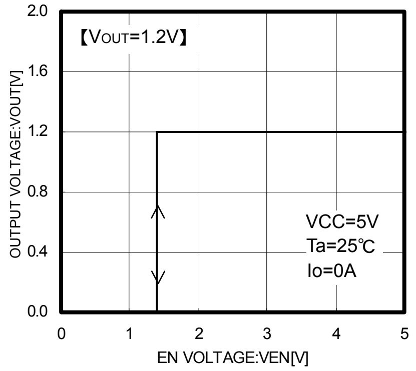

Fig.4 VEN - VOUT

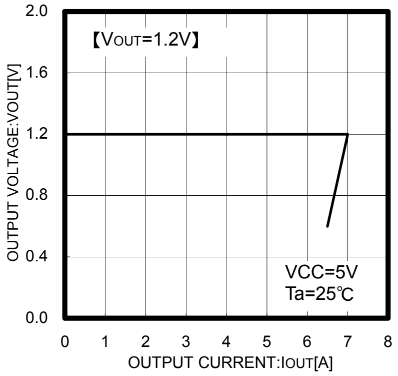

Fig.5 IOUT - VOUT

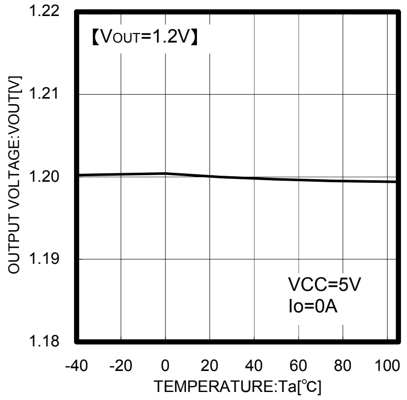

Fig. 6 Ta - VOUT

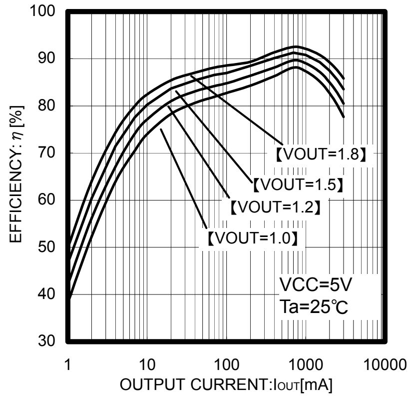

Fig.7 Efficiency

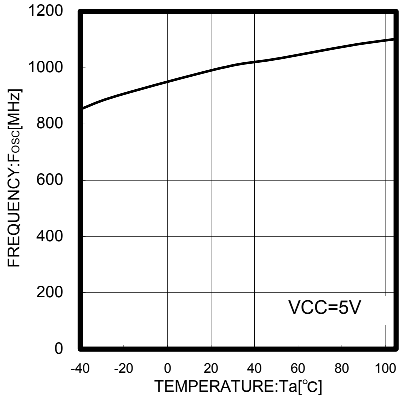

Fig.8 Ta - Fosc

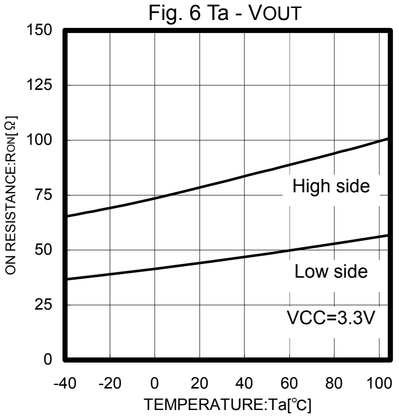

Fig.9 Ta – RONN, RONP

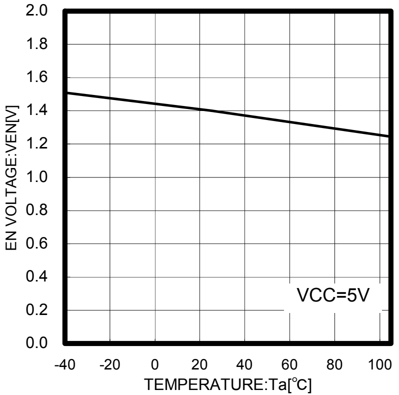

Fig.10 Fig.11 Ta - VEN

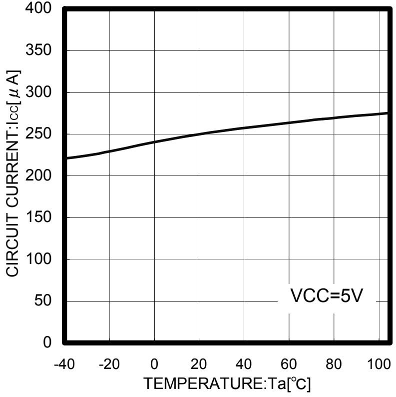

Fig.11 Ta - Icc

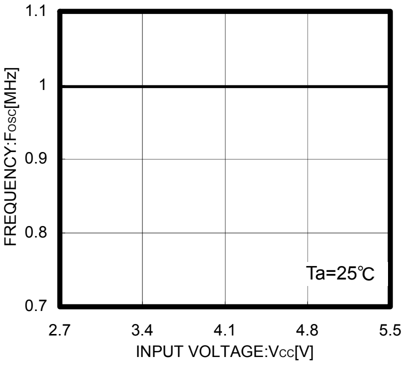

Fig.12 Vcc - Fosc

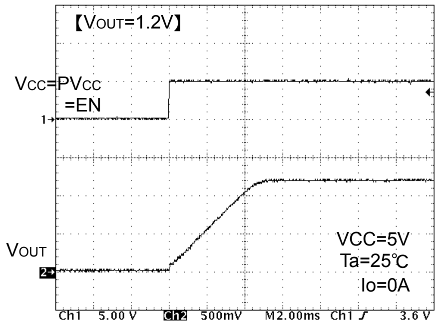

Fig.13 Soft start waveform

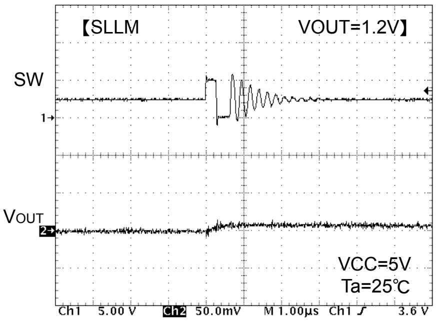

Fig.14 SW waveform Io=10mA

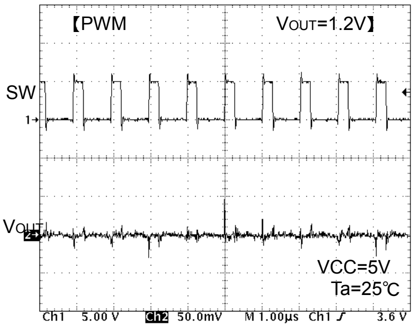

Fig.15 SW waveform Io=3A

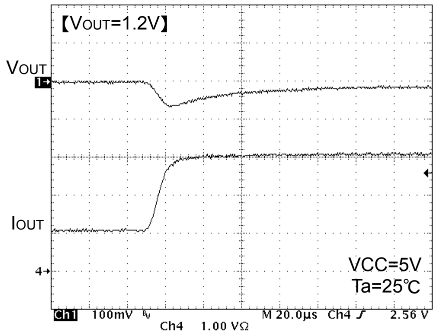

Fig. 16 Transient Response
Io=1→3A(10μs)

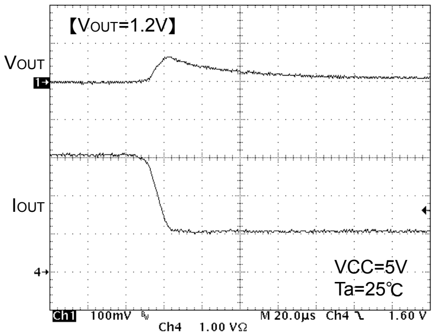

Fig.17 Transient Response
Io=3→1A(10μs)

●Information on advantages

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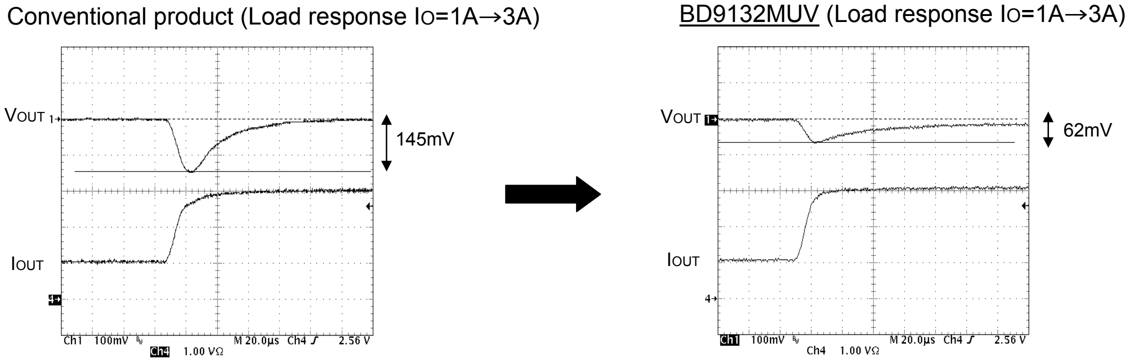
Advantage 1 : Offers fast transient response with current mode control system.



Voltage drop due to sudden change in load was reduced by about 50%.

Fig.18 Comparison of transient response

Advantage 2 : Offers high efficiency for all load range.

- For lighter load:

Utilizes the current mode control mode called SLLM for lighter load, which reduces various dissipation such as switching dissipation (P_{SW}), gate charge/discharge dissipation, ESR dissipation of output capacitor (P_{ESR}) and on-resistance dissipation (P_{RON}) that may otherwise cause degradation in efficiency for lighter load.

↓

Achieves efficiency improvement for lighter load.

- For heavier load:

Utilizes the synchronous rectifying mode and the low on-resistance MOS FETs incorporated as power transistor.

ON resistance of Highside MOS FET : 82mΩ(Typ.)
ON resistance of Lowside MOS FET : 70mΩ(Typ.)

↓

Achieves efficiency improvement for heavier load.

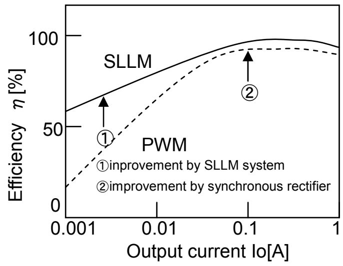


Fig.19 Efficiency

Offers high efficiency for all load range with the improvements mentioned above.

Advantage 3 : ・Supplied in smaller package due to small-sized power MOS FET incorporated.

- Output capacitor Co required for current mode control: 22µF ceramic capacitor
- Inductance L required for the operating frequency of 1 MHz: 2.2µH inductor
- Incorporates FET + Boot strap diode

↓

Reduces a mounting area required.

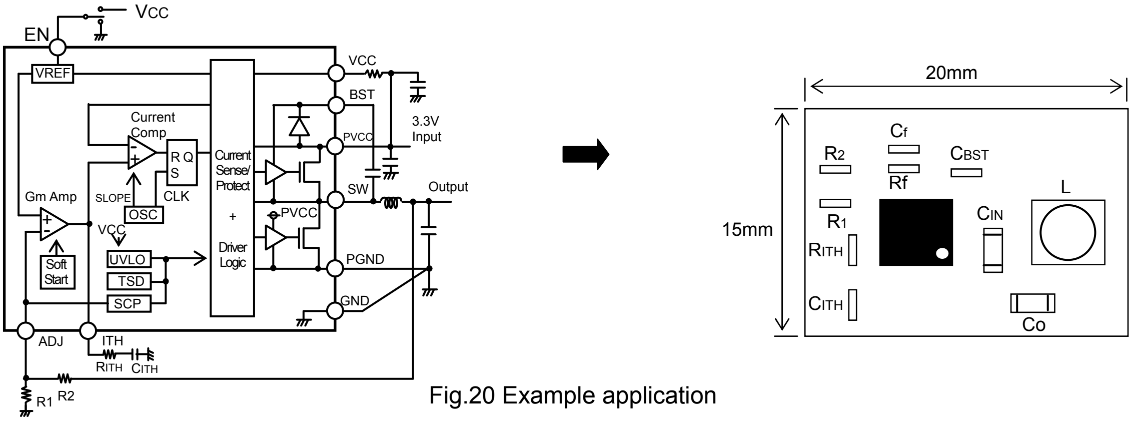


Fig.20 Example application

●Operation

BD9132MUV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM (Simple Light Load Mode) operation for lighter load to improve efficiency.

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○Synchronous rectifier

It does not require the power to be dissipated by a rectifier externally connected to a conventional DC/DC converter IC, and its P.N junction shoot-through protection circuit limits the shoot-through current during operation, by which the power dissipation of the set is reduced.

○Current mode PWM control

Synthesizes a PWM control signal with a inductor current feedback loop added to the voltage feedback.

・PWM (Pulse Width Modulation) control

The oscillation frequency for PWM is 1 MHz. SET signal form OSC turns ON a highside MOS FET (while a lowside MOS FET is turned OFF), and an inductor current I_L increases. The current comparator (Current Comp) receives two signals, a current feedback control signal (SENSE: Voltage converted from I_L) and a voltage feedback control signal (FB), and issues a RESET signal if both input signals are identical to each other, and turns OFF the highside MOS FET (while a lowside MOS FET is turned ON) for the rest of the fixed period. The PWM control repeat this operation.

・SLLM (Simple Light Load Mode) control

When the control mode is shifted from PWM for heavier load to the one for lighter load or vise versa, the switching pulse is designed to turn OFF with the device held operated in normal PWM control loop, which allows linear operation without voltage drop or deterioration in transient response during the mode switching from light load to heavy load or vise versa.

Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is so designed that the RESET signal is held issued if shifted to the light load mode, with which the switching is tuned OFF and the switching pulses are thinned out under control. Activating the switching intermittently reduces the switching dissipation and improves the efficiency.

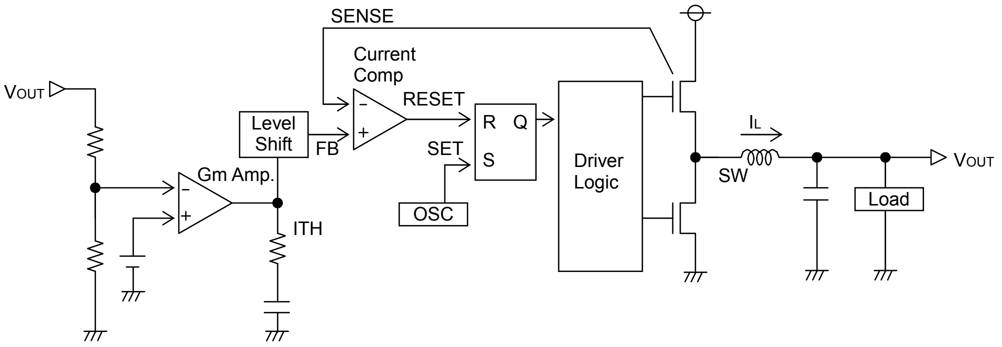

Fig.21 Diagram of current mode PWM control

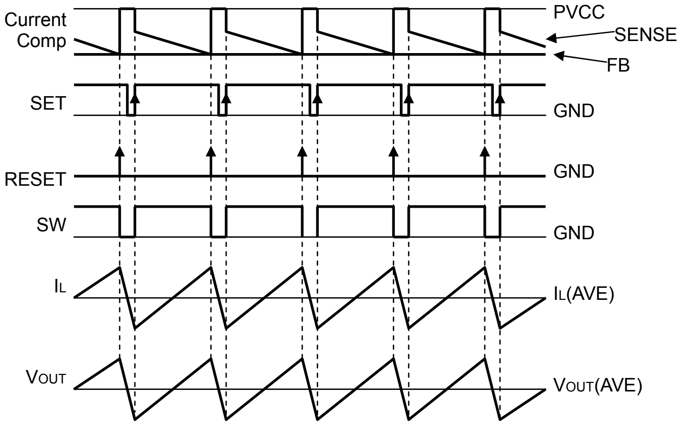

Fig.22 PWM switching timing chart

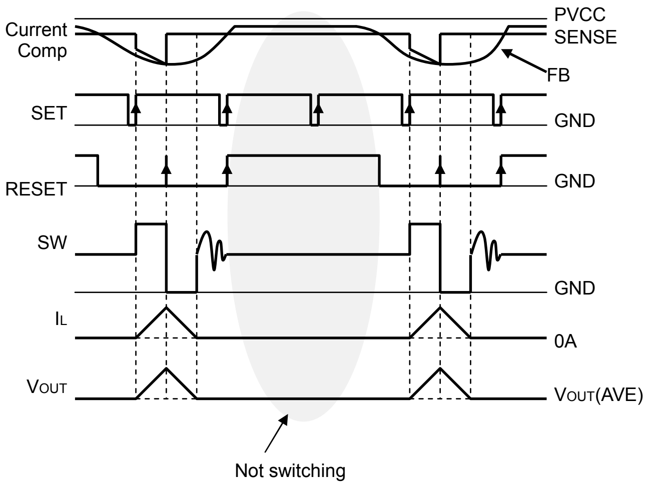

Fig.23 SLLM^{TM} switching timing chart

●Description of operations

・Soft-start function

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EN terminal shifted to "High" activates a soft-starter to gradually establish the output voltage with the current limited during startup, by which it is possible to prevent an overshoot of output voltage and an inrush current.

・Shutdown function

With EN terminal shifted to "Low", the device turns to Standby Mode, and all the function blocks including reference voltage circuit, internal oscillator and drivers are turned to OFF. Circuit current during standby is 0μF (Typ.).

・UVLO function

Detects whether the input voltage sufficient to secure the output voltage of this IC is supplied. And the hysteresis width of 50mV (Typ.) is provided to prevent output chattering.

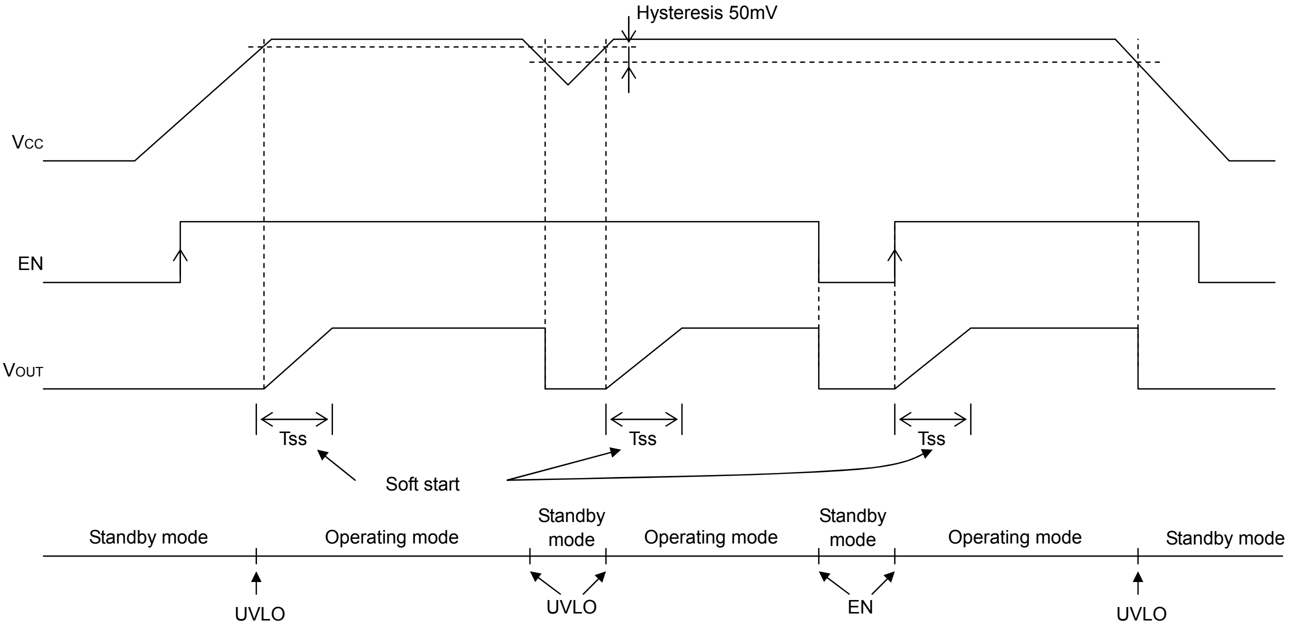

Fig.24 Soft start, Shutdown, UVLO timing chart

- Short-current protection circuit with time delay function

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Turns OFF the output to protect the IC from breakdown when the incorporated current limiter is activated continuously for the fixed time(T_{LATCH}) or more. The output thus held tuned OFF may be recovered by restarting EN or by re-unlocking UVLO.

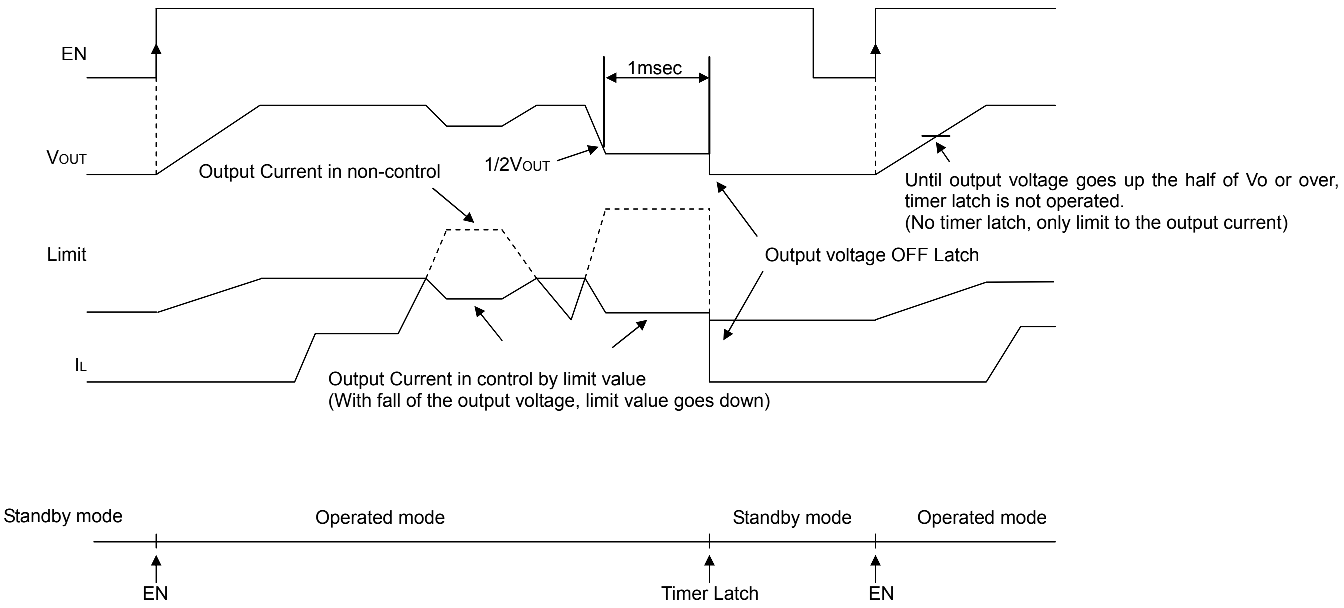

Fig.25 Short-current protection circuit with time delay timing chart

●Switching regulator efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT}\times I_{OUT}}{Vin\times Iin}\times 100[\%] = \frac{P_{OUT}}{Pin}\times 100[\%] = \frac{P_{OUT}}{P_{OUT}+P_{D}\,\alpha}\times 100[\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors $P_{D}\alpha$ as follows:

Dissipation factors:

1) ON resistance dissipation of inductor and FET : $PD(I^2R)$
2) Gate charge/discharge dissipation : PD(Gate)
3) Switching dissipation : PD(SW)
4) ESR dissipation of capacitor : PD(ESR)
5) Operating current dissipation of IC : PD(IC)

1)$PD(I^2R)=I_{OUT}^2\times(R_{COIL}+R_{ON})$ ($R_{COIL}[\Omega]$: DC resistance of inductor, $R_{ON}[\Omega]$: ON resistance of FET, $I_{OUT}[A]$: Output current.)

2)$PD(Gate)=Cgs\times f\times V$ (Cgs[F] : Gate capacitance of FET、f[H] : Switching frequency、V[V] : Gate driving voltage of FET)

3)$PD(SW)=\dfrac{Vin^2\times C_{RSS}\times I_{OUT}\times f}{I_{DRIVE}}$ (C_{RSS}[F] : Reverse transfer capacitance of FET、I_{DRIVE}[A] : Peak current of gate.)

4)$PD(ESR)=I_{RMS}^2\times ESR$ (I_{RMS}[A] : Ripple current of capacitor、ESR[Ω] : Equivalent series resistance.)

5)$PD(IC)=Vin\times I_{CC}$ (I_{CC}[A] : Circuit current.)

●Consideration on permissible dissipation and heat generation

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As this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON resistance of FET are considered. Because the conduction losses are considered to play the leading role among other dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.

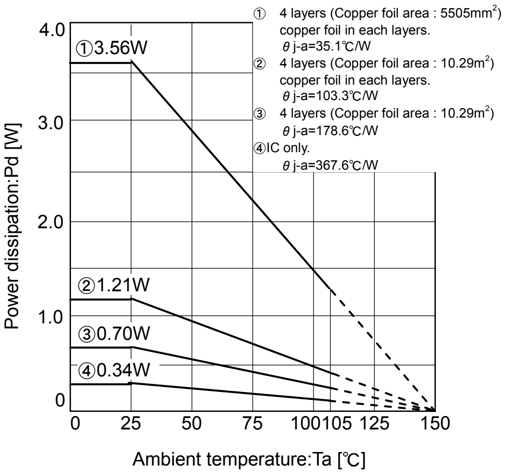

Fig.26 Thermal derating curve
(VQFN020V4040)

$P=I_{OUT}^2 \times R_{ON}$

$R_{ON}=D \times R_{ONP}+(1-D)R_{ONN}$

D : ON duty (=V_{OUT}/V_{CC})

R_{ONH} : ON resistance of Highside MOS FET

R_{ONL} : ON resistance of Lowside MOS FET

I_{OUT} : Output current

If V_{CC}=3.3V, V_{OUT}=1.8V, R_{ONH}=82mΩ, R_{ONL}=70mΩ

I_{OUT}=3A, for example,

$$D=V_{OUT}/V_{CC}=1.8/3.3=0.545$$

$$\begin{aligned} R_{ON} &= 0.545 \times 0.082+(1-0.545) \times 0.07 \\ &= 0.0447+0.0319 \\ &= 0.0766[\Omega] \end{aligned}$$

$$P=3^2 \times 0.0766 = 0.6894[W]$$

As R_{ONH} is greater than R_{ONL} in this IC, the dissipation increases as the ON duty becomes greater. With the consideration on the dissipation as above, thermal design must be carried out with sufficient margin allowed.

●Selection of components externally connected

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1. Selection of inductor (L)

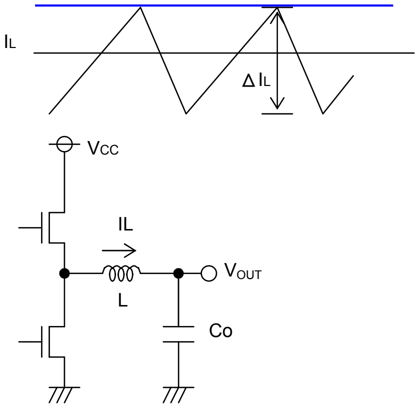

Fig.27 Output ripple current

The inductance significantly depends on output ripple current. As seen in the equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times f} \text{ [A]} \cdots (1)$$

Appropriate ripple current at output should be 20% more or less of the maximum output current.

$$\Delta I_L = 0.2 \times I_{OUT}\text{max. [A]} \cdots (2)$$

$$L = \frac{(V_{CC}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{CC} \times f} \text{ [H]} \cdots (3)$$

(ΔI_L: Output ripple current, and f: Switching frequency)

※Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=5.0V, V_{OUT}=2.5V, f=1MHz, $\Delta I_L = 0.2 \times 3A = 0.6A$, for example,(BD9132MUV)

$$L = \frac{(5-2.5) \times 2.5}{0.6 \times 5 \times 1M} = 2.08\mu \rightarrow 2.2[\mu H]$$

※Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

2. Selection of output capacitor (C_O)

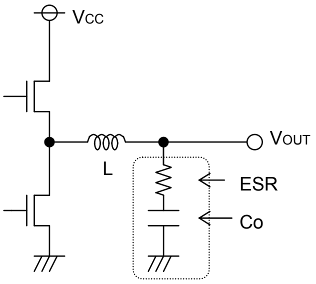

Fig.28 Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required to smooth ripple voltage.

Output ripple voltage is determined by the equation (4) :

$$\Delta V_{OUT} = \Delta I_L \times ESR \text{ [V]} \cdots (4)$$

(ΔI_L: Output ripple current, ESR: Equivalent series resistance of output capacitor)

※Rating of the capacitor should be determined allowing sufficient margin against output voltage. A 22μF to 100μF ceramic capacitor is recommended. Less ESR allows reduction in output ripple voltage.

3. Selection of input capacitor (Cin)

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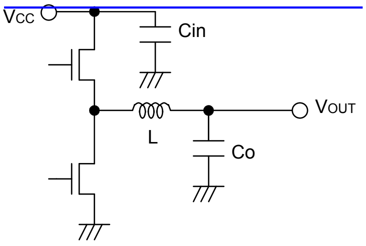

Fig.29 Input capacitor

Input capacitor to select must be a low ESR capacitor of the capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (5):

$$I_{RMS}=I_{OUT}\times\frac{\sqrt{V_{OUT}(V_{CC}-V_{OUT})}}{V_{CC}}\ [A]\cdot\cdot\cdot(5)$$

< Worst case > $I_{RMS(max.)}$

When $V_{CC}=2\times V_{OUT}$, $I_{RMS}=\frac{I_{OUT}}{2}$

If V_{CC}=3.3V, V_{OUT}=1.8V, and $I_{OUTmax.}$=3A, (BD9132MUV)

$$I_{RMS}=2\times\frac{\sqrt{1.8(3.3-1.8)}}{3.3}=1.49[A_{RMS}]$$

A low ESR 22μF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

4. Determination of RITH, CITH that works as a phase compensator

As the Current Mode Control is designed to limit a inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of a output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

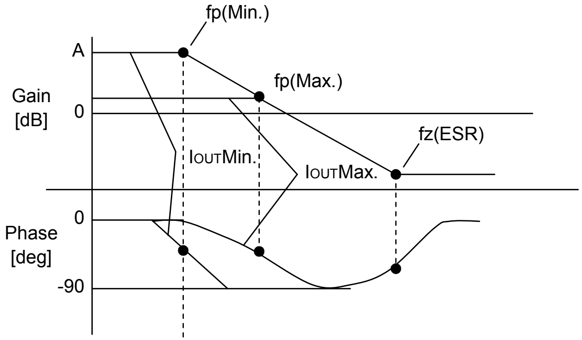

Fig.30 Open loop gain characteristics

$$fp=\frac{1}{2\pi\times R_O\times C_O}$$

$$fz_{(ESR)}=\frac{1}{2\pi\times ESR\times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency lowers.

$$fp_{(Min.)}=\frac{1}{2\pi\times R_{OMax.}\times C_O}\ [Hz]\text{←with lighter load}$$

$$fp_{(Max.)}=\frac{1}{2\pi\times R_{OMin.}\times C_O}\ [Hz]\ \text{←with heavier load}$$

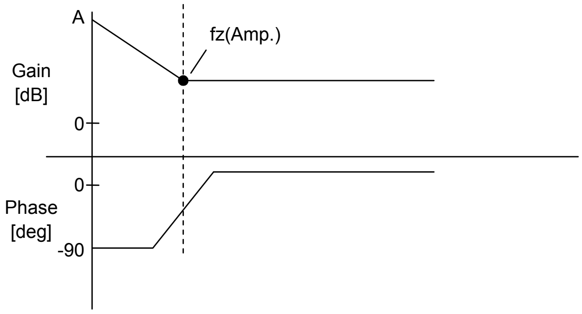

Fig.31 Error amp phase compensation characteristics

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR reduces to half.)

$$fz_{(Amp.)}=\frac{1}{2\pi\times R_{ITH}\times C_{ITH}}$$

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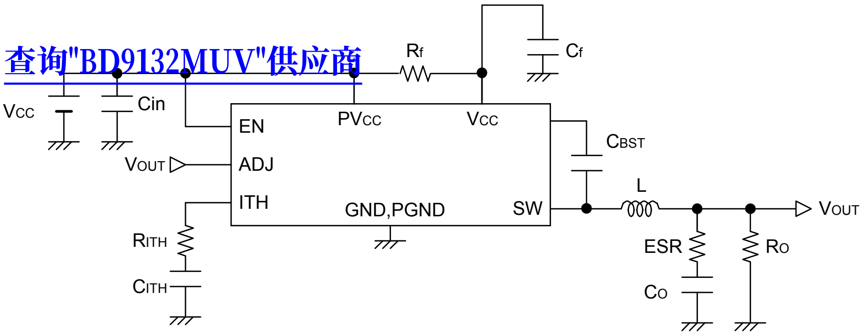

Fig.32 Typical application

Stable feedback loop may be achieved by canceling the pole fp (Min.) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$f_{z(\mathrm{Amp.})} = f_{p(\mathrm{Min.})}$$

$$\longrightarrow \frac{1}{2\pi \times R_{\mathrm{ITH}} \times C_{\mathrm{ITH}}} = \frac{1}{2\pi \times R_{\mathrm{OMax.}} \times C_{\mathrm{O}}}$$

5. Determination of output voltage

The output voltage VOUT is determined by the equation (6):

$V_{OUT}=(R2/R1+1)\times V_{ADJ}$ ・・・(6)　VADJ: Voltage at ADJ terminal (0.8V Typ.)

With R1 and R2 adjusted, the output voltage may be determined as required.

(Adjustable output voltage range : 0.8V～3.3V)

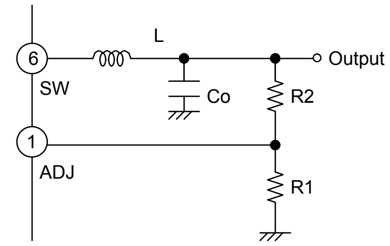

Fig.33 Determination of output voltage

Use 1 kΩ～100 kΩ resistor for R1. If a resistor of the resistance higher than 100 kΩ is used, check the assembled set carefully for ripple voltage etc.

The lower limit of input voltage depends on the output voltage.
Basically, it is recommended to use in the condition :

VCCmin = VOUT+1.2V.

Fig.34. shows the necessary output current value at the lower limit of input voltage. (DCR of inductor : 20mΩ)
This data is the characteristic value, so it' doesn't guarantee the operation range,

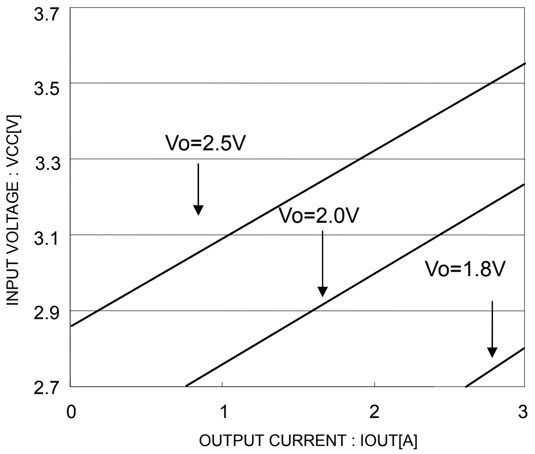

Fig.34 minimum input voltage in each output voltage

●BD9132MUV　Cautions on PC Board layout

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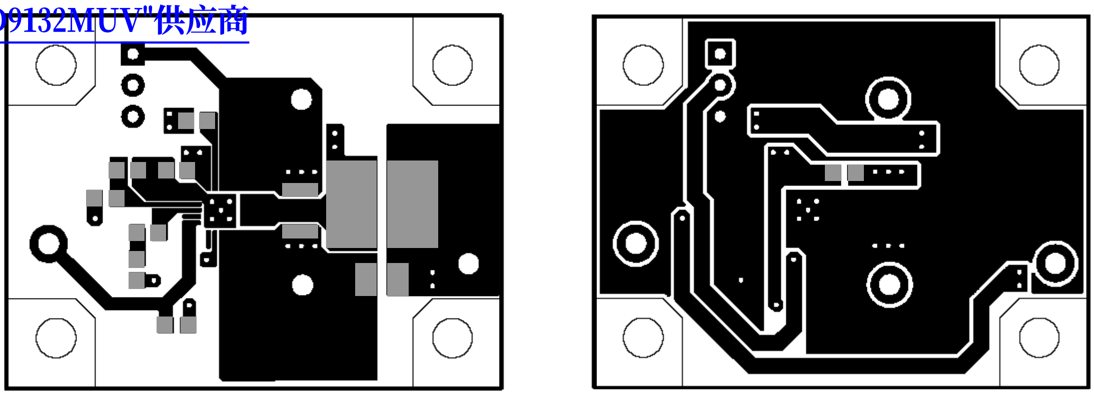

Fig.35 Layout diagram

① Lay out the input ceramic capacitor CIN closer to the pins PVCC and PGND, and the output capacitor Co closer to the pin PGND.

② Lay out CITH and RITH between the pins ITH and GND as neat as possible with least necessary wiring.

※ VQFN020V4040 (BD9132MUV) has thermal PAD on the reverse of the package.
The package thermal performance may be enhanced by bonding the PAD to GND plane which take a large area of PCB.

●Recommended components Lists on above application

Symbol	Part	Value		Manufacturer	Series
L	Coil	2.0uH		Sumida	CDR6D28MNP-2R0NC
		2.2uH		Sumida	CDR6D26NP-2R2NC
CIN	Ceramic capacitor	22uF		Murata	GRM32EB11A226KE20
Co	Ceramic capacitor	22uF		Murata	GRM31CB30J226KE18
CITH	Ceramic capacitor	VOUT=1.0V	1500pF	Murata	CRM18 Serise
		VOUT=1.2V	1000pF	Murata	GRM18 Serise
		VOUT=1.5V	1000pF	Murata	GRM18 Serise
		VOUT=1.8V	560pF	Murata	GRM18 Serise
		VOUT=2.5V	560pF	Murata	GRM18 Serise
		VOUT=3.3V	330pF	Murata	GRM18 Serise
RITH	Resistance	VOUT=1.0V	5.6kΩ	Rohm	MCR03 Serise
		VOUT=1.2V	6.8kΩ	Rohm	MCR03 Serise
		VOUT=1.5V	6.8kΩ	Rohm	MCR03 Serise
		VOUT=1.8V	8.2kΩ	Rohm	MCR03 Serise
		VOUT=2.5V	12kΩ	Rohm	MCR03 Serise
		VOUT=3.3V	15kΩ	Rohm	MCR03 Serise
Cf	Ceramic capacitor	1000 pF		Murata	GRM18 Serise
Rf	Resistance	10Ω		Rohm	MCR03 Serise
CBST	Ceramic capacitor	0.1 uF		Murata	GRM18 Serise

※The parts list presented above is an example of recommended parts. Although the parts are sound, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the VCC and PVCC pins, and a schottky barrier diode or snubber established between the SW and PGND pins.

●I/O equivalence circuit

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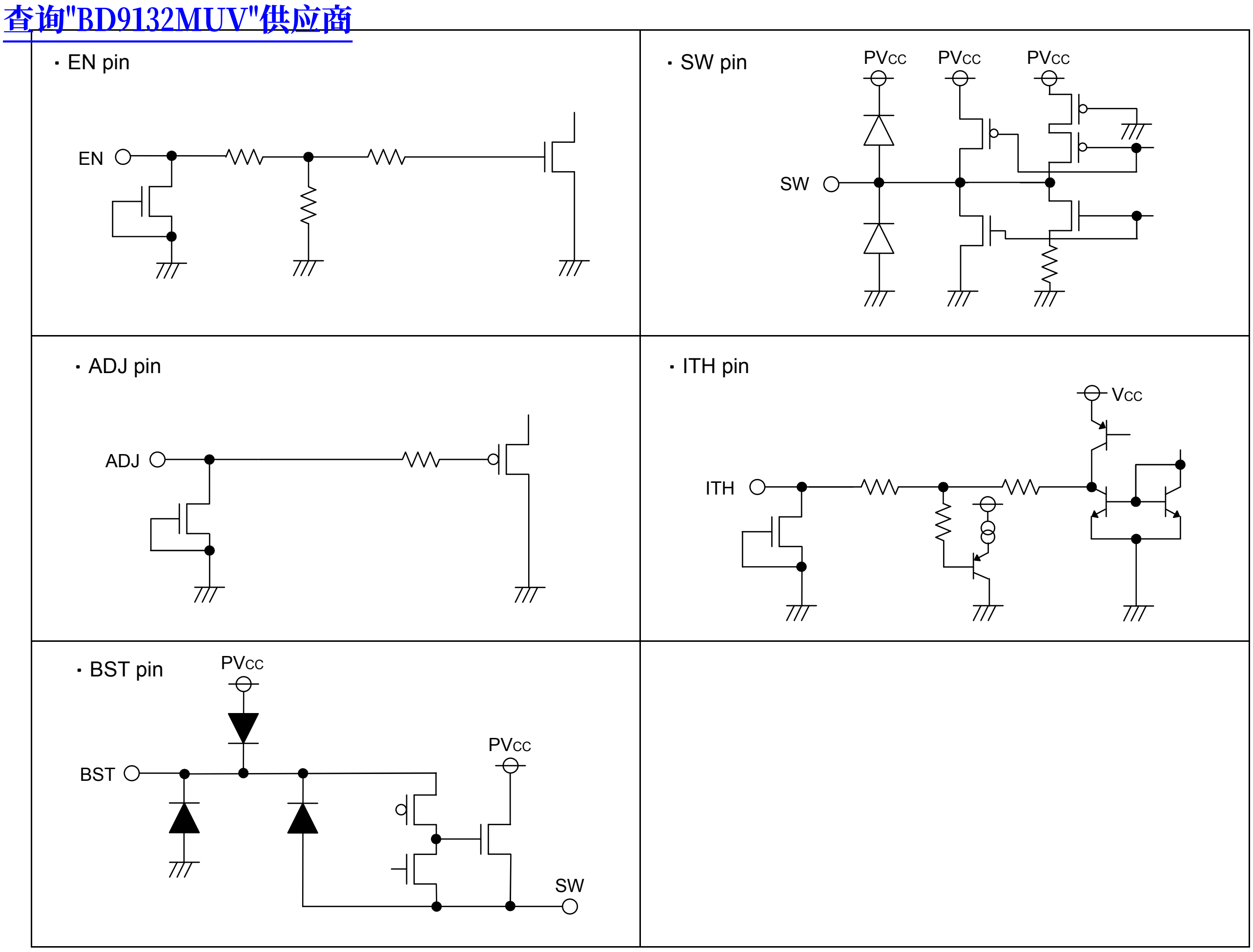

Fig.36 I/O equivalence circuit

●Cautions on use

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1. Absolute Maximum Ratings

While utmost care is taken to quality control of this product, any application that may exceed some of the absolute maximum ratings including the voltage applied and the operating temperature range may result in breakage. If broken, short-mode or open-mode may not be identified. So if it is expected to encounter with special mode that may exceed the absolute maximum ratings, it is requested to take necessary safety measures physically including insertion of fuses.

2. Electrical potential at GND

GND must be designed to have the lowest electrical potential In any operating conditions.

3. Short-circuiting between terminals, and mismounting

When mounting to pc board, care must be taken to avoid mistake in its orientation and alignment. Failure to do so may result in IC breakdown. Short-circuiting due to foreign matters entered between output terminals, or between output and power supply or GND may also cause breakdown.

4. Thermal shutdown protection circuit

Thermal shutdown protection circuit is the circuit designed to isolate the IC from thermal runaway, and not intended to protect and guarantee the IC. So, the IC the thermal shutdown protection circuit of which is once activated should not be used thereafter for any operation originally intended.

5. Inspection with the IC set to a pc board

If a capacitor must be connected to the pin of lower impedance during inspection with the IC set to a pc board, the capacitor must be discharged after each process to avoid stress to the IC. For electrostatic protection, provide proper grounding to assembling processes with special care taken in handling and storage. When connecting to jigs in the inspection process, be sure to turn OFF the power supply before it is connected and removed.

6. Input to IC terminals

This is a monolithic IC with P^+ isolation between P-substrate and each element as illustrated below. This P-layer and the N-layer of each element form a P-N junction, and various parasitic element are formed.

If a resistor is joined to a transistor terminal as shown in Fig 37.

○P-N junction works as a parasitic diode if the following relationship is satisfied; GND>Terminal A (at resistor side), or GND>Terminal B (at transistor side); and

○if GND>Terminal B (at NPN transistor side),

a parasitic NPN transistor is activated by N-layer of other element adjacent to the above-mentioned parasitic diode.

The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown. It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.

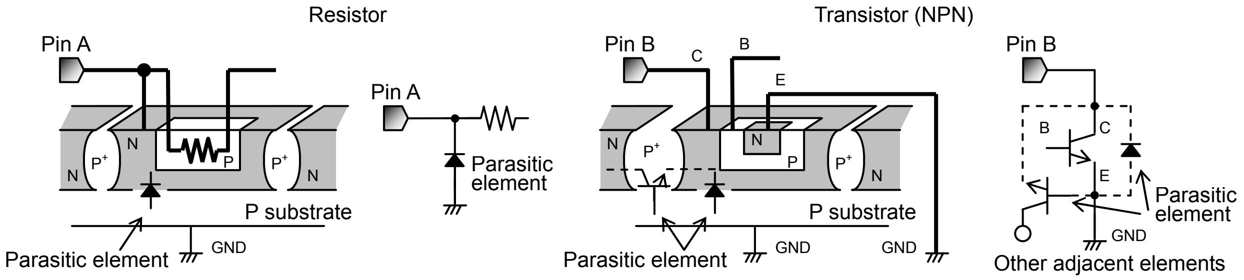

Fig.37 Simplified structure of monorisic IC

7. Ground wiring pattern

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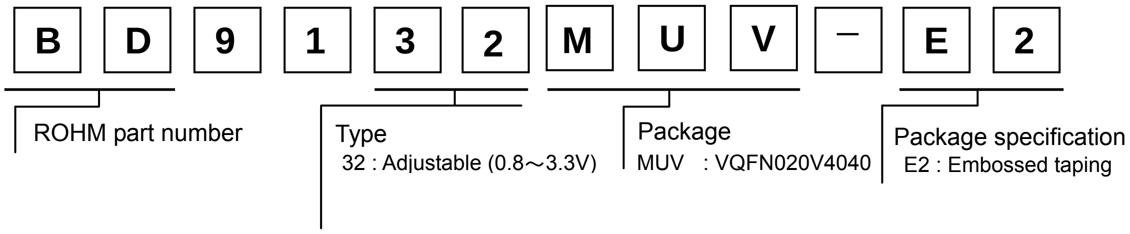
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

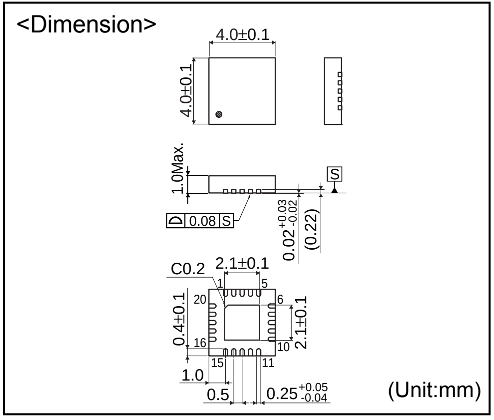
8 . Selection of inductor

It is recommended to use an inductor with a series resistance element (DCR) 0.1Ω or less. Especially, in case output voltage is set 1.6V or more, note that use of a high DCR inductor will cause an inductor loss, resulting in decreased output voltage. Should this condition continue for a specified period (soft start time + timer latch time), output short circuit protection will be activated and output will be latched OFF. When using an inductor over 0.1Ω, be careful to ensure adequate margins for variation between external devices and this IC, including transient as well as static characteristics. Furthermore, in any case, it is recommended to start up the output with EN after supply voltage is within operation range.

●Ordering part number

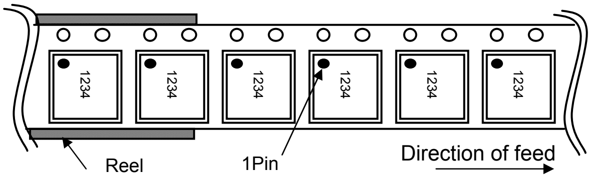


VQFN020V4040



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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