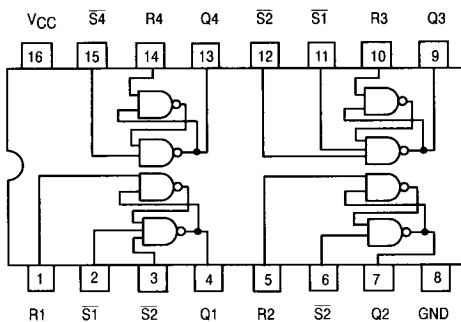


Quad Set-Reset Latch

ELECTRICALLY TESTED PER:
MIL-M-38510/31602

LOGIC DIAGRAM



TRUTH TABLE

Inputs			Output
S1	S2	R	(Q)
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
h = The output is HIGH as long as $\bar{S}1$ or $\bar{S}2$ is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

Military 54LS279



AVAILABLE AS:

- 1) JAN: JM38510/31602BXA
- 2) SMD: 7601801
- 3) 883: 54LS279/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

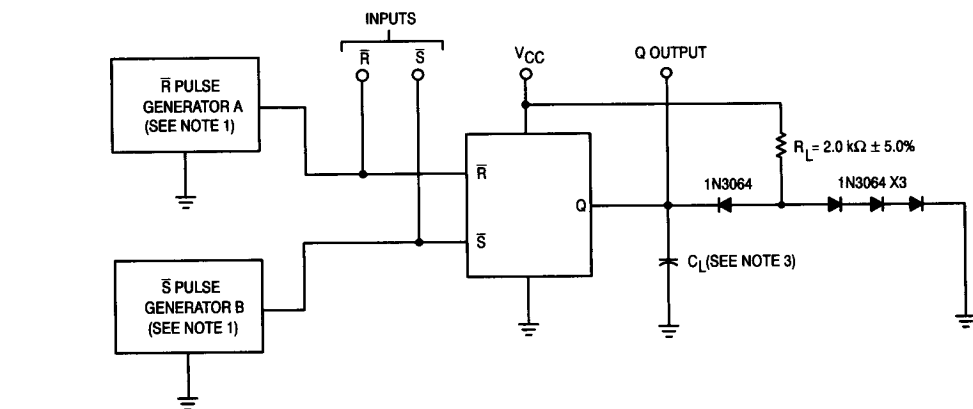
THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

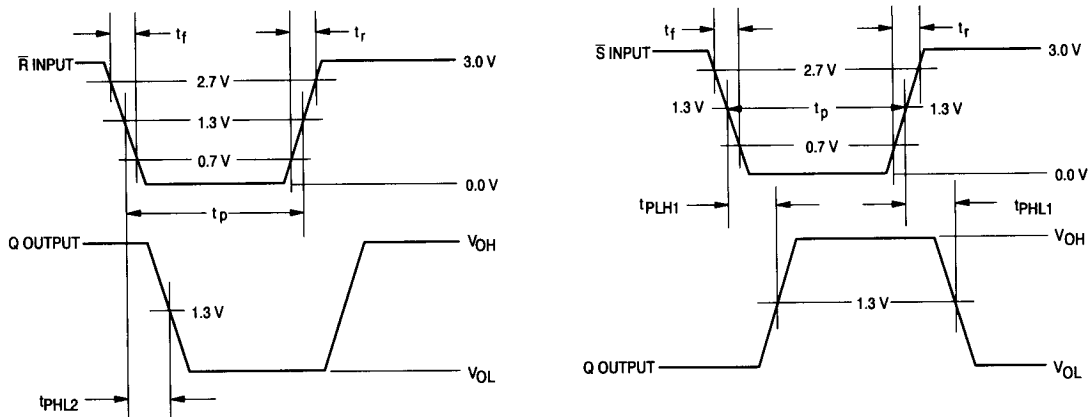
FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
R1	1	1	2	VCC
S1	2	2	3	GND
S2	3	3	4	GND
Q1	4	4	5	VCC
R2	5	5	7	VCC
S2	6	6	8	GND
Q2	7	7	9	VCC
GND	8	8	10	GND
Q3	9	9	12	VCC
R3	10	10	13	VCC
S1	11	11	14	GND
S2	12	12	15	GND
Q4	13	13	17	VCC
R4	14	14	18	VCC
S4	15	15	19	GND
VCC	16	16	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

SWITCHING TEST CIRCUIT



WAVEFORMS



NOTES:

1. $\bar{R}$ and $\bar{S}$ pulse generators have the following characteristics:
 $t_f \leq 15$ ns, $t_r \leq 6.0$ ns, $t_p = 40$ ns ± 10 ns, and $PRR \leq 1.0$ MHz.
2. Inputs not under test are at 2.7 V.
3. $C_L = 50$ pF $\pm 10\%$, which includes scope probe and jig capacitance.
4. $R_L = 2.0$ k Ω $\pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.
6. All diodes are 1N3064 or equivalent.

[查询"54LS279/BFAJC"供应商](#)

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = – 400 μA, V _{IH} = 2.0 V, other input = 2.0 V, or per truth table.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IH} = 2.0 V, other input = 2.0 V, or per truth table.
V _{IC}	Input Clamping Voltage		– 1.5					V	V _{CC} = 4.5 V, I _{IN} = – 18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open.
I _{IL}	Logical "0" Input Current	– 160	– 400	– 160	– 400	– 160	– 400	μA	V _{CC} = 5.5 V, V _{IN} = 0.4V, $\overline{S2}$ = GND, other inputs are open.
I _{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V _{CC} = 5.5 V, V _{IN} = 5.0 V, other inputs = GND, V _{OUT} = GND.
I _{CC}	Power Supply Current		7.0		7.0		7.0	mA	V _{CC} = 5.5 V, V _{IN} ($\overline{S1}$, $\overline{S2}$) = 4.5 V, other inputs are GND.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output S to Output	3.0 —	20 21	3.0 —	26 26	3.0 —	26 26	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PLH1} t _{PLH1}	Propagation Delay /Data-Output S to Output	3.0 —	27 22	3.0 —	35 30	3.0 —	35 30	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PHL2} t _{PHL2}	Propagation Delay /Data-Output R to Output	3.0 —	32 27	3.0 —	42 37	3.0 —	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.

NOTE:1. The limits specified for C_L = 15 pF are guaranteed but not tested.