

## Dual N-Channel 150-V (D-S) MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
150	0.105 at V <sub>GS</sub> = 10 V	4.1
	0.115 at V <sub>GS</sub> = 6 V	3.9

### FEATURES

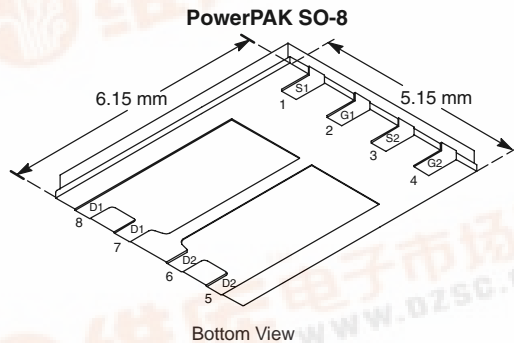
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET<sup>®</sup> Power MOSFET
- Low On-Resistance in New Low Thermal Resistance PowerPAK<sup>®</sup> Package
- Dual MOSFET for Space Savings
- 100 % R<sub>G</sub> Tested



**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**  
 Available

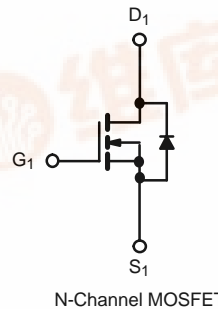
### APPLICATIONS

- High Efficiency Primary Side Switches
- Half Bridge and Forward Converters

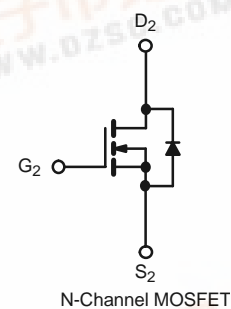


Bottom View

Ordering Information: Si7956DP-T1-E3 (Lead (Pb)-free)  
 Si7956DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V <sub>DS</sub>	150		V
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	4.1	2.6
		T <sub>A</sub> = 70 °C	3.3	2.1
Pulsed Drain Current	I <sub>DM</sub>	20		A
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	2.9	1.2	
Single Avalanche Current	L = 0.1 mH	I <sub>AS</sub>		mJ
Single Avalanche Energy	E <sub>AS</sub>	11		
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25 °C	3.5	1.4
		T <sub>A</sub> = 70 °C	2.2	0.9
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b,c</sup>		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	t ≤ 10 s	26	35
		Steady State	60	85
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	2.2	2.7	°C/W

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



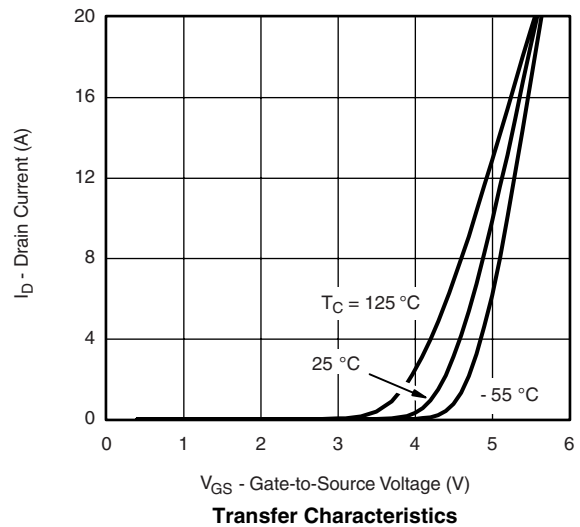
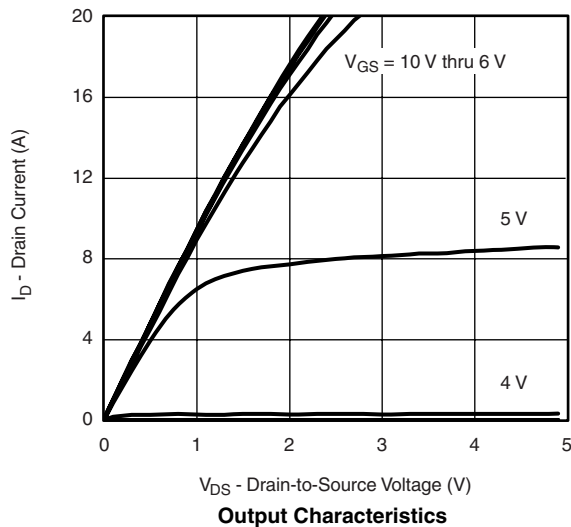
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3.1	4.0	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 4.1\text{ A}$		0.088	0.105	$\Omega$
		$V_{GS} = 6\text{ V}, I_D = 3.9\text{ A}$		0.096	0.115	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 4.1\text{ A}$		10		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.9\text{ A}, V_{GS} = 0\text{ V}$		0.77	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 4.1\text{ A}$		17	26	nC
Gate-Source Charge	$Q_{gs}$			3.9		
Gate-Drain Charge	$Q_{gd}$			5.5		
Gate Resistance	$R_g$		1	2	3	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 75\text{ V}, R_L = 75\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_G = 6\text{ }\Omega$		14	22	ns
Rise Time	$t_r$			13	22	
Turn-Off Delay Time	$t_{d(off)}$			36	58	
Fall Time	$t_f$			18	30	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 2.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		50	75	

Notes:

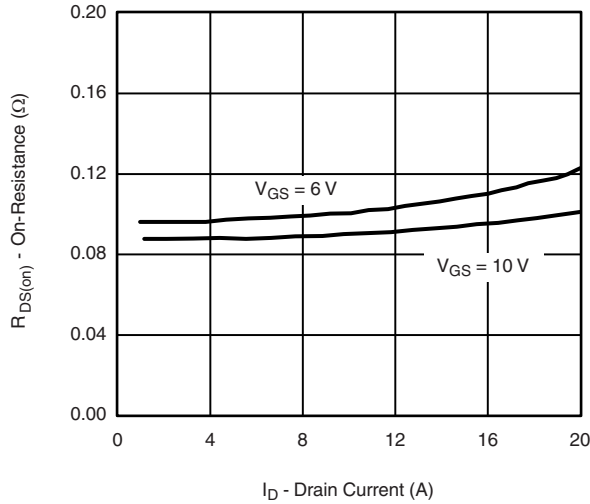
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

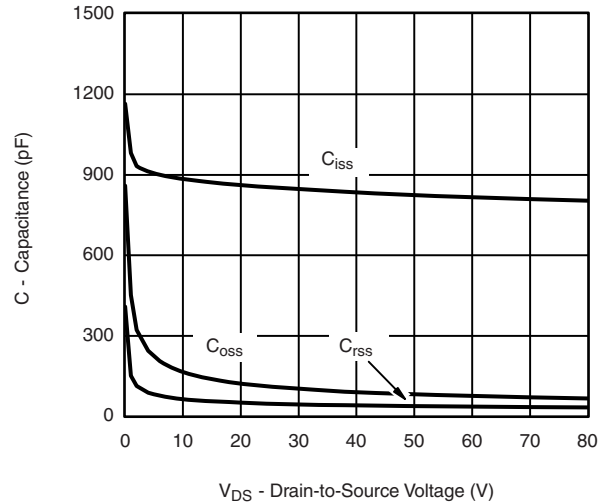
## TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$ , unless otherwise noted



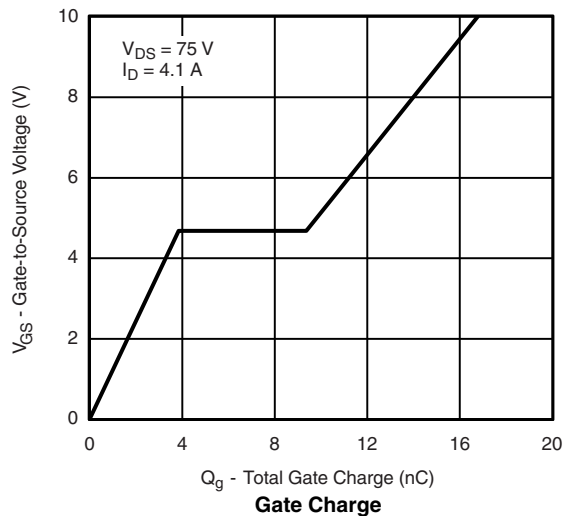
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



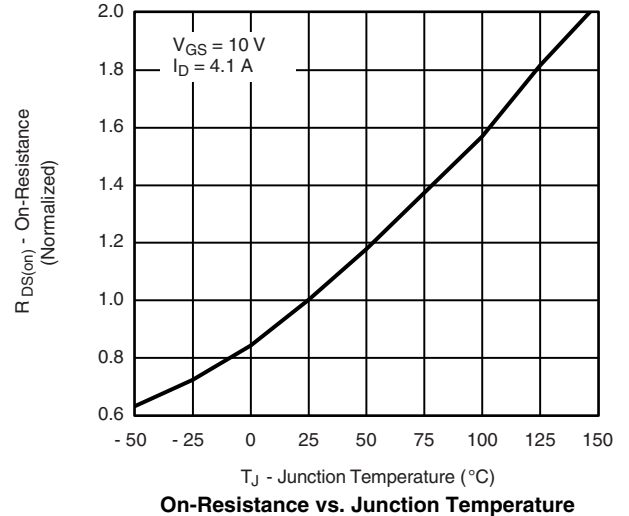
**On-Resistance vs. Drain Current**



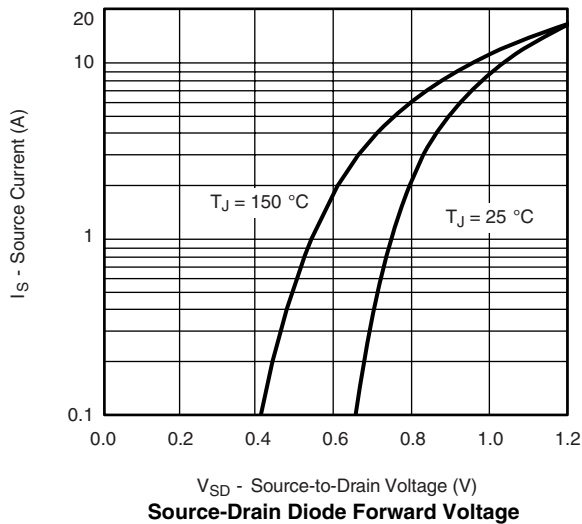
**Capacitance**



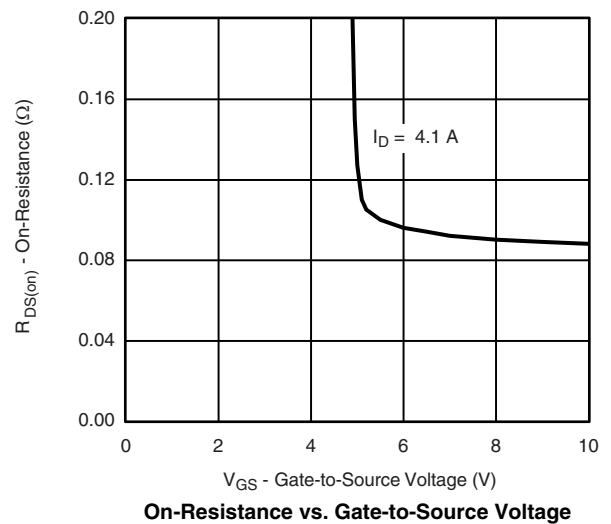
**Gate Charge**



**On-Resistance vs. Junction Temperature**

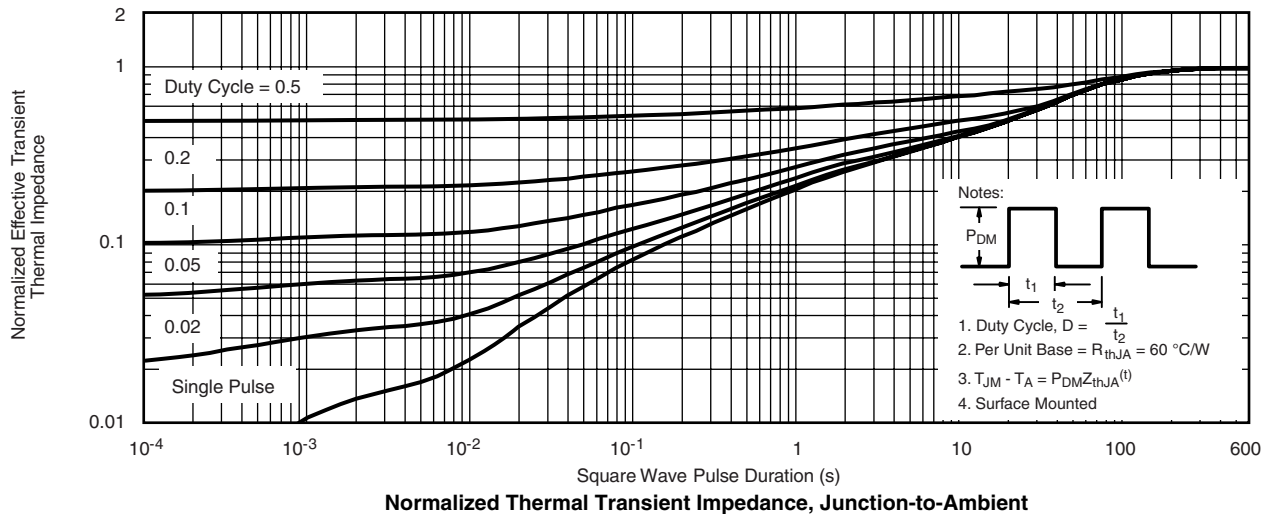
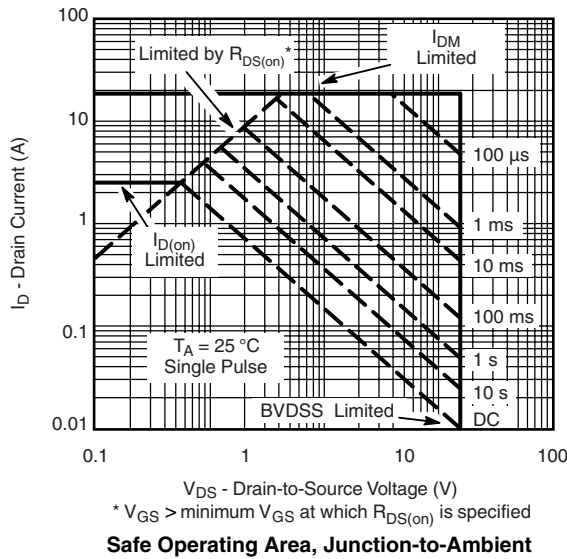
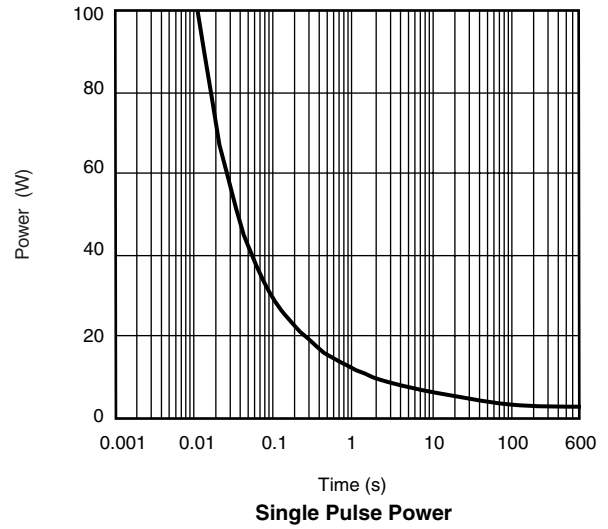
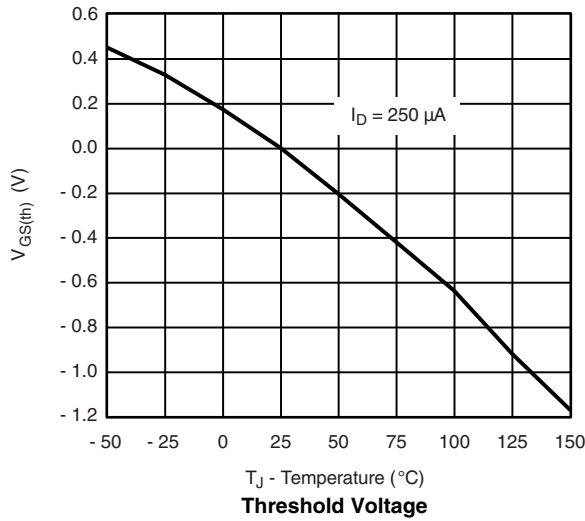


**Source-Drain Diode Forward Voltage**

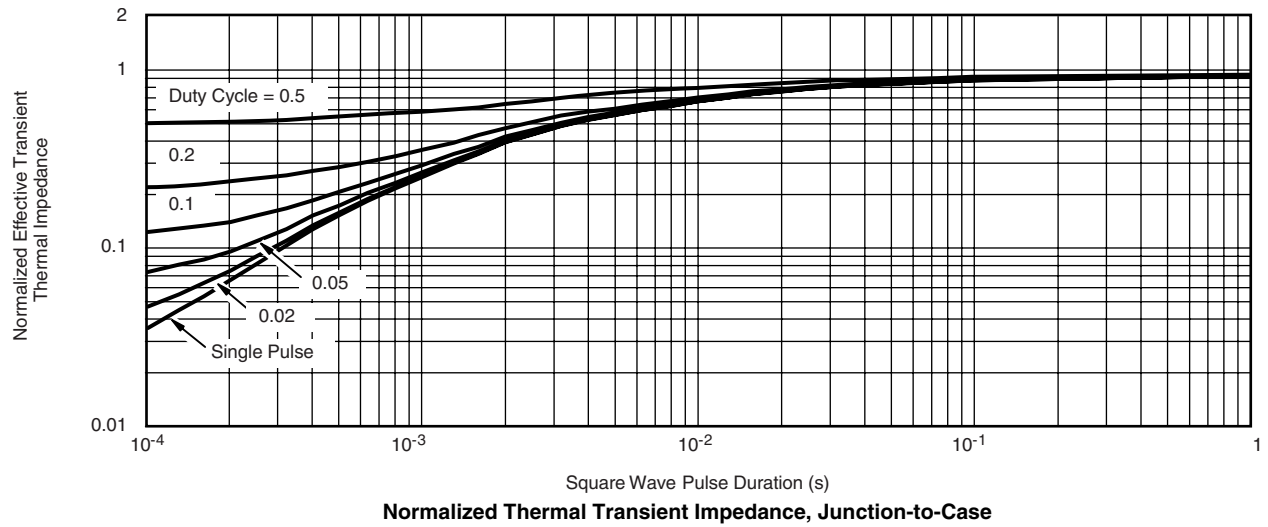


**On-Resistance vs. Gate-to-Source Voltage**

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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