19-4139; Rev 1; 8/08

Overvoltage-Protection Controllers with a Low RON Internal FET

General Description

The MAX4970/MAX4971/MAX4972 family of overvoltage protection devices features a low 40mΩ (typ) R_{ON} internal FET and protect low-voltage systems against voltage faults up to +28V. These devices also drive an optional external pFET to protect against reverse-polarity input voltages. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components.

All switches feature a 2.3A (min) current-limit protection. During a short-circuit occurrence, the device operates in an autoretry mode where the internal MOSFET is turned on to check if the fault has been removed. The autoretry interval time is 15ms, and if the fault is removed, the MOSFET remains on.

The MAX4970/MAX4971/MAX4972 feature an enable input ($\overline{EN}$) that controls the operation of the internal nFET as well as the optional external pFET. The use of $\overline{EN}$ allows the external pFET to block reverse voltages independent of any signal present at the output.

The overvoltage thresholds (OVLO) are preset to 4.65V (MAX4972), 5.8V (MAX4970), or 6.35V (MAX4971). The undervoltage thresholds (UVLO) are preset to 2.45V. When the input voltage drops below the UVLO, the devices enter a low-current standby mode.

All devices are offered in a small 12-bump, WLP package and operate over the -40°C to +85°C extended temperature range.

Applications

Cell Phones

Digital Still Cameras

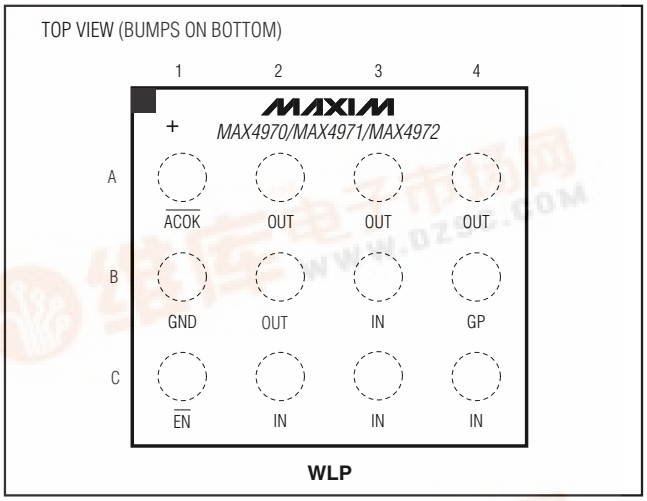
PDAs and Palmtop Devices

MP3 Players

Features

- **Input Voltage Protection up to +28V**
- **Integrated nFET Switch**
- **Reverse Voltage Protection with External pFET**
- **Enable Input**
- **Preset Overvoltage Protection Trip Level**
  - **5.8V (MAX4970)**
  - **6.35V (MAX4971)**
  - **4.65V (MAX4972)**
- **Low-Current Undervoltage-Lockout Mode**
- **Short-Circuit Protection (Autoretry)**
- **Internal 15ms Startup Delay and Retry Times**
- **Input-Voltage Power-Good Logic Output**
- **Thermal-Shutdown Protection**
- **2mm x 1.5mm, 12-Bump WLP Package**

Pin Configuration



WLP

Ordering Information/Selector Guide

PART	PIN-PACKAGE	TOP MARK	PACKAGE CODE	UVLO (V)	OVLO (V)	ACOK ACTION
MAX4970EWC+T	12 WLP	AAA	W121A2+1	2.45	5.8	UVLO only
MAX4971EWC+T	12 WLP	AAB	W121A2+1	2.45	6.35	UVLO only
MAX4972EWC+T	12 WLP	AAC	W121A2+1	2.45	4.65	UVLO and OVLO

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*
+Denotes a lead-free/RoHS-compliant package.
T = *Tape-and-reel package.*

Typical Operating Circuit appears at end of data sheet.

Overvoltage-Protection Controllers with a Low RON Internal FET

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
IN .....-0.3V to +30V
IN-GP .....(30V - 5.4V)
OUT .....-0.3V to +(IN + 0.3)V
$\overline{EN}$, $\overline{ACOK}$ .....-0.3V to +6V
GP .....-0.3V to +30V
Continuous Power Dissipation (T_A = +70°C) for
Multilayer Board:
12-Bump WLP (derate 8.5mW/°C above +70°C).....678mW
WLP Package Junction-to-Ambient Thermal
Resistance (θ_{JA}) (Note 1).....118°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +2.2V to +28V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			2.2		28	V
Input Supply Current	I_{IN}	$\overline{EN}$ = 0V, V_{IN} = 12V; GP clamp on	T_A = +25°C		176	230	µA
			T_A = T_{MIN} to T_{MAX}			250	
		$\overline{EN}$ = 0V, V_{IN} = 5V (MAX4970), V_{IN} = 5.5V (MAX4971), V_{IN} = 3.8V (MAX4972)	T_A = +25°C		60	107	
			T_A = T_{MIN} to T_{MAX}			150	
		$\overline{EN}$ = 1.4V			50	100	
UVLO Supply Current	I_{UVLO}	V_{IN} < V_{UVLO}; V_{IN} = 2.2V				40	µA
IN Undervoltage Lockout	V_{UVLO}	V_{IN} falling		2.20	2.45	2.65	V
		V_{IN} rising		2.25	2.5	2.7	
IN Undervoltage Lockout Hysteresis					1		%
Overvoltage Trip Level	V_{OVLO}	V_{IN} rising	MAX4970	5.6	5.9	6.2	V
			MAX4971	6.0	6.4	6.8	
			MAX4972	4.35	4.70	5.05	
		V_{IN} falling	MAX4970	5.50	5.80	6.15	
			MAX4971	6.00	6.35	6.70	
			MAX4972	4.30	4.65	5.00	
IN Overvoltage Lockout Hysteresis					1		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +2.2V to +28V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch On-Resistance	R_{ON}	V_{IN} = 5V (MAX4970), V_{IN} = 5.5V (MAX4971), V_{IN} = 3.8V (MAX4972); I_{OUT} = 400mA		40	90	mΩ
Overcurrent Protection Threshold	I_{LIM}	V_{IN} = 5V (MAX4970), V_{IN} = 5.5V (MAX4971), V_{IN} = 3.8V (MAX4972)	2.30	3.36		A
GP Clamp Voltage	V_{GPC}	V_{IN} - V_{GP}, V_{IN} up to 28V	5.4	7.0	8.5	V
GP Pulldown Resistor	R_{GPPD}	$\overline{EN}$ = low, V_{GP} = V_{IN} = 5V (MAX4970), V_{GP} = V_{IN} = 5.5V (MAX4971), V_{GP} = V_{IN} = 3.8V (MAX4972)	16	36	54	kΩ
GP Pullup Resistor to IN	R_{GPPU}	$\overline{EN}$ = high, V_{IN} = 5V	9	15	25	kΩ
$\overline{EN}$ Input-Voltage High	V_{IH}		1.4			V
$\overline{EN}$ Input-Voltage Low	V_{IL}				0.4	V
$\overline{EN}$ Input Leakage Current	I_{EN}	$V_{\overline{EN}}$ = 5V			1	µA
$\overline{ACOK}$ Output-Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
$\overline{ACOK}$ High Leakage Current		$V_{\overline{ACOK}}$ = 5.5V, $\overline{ACOK}$ deasserted			1	µA
Thermal Shutdown				+150		°C
Thermal-Shutdown Hysteresis				40		°C
Maximum Output Capacitance	C_{OUT}				1000	µF
TIMING CHARACTERISTICS (Figure 1)						
Debounce Time	t_{INDBC}	Time from V_{UVLO} < V_{IN} < V_{OVLO}, R_{LOAD} = 100Ω, C_{LOAD} = 1µF to charge-pump enable		15		ms
Switch Turn-On Time	t_{ON}	V_{UVLO} < V_{IN} < V_{OVLO}, R_{LOAD} = 100Ω, C_{LOAD} = 1µF from $\overline{EN}$ low to 90% of V_{OUT}		13		ms
$\overline{ACOK}$ Assertion Time	$t_{\overline{ACOK}}$	V_{UVLO} < V_{IN} to $\overline{ACOK}$ low (MAX4970/MAX4971)		15		ms
		V_{UVLO} < V_{IN} < V_{OVLO} to $\overline{ACOK}$ low (MAX4972)				
Switch Turn-Off Time	t_{OFF}	V_{IN} < V_{UVLO} to internal switch off		4	8	µs
		V_{IN} > V_{OVLO} to internal switch off, R_{LOAD} = 100Ω		5	11	
Current Limit Turn-Off Time	t_{BLANK}	Overcurrent fault to internal switch off		10		µs
Autoretry Time	t_{RETRY}	From overcurrent fault to internal switch turn-on, Figure 2		15		ms

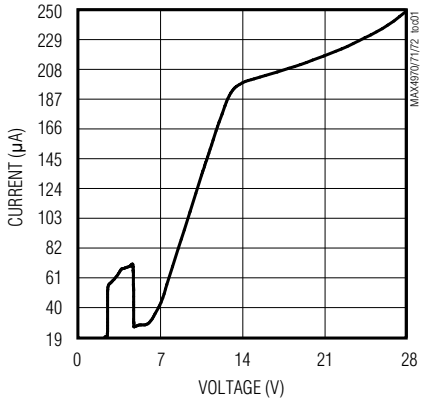
Note 2: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. Specifications are over -40°C to +85°C and are guaranteed by design.

Overvoltage-Protection Controllers with a Low RON Internal FET

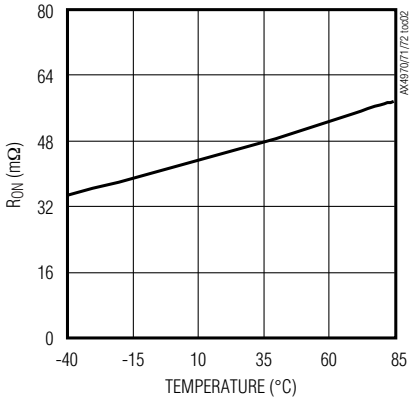
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

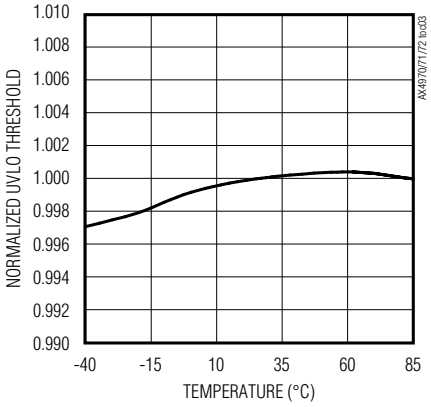
SUPPLY CURRENT vs. SUPPLY VOLTAGE



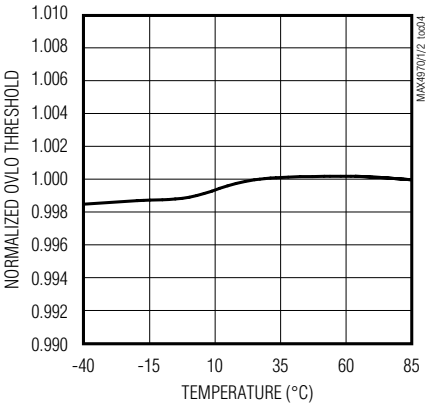
RON vs. TEMPERATURE



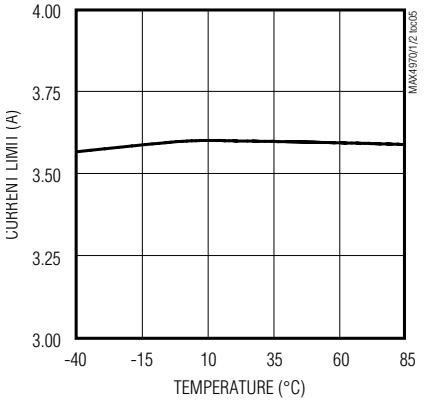
NORMALIZED UVLO THRESHOLD vs. TEMPERATURE



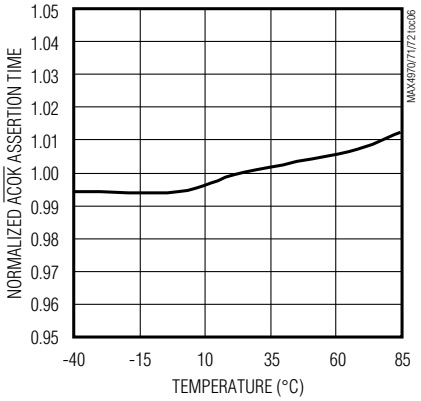
NORMALIZED OVLO THRESHOLD vs. TEMPERATURE



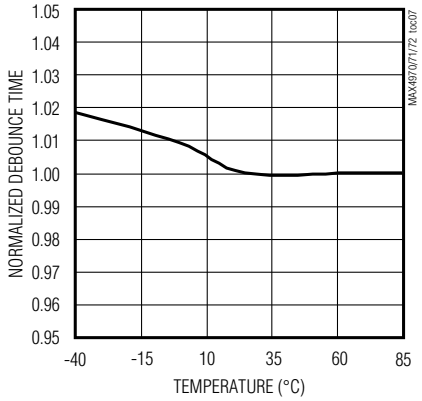
CURRENT LIMIT vs. TEMPERATURE



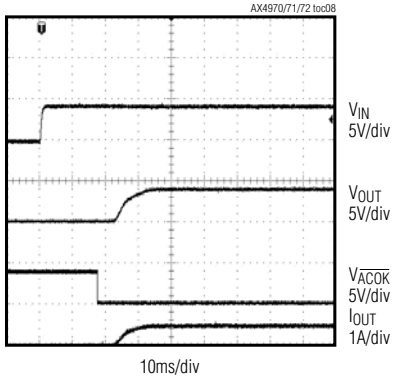
NORMALIZED $\overline{ACOK}$ ASSERTION TIME vs. TEMPERATURE



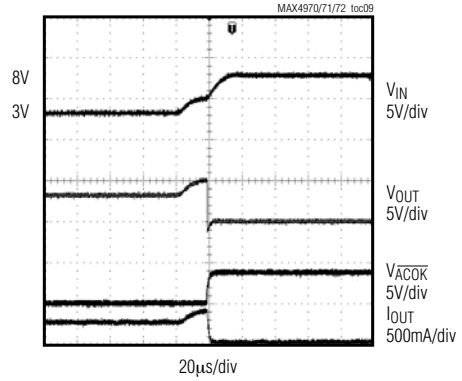
NORMALIZED DEBOUNCE TIME vs. TEMPERATURE



POWER-UP RESPONSE



OVERVOLTAGE FAULT RESPONSE

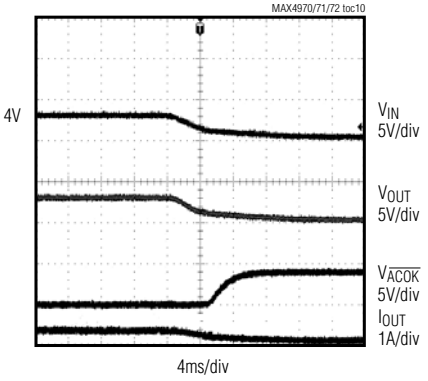


Overvoltage-Protection Controllers with a Low RON Internal FET

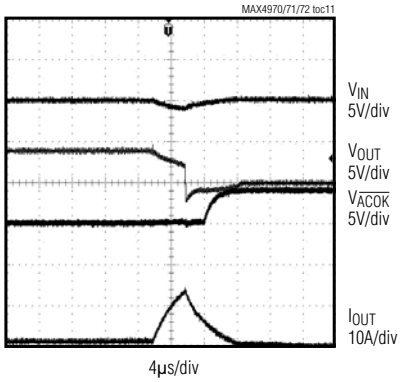
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

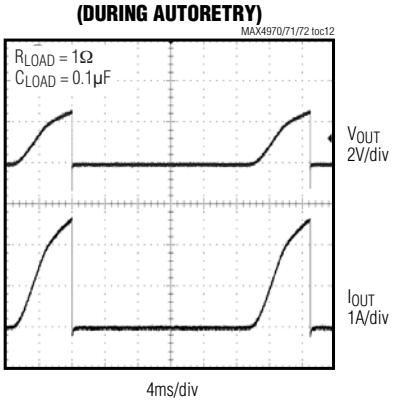
UNDERVOLTAGE FAULT RESPONSE



SHORT-CIRCUIT FAULT RESPONSE



OVERCURRENT DURATION TIME (DURING AUTORETRY)

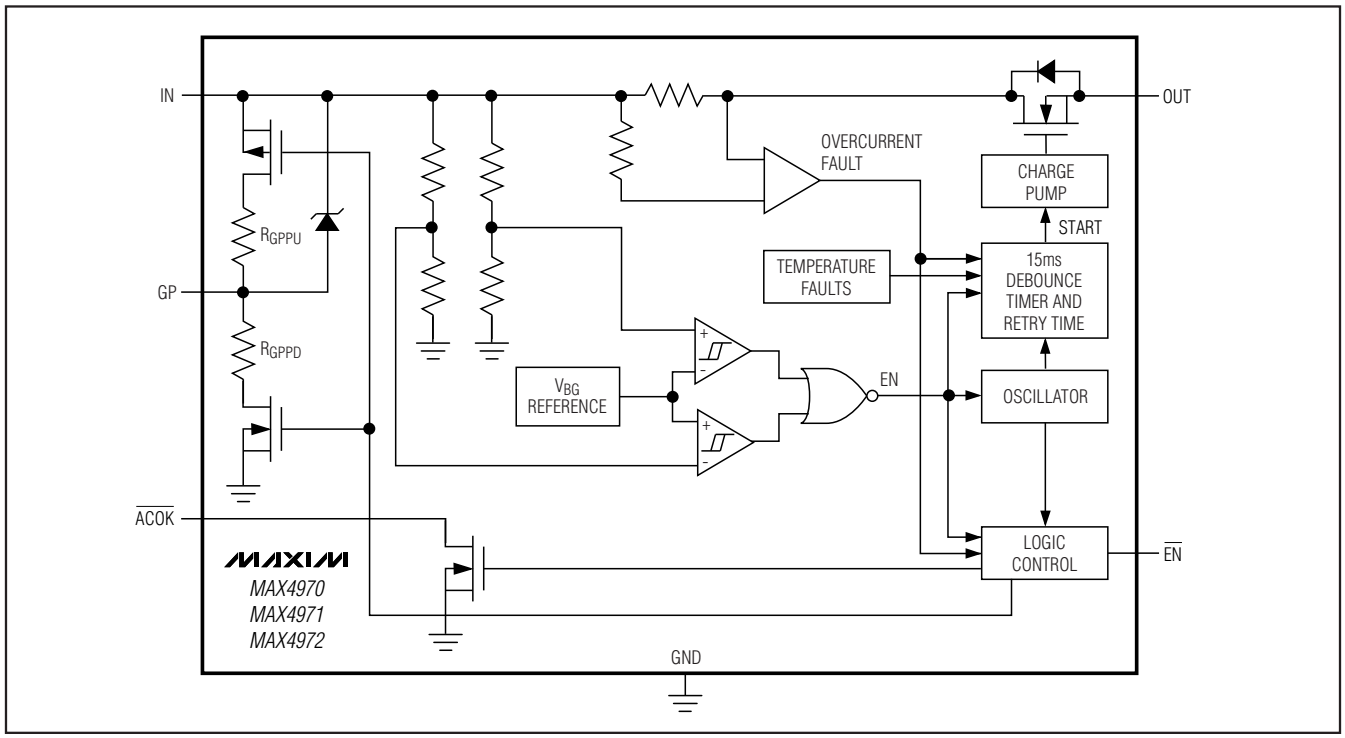


Pin Description

PIN	NAME	FUNCTION
A1	$\overline{ACOK}$	Active-Low Open-Drain Adapter-Voltage Indicator Output. $\overline{ACOK}$ is driven low after the adapter voltage is stable between UVLO and OVLO for 15ms (typ) (MAX4972), or after the adapter voltage is stable and greater than UVLO for 15ms (typ) (MAX4970/MAX4971). Connect a pullup resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system.
A2, A3, A4, B2	OUT	Output Voltage. Output of the internal switch. Connect all the OUT outputs together for proper operation.
B1	GND	Ground
B3, C2, C3, C4	IN	Voltage Input. Bypass IN with a 1µF ceramic capacitor as close as possible to the device to obtain ±15kV Human Body Model (HBM) ESD protection. No capacitor is required for ±2kV (HBM) ESD protection. Connect all the IN inputs together for proper operation.
B4	GP	External pFET Gate-Drive Output. GP pulls the external pFET gate down when the input is above UVLO and when $\overline{EN}$ is active (low).
C1	$\overline{EN}$	Enable Input. Drive $\overline{EN}$ low to turn GP pulldown on, GP pullup off, and to turn on the charge pump. Drive $\overline{EN}$ high to turn off the device.

Overvoltage-Protection Controllers with a Low RON Internal FET

Functional Diagram



Detailed Description

The MAX4970/MAX4971/MAX4972 overvoltage protection devices feature a low R_{ON} internal FET and protect low-voltage systems against voltage faults up to +28V. If the input voltage exceeds the overvoltage threshold, the internal MOSFET is turned off to prevent damage to the protected components. These devices also drive an optional external pFET to protect against reverse-polarity input voltages. The 15ms debounce time prevents false turn-on of the internal nFET during startup.

Device Operation

The MAX4970/MAX4971/MAX4972 have timing logic that control the turn-on of the internal nFET. The timing logic controls the turn-on of the charge pump and the state of the open-drain $\overline{ACOK}$ output. If $V_{IN} < V_{UVLO}$ or if $V_{IN} > V_{OVLO}$, the timing logic disables the charge pump. If $V_{UVLO} < V_{IN} < V_{OVLO}$, the internal charge pump is enabled. The charge-pump startup, after a 15ms debounce delay, turns on the internal nFET (see the *Functional Diagram*). $\overline{ACOK}$ is high impedance during startup until the $\overline{ACOK}$ 15ms debounce period expires. At this point, the device is in its on state. At any time, if V_{IN} drops below V_{UVLO} or rises above V_{OVLO}, the charge pump is disabled.

Internal nFET

The MAX4970/MAX4971/MAX4972 incorporate an internal nFET with a 40mΩ (typ) R_{ON}. The nFET is internally driven by a charge pump that generates a 5V voltage above IN. The internal nFET is equipped with 2.3A (min) current-limit protection that turns off the nFET within 10µs (typ) during an overcurrent fault condition.

Autoretry

The MAX4970/MAX4971/MAX4972 have an overcurrent autoretry function that turns on the nFET again after a 15ms (typ) retry time (see Figure 2). The fast turn-off time and 15ms retry time result in a very low duty cycle to keep power consumption low. If the faulty load condition is not present, the nFET remains on.

GP gate Drive

The GP gate drive is controlled by internal logic and by the $\overline{EN}$ input. When $\overline{EN}$ is high, the internal pullup between GP and IN is active, thus disabling the external pFET, and the load is protected against negative voltages down to the voltage rating of the external pFET. When $\overline{EN}$ is active (low), and the input voltage at IN is above the UVLO threshold, the pulldown between GP and IN is active, thus enabling the external pFET.

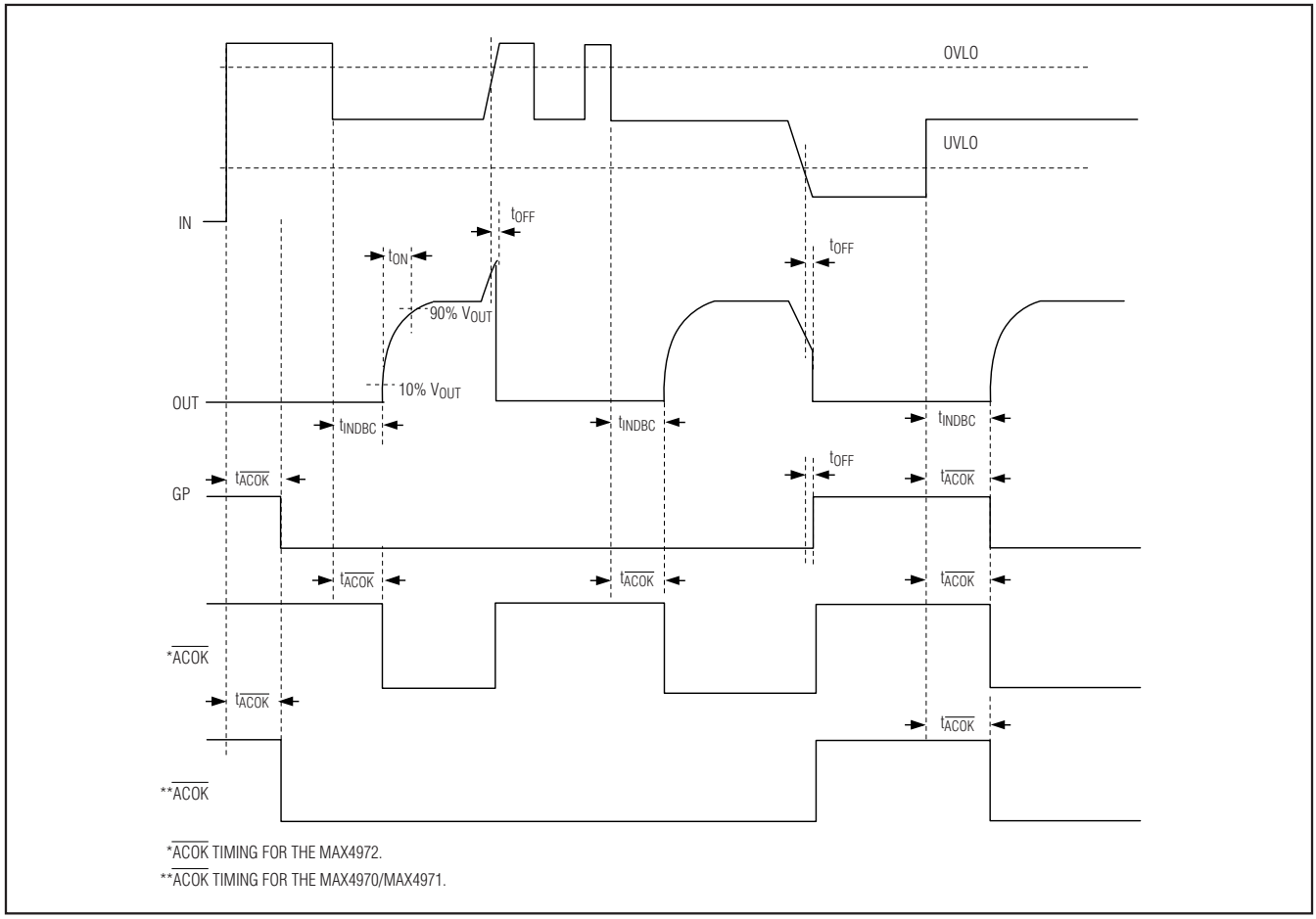


Figure 1. MAX4970/MAX4971/MAX4972 Timing Diagram

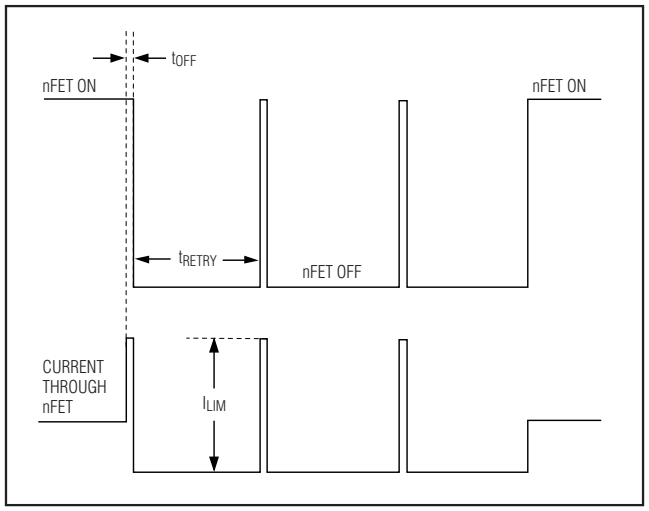


Figure 2. Autoretry Timing Diagram

Note that the UVLO threshold is measured at IN, but the input voltage is applied at the drain of the external pFET. The body diode of the external pFET adds to the UVLO threshold increasing its value to $V_{BODYDIODE}$ + V_{UVLO}. The internal clamp diode limits the gate to source voltage on the external pFET to 7.0V (typ) for protection of the pFET during an overvoltage fault.

Undervoltage Lockout (UVLO)

The MAX4970/MAX4971/MAX4972 have a 2.45V undervoltage-lockout threshold (UVLO). When V_{IN} is less than V_{UVLO}, $\overline{ACOK}$ is high impedance.

Overvoltage Lockout (OVLO)

The MAX4970 has a 5.8V (typ) overvoltage threshold (OVLO), the MAX4971 has a 6.35V (typ) OVLO threshold, and the MAX4972 has a 4.65V (typ) OVLO threshold. When V_{IN} is greater than V_{OVLO}, $\overline{ACOK}$ is high impedance for the MAX4972.

Overvoltage-Protection Controllers with a Low RON Internal FET

ACOK

ACOK is an active-low, open-drain output that asserts low when $V_{UVLO} < V_{IN} < V_{OVLO}$ for 15ms (typ) for the MAX4972. ACOK asserts low when $V_{IN} > V_{UVLO}$ for 15ms (typ) for the MAX4970 and MAX4971. Connect a pullup resistor from ACOK to the logic I/O voltage of the host system. During a short-circuit fault, ACOK may deassert due to V_{IN} dropping below V_{UVLO} from high current.

Thermal-Shutdown Protection

The MAX4970/MAX4971/MAX4972 feature thermal-shutdown circuitry. The internal nFET turns off when the junction temperature exceeds +150°C (typ). The device exits thermal shutdown after the junction temperature cools by 40°C (typ).

Applications Information

Reverse Polarity Protection

The optional external p-channel MOSFET can provide reverse polarity protection down to the voltage rating of the pFET.

IN Bypass Capacitor

For most applications, bypass IN to GND with a 1µF ceramic capacitor as close as possible to the device to enable ±15kV (HBM) ESD protection on the pin. If the external pFET is used, the 1uF capacitor must be connected between the drain and ground. If ±15kV (HBM) ESD is not required, there is no capacitor required at IN. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the +30V absolute maximum rating on IN.

OUT Output Capacitor

The slow turn-on time provides a soft-start function that allows the MAX4970/MAX4971/MAX4972 to charge an output capacitor up to 1000µF without turning off due to an overcurrent condition.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4970/MAX4971/MAX4972 are specified for ±15kV (HBM) typical ESD resistance on IN when IN is bypassed to ground with a 1µF ceramic capacitor.

HBM ESD Protection

Figure 3 shows the Human Body Model, and Figure 4 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

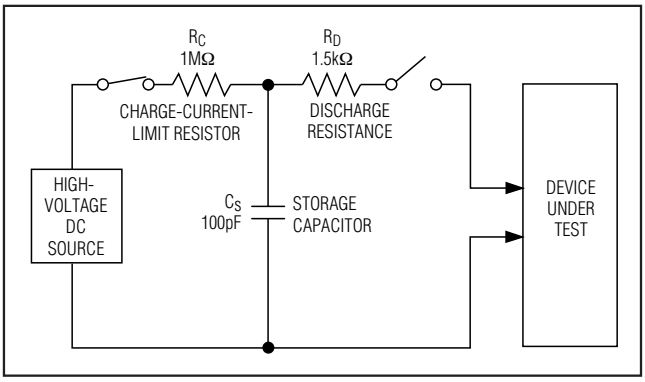


Figure 3. Human Body ESD Test Model

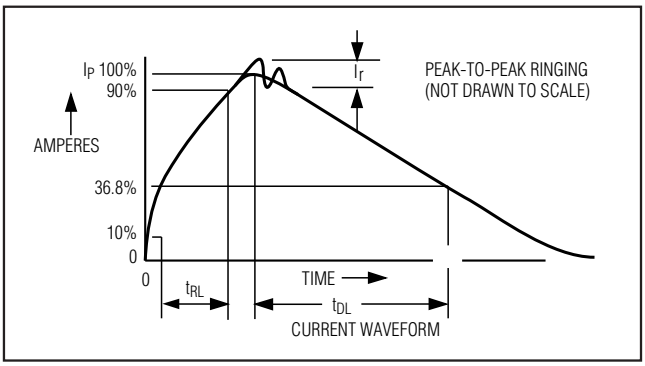
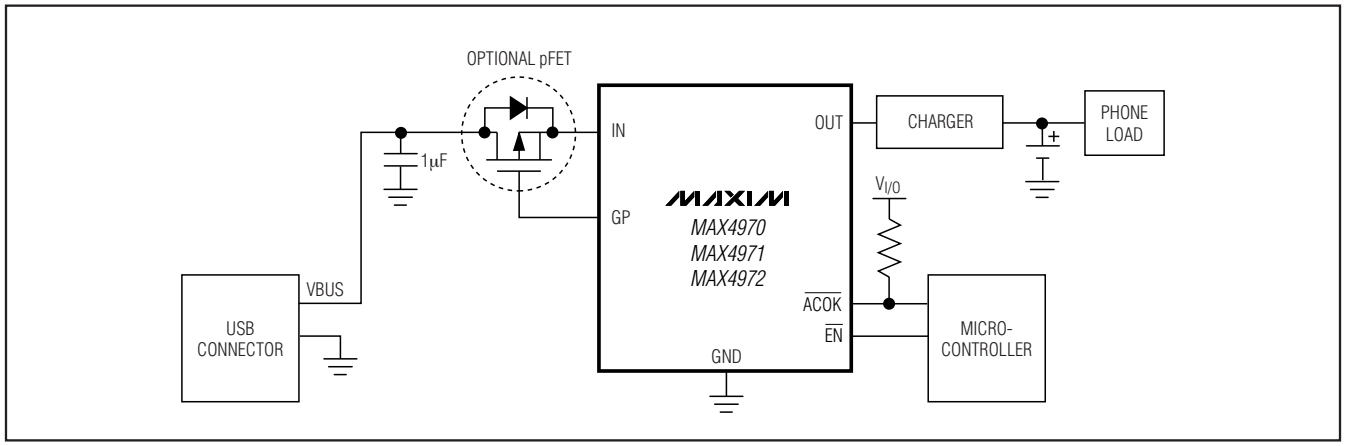


Figure 4. Human Body Current Waveform

Overvoltage-Protection Controllers with a Low RON Internal FET

Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
12 WLP	W121A2+1	**21-0009**