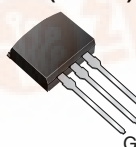


Power MOSFET

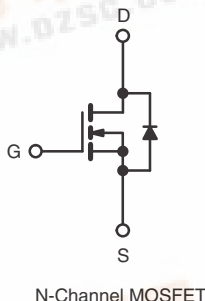
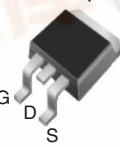
PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.85
Q_g (Max.) (nC)	39	
Q_{gs} (nC)	10	
Q_{gd} (nC)	19	
Configuration	Single	

I²PAK (TO-262)



D²PAK (TO-263)



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V V_{GS} Rating
- Reduced C_{iss} , C_{oss} , C_{rss}
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge than conventional Power MOSFETs. Utilizing the new LCDMOS (low charge device Power MOSFETs) technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge Power MOSFETs.

These device improvements combined with the proven ruggedness and reliability that characterize Power MOSFETs offer the designer a new power transistor standard for switching applications.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF840LCS-GE3	-	SiHF840LCL-GE3
Lead (Pb)-free	IRF840LCS-PbF	-	IRF840LCL-PbF
	SiHF840LCS-E3	-	SiHF840LCL-E3
SnPb	IRF840LCS	IRF840LCSTR ^a	IRF840LCL
	SiHF840LCS	SiHF840LCSTR ^a	SiHF840LCL

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^{a, e}	I_{DM}	28	
Linear Derating Factor		1.0	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^{b, e}	E_{AS}	510	mJ
Avalanche Current ^a	I_{AR}	8.0	A
Repetitive Avalanche Energy ^a	E_{AR}	13	mJ
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	W
		$T_A = 25^\circ\text{C}$	
Peak Diode Recovery dV/dt ^e	dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Starting $T_J = 25^\circ\text{C}$, $L = 14$ mH, $R_g = 25\ \Omega$, $I_{AS} = 8.0$ A (see fig. 12).

c. $I_{SD} \leq 8.0$ A, $dI/dt \leq 100$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.

d. 1.6 mm from case.

e. Uses IRF840LC, SiHF840LC data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply



IRF840LCS, IRF840LCL, SiHF840LCS, SiHF840LCL



Vishay Siliconix IRF840LCL, SiHF840LCS, SiHF840LCL"供应商

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, Steady-State) ^a	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^c		-	0.63	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.8 A ^b	-	-	0.85	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 4.8 A ^b		4.0	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^c		-	1100	-	pF
Output Capacitance	C _{oss}			-	170	-	
Reverse Transfer Capacitance	C _{rss}			-	18	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 8.0 A, V _{DS} = 400 V, see fig. 6 and 13 ^{b, c}	-	-	39	nC
Gate-Source Charge	Q _{gs}			-	-	10	
Gate-Drain Charge	Q _{gd}			-	-	19	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 8.0 A, R _g = 9.1 Ω, R _D = 30 Ω, see fig. 10 ^{b, c}		-	12	-	ns
Rise Time	t _r			-	25	-	
Turn-Off Delay Time	t _{d(off)}			-	27	-	
Fall Time	t _f			-	19	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	8.0	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	28	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 8.0 A, V _{GS} = 0 V ^b		-	-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 8.0 A, dI/dt = 100 A/μs ^{b, c}		-	490	740	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	3.0	4.5	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- Uses SiHF840LC data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

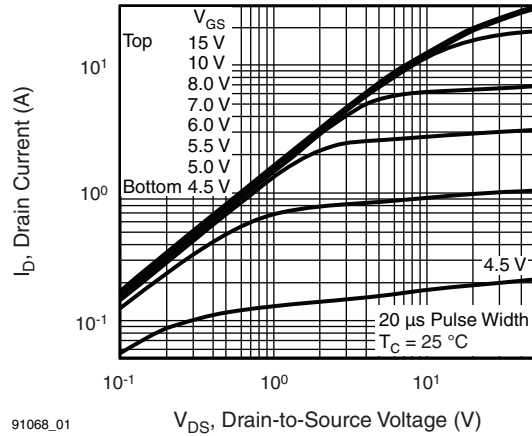


Fig. 1 - Typical Output Characteristics

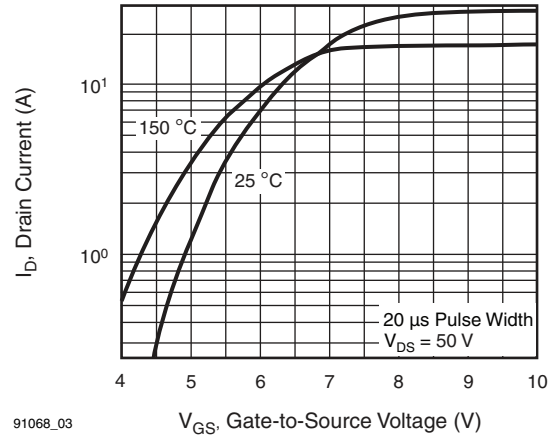


Fig. 3 - Typical Transfer Characteristics

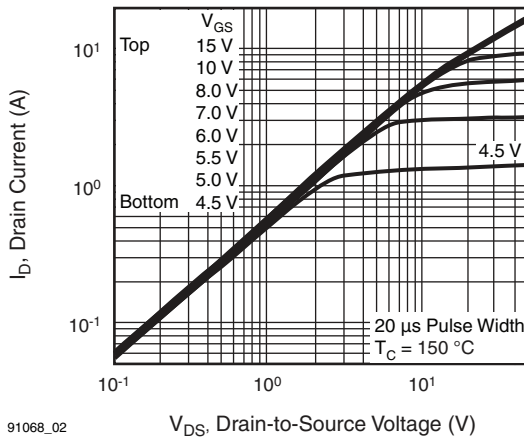


Fig. 2 - Typical Output Characteristics

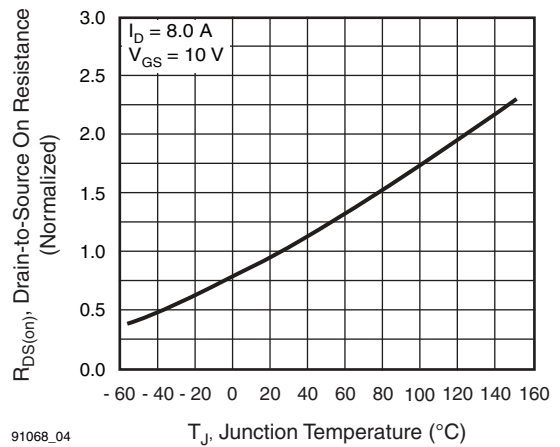


Fig. 4 - Normalized On-Resistance vs. Temperature

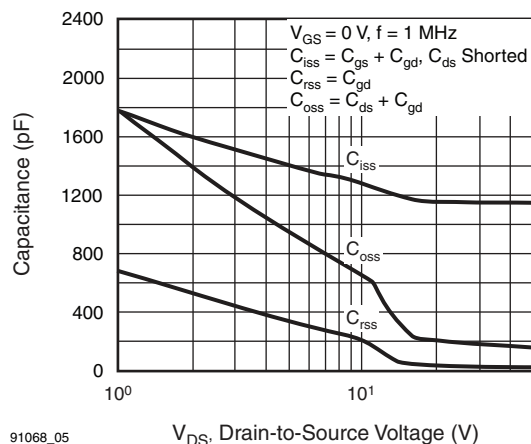


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

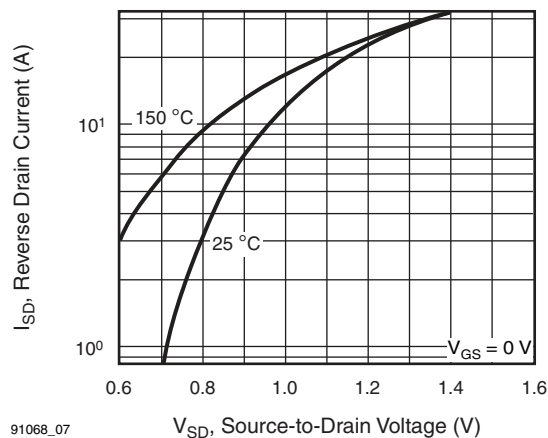


Fig. 7 - Typical Source-Drain Diode Forward Voltage

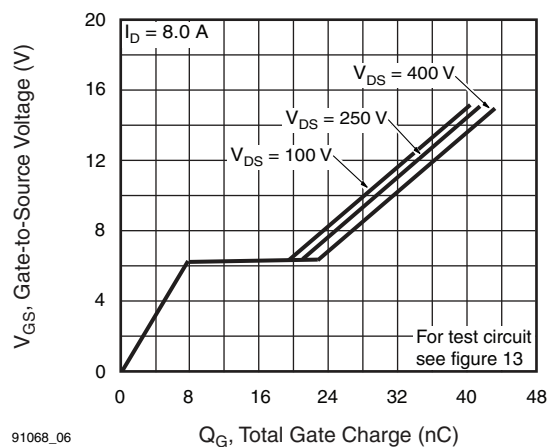


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

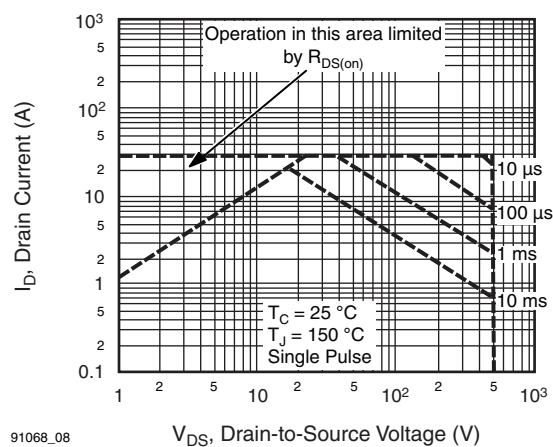
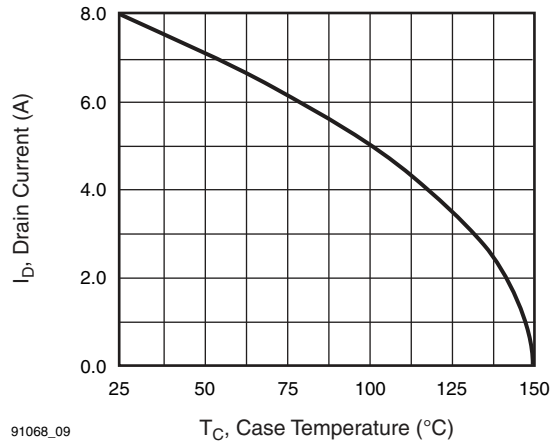


Fig. 8 - Maximum Safe Operating Area



91068_09

Fig. 9 - Maximum Drain Current vs. Case Temperature

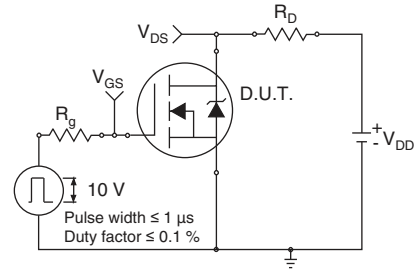


Fig. 10a - Switching Time Test Circuit

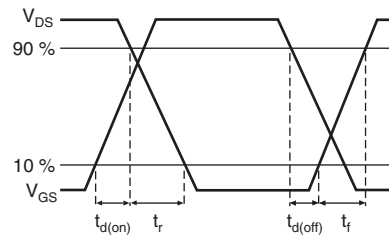
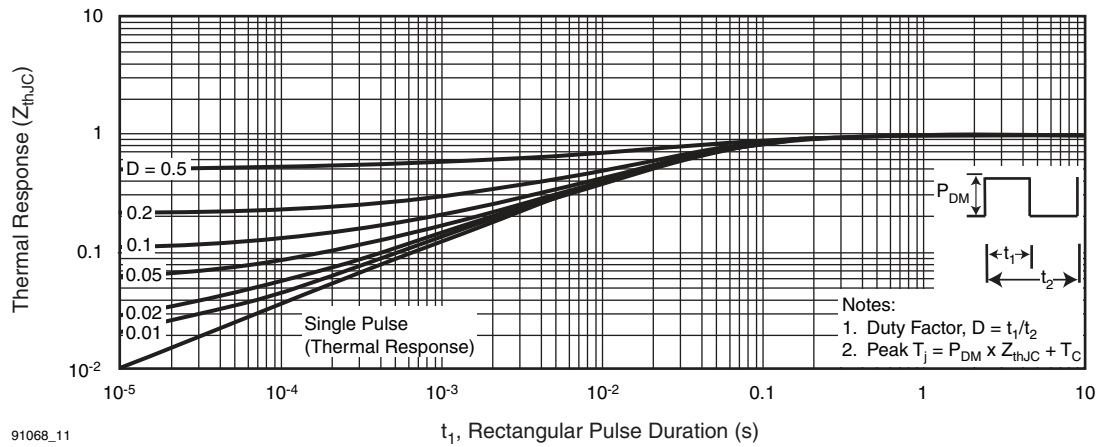


Fig. 10b - Switching Time Waveforms



91068_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

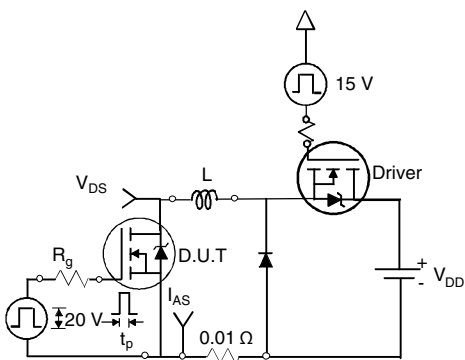


Fig. 12a - Unclamped Inductive Test Circuit

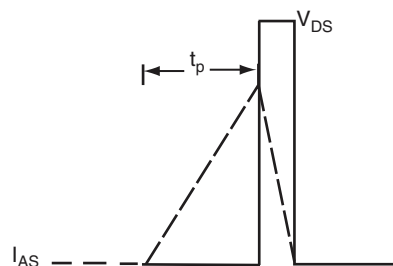


Fig. 12b - Unclamped Inductive Waveforms

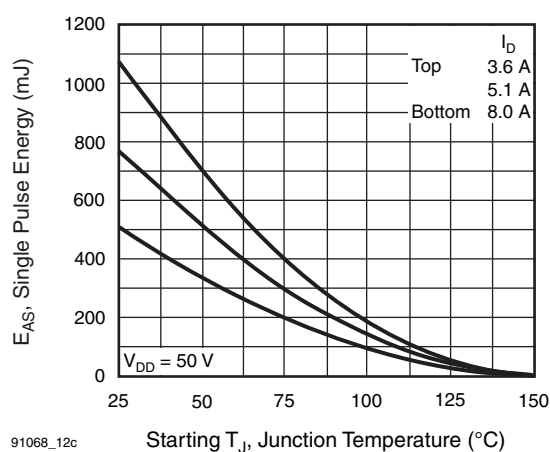


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

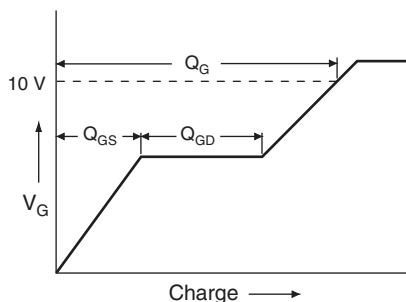


Fig. 13a - Basic Gate Charge Waveform

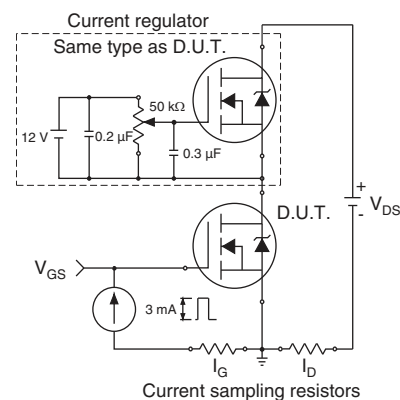
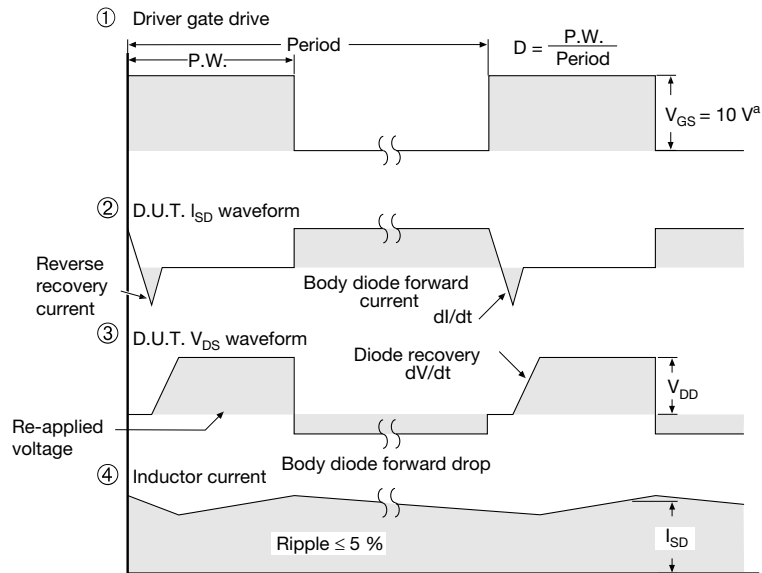
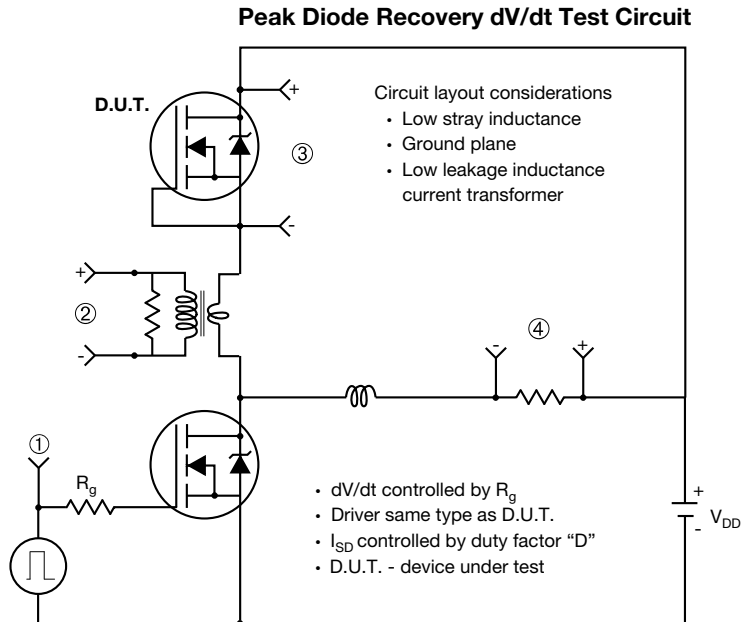


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel



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