DDC
ILC DATA DEVICE CORPORATION

BU-65170 and BU-61580

MIL-STD-1553A/B NOTICE 2 RT and BC/RT/MT, ADVANCED COMMUNICATION ENGINE (ACE)

PRELIMINARY

DESCRIPTION

DDC's BU-65170 RT and BU-61580 BC/RT/MT Advanced Communication Engine (ACE) family of terminals comprise complete integrated interfaces between a host processor and a MIL-STD-1553 bus. The ACE series of components provides RT-only and BC/RT/MT functions in the identical 1.9 square inch package footprint. The ACE components integrate dual transceiver, protocol, memory management and processor interface logic, and 4K words of internal buffered RAM in the choice of 70-pin DIP, flatpack, or J-lead packages. Transceiver options include +5(only), +5/-15, and +5/-12V.

To minimize board space and "glue" logic, the ACE terminals provide ultimate flexibility in interfacing to a host processor and internal/external RAM.

The ACE components provide complete multiprotocol support of MIL-STD-1553A/B/McAir and STANAG 3838. The advanced functional architecture of the ACE terminals provides software compatibility to DDC's previous AIM series hybrids. In addition, the ACE Terminals incorporate a multiplicity of architectural enhancements allowing flexible operation while offloading the host processor, ensuring data consistency, and supporting bulk data transfers.

The ACE hybrids may be operated at either 12 or 16MHz. Wire bond options allow for programmable RT address (hardwired is standard), interface to 17-bit RAM for parity generation/checking, and a direct interface to fiber optic (MIL-STD-1773) transceivers.

The ACE terminals operate over the full military temperature range of -55 to +125 °C. Available screened to MIL-STD-883B, the terminals are ideal for demanding military and industrial processor-to-1553 applications.

FEATURES

- ***Fully Integrated 1553A/B Notice 2, STANAG 3838 Interface Terminal***
- ***Small Ceramic Package***
- ***RT or BC/RT/MT In Same Footprint***
- ***Flexible Processor/Memory Interface: 16-Bit Buffered and Transparent, 8-Bit Buffered, Zero Wait State, and 16-Bit DMA; 4K Words Internal Ram***
- ***Advanced BC Features: Automatic Retries, Programmable Gap Times, Frame Auto-Repeat***
- ***Advanced RT Features: Programmable Illegalization and Busy; Choice of Single Message, Double Buffering, and Circular Buffering***
- ***Advanced Monitor Features: Choice of Word Monitor, Selective Message Monitor, or Simultaneous RT/Monitor Modes***

FIGURE1. BU-61580/65170 BLOCK DIAGRAM

TABLE 1. BU-61580 SERIES SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
Supply Voltage				
■ Logic +5V	-0.3		7.0	V
■ Transceiver +5V	-0.5		7.0	V
■ -15V	+0.3		-18.0	V
■ -12V	+0.3		-18.0	V
Logic				
■ Voltage Input Range	-0.3		V_{CC}+0.3	V
RECEIVER				
Differential Input Resistance				
■ (BU-65170/61580X1,BU-65170/61580X2) (Notes 1-6)	11			kohm
■ (BU-65170/61580X3,BU-65170/61580X6) (Notes 1-6)	1.5			kohm
Differential Input Capacitance				
■ (BU-65170/61580X1,BU-65170/61580X2) (Notes 1-6)			10	pf
■ (BU-65170/61580X3,BU-65170/61580X6) (Notes 1-6)			5	pf
Threshold Voltage, Transformer Coupled, Measured on Stub			0.860	V_{P-P}
Common Mode Voltage (Note 7)			10	V_{peak}
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Across 35 ohms, Measured on Bus	6		9	V_{P-P}
■ Transformer Coupled, Measured on Stub				
• BU-65170/61580X1	20	22	27	V_{P-P}
• BU-65170/61580X2	18	21	27	V_{P-P}
• BU-65170/61580X3,BU-65170/61580X6	18	21	27	V_{P-P}
Output Noise, Differential (Direct Coupled)			10	$mV_{P-P,diff}$
Output Offset Voltage, Direct Coupled Across 35 ohms	-90		90	mV
Rise/Fall Time	100	150	300	nsec
LOGIC				
V_{IH}	2.0			V
V_{IL}			0.8	V
I_{IH} (V_{CC}=5.5V, V_{IN}=5.0V)	-10		10	µA
I_{IH} (V_{CC}=5.5V, V_{IN}=2.4V)	-346		-42	µA
I_{IL} (V_{CC}=5.5V, V_{IN}=0V)	-397		-50	µA
V_{OH} (V_{CC}=4.5V, V_{IH}=2.4V, V_{IL}=0.7V, I_{OH}=max)	3.7			V
V_{OL} (V_{CC}=4.5V, V_{IH}=2.4V, V_{IL}=0.7V, I_{OL}=max)			0.4	V
I_{OL}				
■ DB0-DB15, A0-A15, $\overline{MEMOE}$/ADDR_LAT, $\overline{MEMWR}$/ZEROWAIT, $\overline{DTREQ}$/16/$\overline{8}$, $\overline{DTACK}$/POLARITY_SEL	-6.67			mA
■ $\overline{INCMD}$, $\overline{INT}$, $\overline{MEMENA\_OUT}$, $\overline{READYD}$, $\overline{IOEN}$	-3.3			mA
I_{OH}				
■ (DB0-DB15, A0-A15, $\overline{MEMOE}$/ADDR_LAT, $\overline{MEMWR}$/ZEROWAIT, $\overline{DTREQ}$/16/$\overline{8}$, $\overline{DTACK}$/POLARITY_SEL)			6.67	mA
■ $\overline{INCMD}$, $\overline{INT}$, $\overline{MEMENA\_OUT}$, $\overline{READYD}$, $\overline{IOEN}$			3.3	mA

TABLE 1. BU-61580 SERIES SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
■ +5V (Logic)	4.5		5.5	V
■ +5V (CH. A, CH. B)				
• (BU-65170/61580X1,BU-65170/61580X2)	4.5		5.5	V
• (BU-65170/61580X3,BU-65170/61580X6)	4.75		5.5	V
■ -15V (CH. A, CH. B)				
• (BU-65170/61580X1)	-15.75		-14.25	V
■ -12V (CH. A, CH. B)				
• (BU-65170/61580X2)	-12.6		-11.4	V
Current Drain (Total Hybrid)				
■ +5V (BU-65170/61580X1)			190	mA
■ +5V (BU-65170/61580X2)			190	mA
■ +5V (BU-65170/61580X3,BU-65170/61580X6)				
• Idle			200	mA
• 25% Duty Cycle			338	mA
• 50% Duty Cycle			575	mA
• 100% Duty Cycle			950	mA
■ +5v (BU-65170/61580X4,BU-65620X4)			100	mA
■ -15V (BU-65170/61580X1)				
• Idle			60	mA
• 25% Duty Cycle			108	mA
• 50% Duty Cycle			160	mA
• 100% Duty Cycle			255	mA
■ -12V (BU-65170/61580X2)				
• Idle			60	mA
• 25% Duty Cycle			120	mA
• 50% Duty Cycle			185	mA
• 100% Duty Cycle			305	mA
POWER DISSIPATION				
Total Hybrid				
■ (BU-65170/61580X1)				
• Idle			1.85	W
• 25% Duty Cycle			2.25	W
• 50% Duty Cycle			2.72	W
• 100% Duty Cycle			3.52	W
■ (BU-65170/61580X2)				
• Idle			1.67	W
• 25% Duty Cycle			2.10	W
• 50% Duty Cycle			2.59	W
• 100% Duty Cycle			3.46	W
■ (BU-65170/61580X3,BU-65170/61580X6)				
• Idle			1.00	W
• 25% Duty Cycle			1.65	W
• 50% Duty Cycle			2.30	W
• 100% Duty Cycle			3.60	W
■ (BU-65170/61580X4,BU-65620X4)			0.5	W
Hottest Die				
■ (BU-65170/61580X1)				
• Idle			0.68	W
• 25% Duty Cycle			1.06	W
• 50% Duty Cycle			1.45	W
• 100% Duty Cycle			2.23	W
■ (BU-65170/61580X2)				
• Idle			0.59	W
• 25% Duty Cycle			0.92	W
• 50% Duty Cycle			1.36	W
• 100% Duty Cycle			2.16	W

TABLE 1. BU-61580 SERIES SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
POWER DISSIPATION (continued)				
■ (BU-65170/61580X3,BU-65170/61580X6)				
• Idle			0.25	W
• 25% Duty Cycle			0.90	W
• 50% Duty Cycle			1.55	W
• 100% Duty Cycle			2.85	W
■ (BU-65170/61580X4,BU-65620X4)			0.5	W
CLOCK INPUT				
Frequency				
■ Nominal Value				
• (BU-65170/61580XX-XX0)		16.0		MHz
• (BU-65170/61580XX-XX1)		12.0		MHz
■ Long Term Tolerance				
• 1553A Mode			0.01	%
• 1553B Mode			0.1	%
■ Short Term Tolerance, 1 second				
• 1553A Mode			0.001	%
• 1553B Mode			0.01	%
■ Duty Cycle				%
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of First BC Message				µs
BC Intermessage Gap				µs
BC Response Timeout				µs
RT Response Time				µs
RT-to-RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status)				µs
Transmitter Watchdog Timeout				µs
THERMAL				
Thermal Resistance, Junction-to-Case, Hottest Die (θ_{JC})				
■ (BU-65170/61580X1,BU-65170/61580X2)		5.54		°C/W
■ (BU-65170/61580X3,BU-65170/61580X6)		6.8		°C/W
■ (BU-65170/61580X4,BU-65620X4)				°C/W
Thermal Resistance, Case-to-Ambient (θ_{CA})				
■ (BU-65170/61580X1,BU-65170/61580X2)				°C/W
■ (BU-65170/61580X3,BU-65170/61580X6)				°C/W
■ (BU-65170/61580X4,BU-65620X4)				°C/W
Operating Junction Temperature	-55		160	°C
Storage Temperature	-65		150	°C
Lead Temperature (soldering, 10 seconds)			+300	°C
PHYSICAL CHARACTERISTICS				
Size				
■ 70-pin DIP, FLATPACK, J-LEAD		1.9 X 1.0 X 0.215 (48.26X25.4X5.08)		in (mm)
Weight				
■ 70-pin DIP, FLATPACK, J-LEAD		1.0 (29)		oz (g)

NOTES: Notes 1 through 6 are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:
(1) Specifications include both transmitter and receiver (tied together internally).
(2) Measurement of impedance is directly between pins TX/RX A(B) and TX/RX A(B) of the BU-65170/61580XX hybrid.
(3) Assuming the connection of all power and ground inputs to the hybrid.
(4) The specifications are applicable for both unpowered and powered conditions.
(5) The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75kHz to 1MHz.
(6) Minimum resistance and maximum capacitance parameters are guaranteed,but not tested, over the operating range.
(7) Assumes a common mode voltage within the frequency range of dc to 2MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), referenced to hybrid ground. Transformer must be a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.

INTRODUCTION

DDC's ACE series of Integrated BC/RT/MT hybrids provide a complete, flexible interface between a microprocessor and a MIL-STD-1553A, B Notice 2, McAir, or STANAG 3838 bus, implementing Bus Controller, Remote Terminal (RT) and Monitor Terminal (MT) modes. Packaged in a single 1.9 square inch 70-pin DIP or surface mountable flatpack or J-lead package, the ACE series contains dual low-power transceivers and encoder/decoders, complete BC/RT/MT multi-protocol logic, memory management and interrupt logic, 4K X 16 of shared static RAM and a direct, buffered interface to a host processor bus.

The BU-65170/61580 contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. The BU-65170/61580 may be interfaced directly to both 16-bit and 8-bit microprocessors in a buffered shared RAM configuration. In addition, the ACE may connect to a 16-bit processor bus via a Direct Memory Access (DMA) interface. The BU-65170/61580 includes 4K words of buffered RAM. Alternatively, the ACE may be interfaced to as much as 64K words of external RAM in either the shared RAM or DMA configurations.

The ACE RT mode is multiprotocol, supporting MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838 (including EFAbus), and the McAir A3818, A5232, and A5690 protocols. The memory management scheme for RT mode provides an option for separation of broadcast data, in compliance with 1553B Notice 2. Both double buffer and circular buffer options are programmable by subaddress. These features serve to ensure data consistency and to off-load the host processor for bulk data transfer applications.

The ACE series implements three monitor modes: a word monitor, a selective message monitor, and a combined RT/selective monitor.

Other features include options for automatic retries and programmable intermessage gap for BC mode, an internal Time Tag Register, an Interrupt Status Register and internal command illegalization for RT mode.

TRANSCEIVERS

Low-power bipolar analog monolithic and thick-film hybrid technology makes implementation of the transceiver front end of the BU-65170/61580X1(X2) ACE hybrids possible. The transceiver requires +5 V and -15V (-12V) only (requiring no +15V/+12V) and includes voltage source transmitters. The voltage source transmitters provide superior line driving capability for long cables and heavy amounts of bus loading. In addition, the monolithic transceivers in the BU-65170/61580X1 provide a minimum stub voltage level of 20 volts peak-to-peak transformer coupled, making them suitable for MIL-STD-1760 applications.

Fully monolithic transceiver chips make the 5 volt dual transceiver front end of the BU-65170/61580X3 possible. Besides eliminating the need for an additional power supply, the use of a 5 volt (only) transceiver requires the use of step-up, rather than step-down, isolation transformers. This provides the advantage of a higher terminal input impedance than is possible for a 15 volt or 12 volt transmitter. As a result, there is greater margin for the input impedance test, mandated for 1553 validation testing. This allows for longer cable lengths between an LRU's system connector and the isolation transformers of an embedded 1553 terminal. The receiver sections of the BU-65170 and BU-61580 are fully compliant to MIL-STD-1553B in terms of overvoltage protection, threshold, common mode rejection, and bit error rate.

The receiver sections of the BU-65170/61580X1(X2,X3) are fully compliant with MIL-STD-1553B in terms of front end overvoltage protection, threshold, common mode rejection, and word error rate. In addition, the receiver filters have been designed for optimal operation with the J' chip's Manchester II decoders.

J' DIGITAL MONOLITHIC

The J' digital monolithic represents the cornerstone element of the ACE family of terminals. The development of the J' chip represented the fifth generation of 1553 protocol and interface design for DDC. Over the years, DDC's 1553 protocol and interface design has evolved from: (1) discrete component sets, consisting of multiple hybrids (with a large number of chips inside the hybrids) and programmable logic devices, to (2) multiple custom ASICs to perform the functions of encoder/decoder and RT protocol within a single hybrid, to (3) the BUS-61553 Advanced Integrated Mux Hybrid (AIM-HY) series, containing, in addition to a dual monolithic/thick-film transceiver and discrete RAM chips, a custom protocol chip and a separate custom memory management/processor interface chip; (4) the BUS-61559 Advanced Integrated Mux Hybrids with Enhanced RT Features (AIM-HY'er); the AIM-HY'er series includes memory management and processor interface functions beyond those of the AIM-HY series; (5) the full integration of the J' chip.

The J' chip consists of a dual encoder/decoder, complete protocol for Bus Controller (BC), 1553A/B/McAir Remote Terminal (RT), and Monitor (MT) modes; memory management and interrupt logic; a flexible, buffered interface to a host processor bus and optional external RAM; and 4K words of on-chip RAM. Reference the region within the dotted line of Figure 1. Besides realizing all the protocol, memory management, and interface functions of the earlier AIM-HY'er series, the J' chip includes a large number of enhancements to facilitate hardware and software design, and to further off-load the 1553 terminal's host processor.

DECODERS

The default mode of operation for the BU-65170 RT and BU-61580 BC/RT/MT requires a 16MHz clock input. If needed, a software programmable option allows the device to be operated from a 12MHz clock input. Most current 1553 decoders sample using a 10MHz or 12MHz clock. In the 16MHz mode (default following a hardware or software reset), the ACE decoders sample 1553 serial data using the 16MHz clock. In the 12MHz mode, the decoders sample using both clock edges; this provides a sampling rate of 24MHz. The faster sampling rate for the J-prime's Manchester II decoders provides superior performance in terms of bit error rate and zero-crossing distortion tolerance.

For interfacing to fiber optic transceivers for MIL-STD-1773 applications, the transceiverless BU-61581D4(F4) can be used. These versions provide a software programmable option for a direct interface to the single-ended outputs of a fiber optic receiver. No external logic is needed.

TIME TAGGING

The ACE includes an internal read/writable Time Tag Register.

This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. Also, the Time Tag Register may be clocked from an external oscillator. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register.

For each message processed, the value of the Time Tag register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both BC and RT modes.

Additional provided options will: clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command; enable an interrupt request and a bit setting in the Interrupt Status Register when the Time Tag Register rolls over from 0000 to FFFF. Assuming the Time Tag Register is not

loaded or reset, this will occur at approximately 4-second time intervals, for 64 µs/LSB resolution, down to 131 ms intervals, for 2 µs/LSB resolution.

Another programmable option for RT mode is the automatic clearing of the Service Request Status Word bit following the ACE's response to a Transmit Vector Word mode command.

INTERRUPTS

The ACE series components provide many programmable options for interrupt generation and handling. The interrupt output pin ($\overline{INT}$) has three software programmable modes of operation: the interrupt output may be a pulse, the level output may be cleared under software control, or the level output may be cleared by the interrupt acknowledge input. It should be noted that the interrupt acknowledge is not accessible on all versions of the ACE series components.

Individual interrupts are enabled by the Interrupt Mask Register. The host processor may easily determine the cause of the interrupt by using the Interrupt Status Register. The Interrupt Status Register provides the current state of the interrupt conditions. The Interrupt Status Register may be updated in two ways. In the standard interrupt handling mode, a particular bit in the Interrupt Status Register will be updated only if the condition exists and the corresponding bit in the Interrupt Mask Register is enabled. In the enhanced interrupt handling mode, a particular bit in the Interrupt Status Register will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit.

ADDRESSING INTERNAL REGISTERS, AND MEMORY MANAGEMENT

The software interface of the BU-65170/61580 to the host processor consists of 17 internal operational registers for normal operation, an additional 8 test registers, plus 64K X 16 of shared memory address space. The BU-65170/61580's 4K X 16 of internal RAM resides in this address space.

Definition of the address mapping and accessibility for the BU-65170/61580's 17 non-test registers, and the test registers, is as follows:

ADDRESS LINES						REGISTER DESCRIPTION/ACCESSIBILITY
HEX	A4	A3	A2	A1	A0	
00	0	0	0	0	0	Interrupt Mask Register (RD/WR)
01	0	0	0	0	1	Configuration Register # 1 (RD/WR)
02	0	0	0	1	0	Configuration Register # 2 (RD/WR)
03	0	0	0	1	1	Start/Reset Register (WR)
03	0	0	0	1	1	Command Stack Pointer Register (RD)
04	0	0	1	0	0	BC Control Word*/RT Subaddress Control Word Register (RD/WR)
05	0	0	1	0	1	Time Tag Register (RD/WR)
06	0	0	1	1	0	Interrupt Status Register (RD)
07	0	0	1	1	1	Configuration Register #3
08	0	1	0	0	0	Configuration Register #4
09	0	1	0	0	1	Configuration Register #5
0A	0	1	0	1	0	Data Stack Address Register (RD/WR)
0B	0	1	0	1	1	BC Frame Time Remaining Register (RD)*
0C	0	1	1	0	0	BC Time Remaining to Next Message Register (RD)*
0D	0	1	1	0	1	BC Frame Time*/RT Last Command/MT Trigger Word* Register (RD/WR)
0E	0	1	1	1	0	RT Status Word Register (RD)
0F	0	1	1	1	1	RT BIT Word Register (RD)
10	1	0	0	0	0	Test Mode Register 0
11	1	0	0	0	1	Test Mode Register 1
17	1	0	1	1	1	Test Mode Register 7
18	1	1	0	0	0	reserved
1F	1	1	1	1	1	reserved

NOTE: * BU-61580 Only

Interrupt Mask Register: used to enable and disable interrupt requests for various conditions. Configuration Registers #1 and #2: used to select the BU-61580's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and control of the Time Tag operation.

Stack Pointer Register: allows the host CPU to determine the pointer location for the current or most recent message when the BU-61580 is in BC or RT modes.

Start/Reset Register: used for "command" type functions, such as software reset, BC/MT Start, Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Start/Reset Register includes provisions for stopping the BC in its AUTO-REPEAT mode, either at the end of the current message or at the end of the current BC frame.

Subaddress Control Word Register: allows the host processor access to the current or most recent Subaddress Control Word; the read/write accessibility of this register can be used as an aid for testing the BU-61580.

16-bit Time Tag Register: maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The TAG_CLK input signal also may cause an external oscillator to clock the Time Tag Register. Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes causes a write of the current value of the Time Tag Register to the stack area of RAM.

The Interrupt Status Register mirrors the Interrupt Mask Register and contains a Master Interrupt bit. It allows the host processor to determine the cause of an interrupt request by means of a single READ operation.

Configuration Registers #3, #4, and #5: used to enable many of the BU-61580's advanced features. These include all the enhanced mode features; that is, all the functionality beyond that of the previous generation product, the BUS-61559 Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er). For all three modes, use of the Enhanced Mode enables the various read-only bits in Configuration Register #1.

For BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional STOP-ON-ERROR and STOP-ON-STATUS SET functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message.

For RT mode, the enhanced mode features include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the "RTFAIL" output signal to the "RTFLAG" input signal, the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word.

For MT mode, use of the enhanced mode enables use of the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

Data Stack Address Register: used to point to the current address location in shared RAM used for storing message words (second Command Words, Data Words, RT Status Words) in the Selective Word Monitor mode.

The Frame Time Remaining Register provides a read only indication of the time remaining in the current BC frame. The resolution of this register is 100 µs/LSB.

The Message Time Remaining Register provides a read only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 µs/LSB.

Different modes of operation use the register at register address 0D differently: In BC mode, it programs the BC frame time, for use in the FRAME AUTO-REPEAT mode. The resolution of this register is 100 µs/LSB, with a range of 6.55 seconds; in RT mode, this register stores the current (or most previous) 1553 Command Word processed by the ACE RT; in the Monitor mode, this register specifies a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

The Status Word Register and BIT Word Register provide read-only indications of the BU-65170/61580's RT Status and BIT Words.

The ACE also includes a set of test registers. These registers may be used to facilitate production or maintenance testing of the BU-61580 and systems incorporating the BU-61580.

BIT	DESCRIPTION
15 MSB	RESERVED
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT CMD STK ROLLOVER
11	MT CMD STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	RT MODE/MT PATTERN TRIG
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	STATUS SET
0 LSB	END OF MESSAGE

NOTE: The host processor can read or write to bits 15 through 8.

FIGURE 2. INTERRUPT MASK REGISTER (READ/WRITE)

BIT	DESCRIPTION
15 MSB	RT/$\overline{BC}$-MT
14	
13	
12	
11	MT/$\overline{BC}$-RT
10	
9	
8	
7	CURRENT AREA B/$\overline{A}$
6	
5	
4	
3	
2	
1	
0 LSB	

NOTE: See Table 2

FIGURE 3. CONFIGURATION REGISTER #1 (READ/WRITE)

TABLE 2.

BIT	BC FUNCTION (bits 11-0 Enhanced Mode only)	RT W/O ALTERNATE STATUS	RT WITH ALTERNATE STATUS (Enhanced Mode Only)	MONITOR FUNCTION (Enhanced Mode Only)
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	DYNAMIC BUS CONTROL ACCEPTANCE	S10	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	BUSY	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	SERVICE REQUEST	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	SUBSYSTEM FLAG	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	RTFLAG (enhanced mode only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTER-MESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	NOT USED	NOT USED	S02	NOT USED
2	BC ENABLED (Read Only)	NOT USED	S01	MONITOR ENABLED (Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0	BC MESSAGE IN PROGRESS (Read only)	RT MESSAGE IN PROGRESS (Enhanced Mode only) (Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

BIT	DESCRIPTION
15 MSB	ENHANCED INTERRUPTS
14	RAM PARITY ENABLED
13	BUSY LOOKUP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDR DISBL
9	TIME TAG RESOLUTION 2 (TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0 LSB	SEPARATE BROADCAST DATA

FIGURE 4. CONFIGURATION REGISTER #2 (READ/WRITE)

BIT	DESCRIPTION
15 MSB	COMMAND STACK POINTER 15
14	
13	
12	
11	
10	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0 LSB	COMMAND STACK POINTER 0

FIGURE6. BC/RT COMMAND STACK POINTER REGISTER (READ)

BIT	DESCRIPTION
15 MSB	RESERVED
14	
13	
12	
11	BC/MT STOP-ON-MESSAGE
10	
9	
8	
7	
6	
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0 LSB	RESET

FIGURE 5. START/RESET REGISTER (WRITE)

BIT	DESCRIPTION
15 MSB	RESERVED
14	M.E. MASK
13	SUBSYS BUSY BIT MASK
12	SUBSYS FLAG BIT MASK
11	TERMINAL FLAG BIT MASK
10	RESERVED BITS MASK
9	RETRY ENABLED
8	BUS CHANNEL A/$\overline{B}$
7	OFF LINE SELF TEST
6	MASK BROADCAST BIT
5	EOM INTERRUPT ENABLE
4	1553A/B SELECT
3	MODE CODE FORMAT
2	BROADCAST FORMAT
1	RT-RT FORMAT
0 LSB	

FIGURE 7. BC CONTROL WORD REGISTER (READ/WRITE)

BIT	DESCRIPTION
15 MSB	RX DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MM2
11	TX: MM1
10	TX: MM0
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MM2
6	RX: MM1
5	RX: MM0
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MM2
1	BCST: MM1
0 LSB	BCST: MM0

FIGURE 8. SUBADDRESS CONTROL WORD REGISTER (READ/WRITE)

BIT	DESCRIPTION
15 MSB	TIME TAG 15
•	•
•	•
•	•
0 LSB	TIME TAG 0

FIGURE 9. TIME TAG REGISTER (READ/WRITE)

BIT	DESCRIPTION
15 MSB	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	RT MODE/MT PATTERN TRIGGER
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	STATUS SET
0 LSB	END OF MESSAGE

FIGURE 10. INTERRUPT STATUS REGISTER (READ/WRITE)

BIT	DESCRIPTION
15 MSB	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/$\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER DISABLE
2	RTFAIL-FLAG WRAP ENABLE
1	1553A MODE CODES ENA
0 LSB	ENHANCED MODE CODE HANDLING

FIGURE 11. CONFIGURATION REGISTER #3 (READ/WRITE)

BIT	DESCRIPTION
15 MSB	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENA/$\overline{XOR}$
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/$\overline{SAME}$ BUS
7	2ND RETRY ALT/$\overline{SAME}$ BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDR WITH CONFIG #5
2	TEST MODE 2
1	TEST MODE 1
0 LSB	TEST MODE 0

FIGURE 12. CONFIGURATION REGISTER #4 (READ/WRITE)

BIT	DESCRIPTION
15 MSB	12MHZ CLOCK SELECT
14	SINGLE ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDR LATCH/$\overline{TRANSPARENT}$
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0 LSB	RT ADDRESS PARITY

FIGURE 13. CONFIGURATION REGISTER #5 (READ/WRITE)

BIT	DESCRIPTION
15 MSB	MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0 LSB	MONITOR DATA STACK ADDRESS 0

FIGURE14. MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE)

BIT	DESCRIPTION
15 MSB	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0 LSB	BC FRAME TIME REMAINING 0

Note: resolution = 100 µs per LSB

FIGURE 15. BC FRAME TIME REMAINING REGISTER (READ/WRITE)

BIT	DESCRIPTION
15 MSB	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0 LSB	BC MESSAGE TIME REMAINING

Note: resolution = 100 µs per LSB

FIGURE 16. BC MESSAGE TIME REMAINING REGISTER (READ)

BIT	DESCRIPTION
15 MSB	BIT 15
•	•
•	•
•	•
0 LSB	BIT 0

FIGURE 17. BC FRAME TIME/RT LAST COMMAND/MT TRIGGER REGISTER (READ/WRITE)

BIT	DESCRIPTION
15 MSB	RT ADDRESS 4
14	RT ADDRESS 3
13	RT ADDRESS 2
12	RT ADDRESS 1
11	RT ADDRESS 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST CMD RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0 LSB	TERMINAL FLAG

FIGURE 18. RT STATUS WORD REGISTER (READ)

BIT	DESCRIPTION
15 MSB	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL B/$\overline{A}$
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0 LSB	COMMAND WORD CONTENTS ERROR

FIGURE 19. RT BIT WORD REGISTER (READ)

BIT	DESCRIPTION
15 MSB	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0 LSB	INVALID WORD

FIGURE 20. BC MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15 MSB	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-RT FORMAT ERROR
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0 LSB	COMMAND WORD CONTENTS ERROR

FIGURE 21. RT MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15 MSB	GAP TIME
14	WORD FLAG
13	THIS RT
12	BROADCAST
11	ERROR
10	COMMAND/$\overline{DATA}$
9	CHANNEL B/$\overline{A}$
8	CONTIGUOUS DATA/$\overline{GAP}$
7	MODE CODE
6	
5	
4	
3	
2	
1	
0 LSB	

FIGURE 22. WORD MONITOR IDENTIFICATION WORD

BIT	DESCRIPTION
15 MSB	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0 LSB	COMMAND WORD CONTENTS ERROR

FIGURE 23. MESSAGE MONITOR MODE BLOCK STATUS WORD

BUS CONTROLLER (BC) ARCHITECTURE

The BC protocol of the BU-61580 implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of bits in the BC Control Word and the T/$\overline{R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The BU-61580's BC response timeout value is programmable from among 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

The BU-61580 may be programmed to process BC frames of up to 512 messages with no processor intervention. It is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input. The internal BC frame time is programmable up to 6.55 seconds in increments of 100 µs. In addition to BC frame time, intermessage gap time, defined as the start of the current message to the start of the subsequent message, is programmable on an individual message basis. Intermessage gap is programmable up to 65.5 ms, in increments of 1 µs. Figure 24 illustrates BC intermessage gap and frame timing.

BC MEMORY ORGANIZATION

Table 3 illustrates a typical memory map for BC mode. It is important to note that the only fixed locations for the BU-61580 in the Standard BC mode are for the two Stack Pointers (address locations 0100 (hex) and 0104) and for the two Message Count locations (0101 and 0105). Enabling the Frame Auto-Repeat mode will reserve four more memory locations for use in the Enhanced BC mode; these locations are for the two Initial Stack Pointers (address locations 102 (hex) and 106) and for the Initial Message Count locations (103 and 107). The user is free to locate the Stack and BC Message Blocks anywhere else within the 64K (4K internal) shared RAM address space.

For simplicity of illustration, assume the allocation of the maximum length of a BC message for each message block in the typical BC memory map of Table 3. The maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words). Note, however, that this example assumes the disabling of the 256-word boundaries.

TABLE 3. TYPICAL BC MEMORY ORGANIZATION
(shown for 4K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101	Message Count A (fixed location)
0102	Initial Stack Pointer A (see note) (Auto-Frame Repeat Mode)
0103	Initial Message Count A (see note) (Auto-Frame Repeat Mode)
0104	Stack Pointer B
0105	Message Count B
0106	Initial Stack Pointer B (see note) (Auto-Frame Repeat Mode)
0107	Initial Message Count B (see note) (Auto-Frame Repeat Mode)
0108-012D	Message Block 0
012E-0153	Message Block 1
0154-0179	Message Block 2
•	•
•	•
•	•
0140-017F	Message Block 0
0180-01BF	Message Block 1
01C0-01FF	Message Block 2
•	•
•	•
•	•
0ED6-0EFB	Message Block 93
0EFC-0EFF	Not Used
0F00-0FFF	Stack B

* Note: Used only in the Enhanced BC mode with Frame Auto-Repeat enabled.

BC INTERRUPTS

BC interrupts may be enabled by the Interrupt Mask Register for Stack Rollover, Retry, End-of-Message (global), End-of-Message (in conjunction with the BC Control Word for individual messages), response timeout, message error, end of BC frame, and Status Set conditions. The definition of "Status Set" is programmable on an individual message basis by means of the BC Control Word. This allows for masking ("care/don't care") for the individual RT Status Word bits.

AUTOMATIC RETRIES

The BU-61580 BC implements automatic message retries. When enabled, retries will occur, either one or two times, following response timeout or format error conditions. As additional options, retries may be enabled when setting the Message Error Status Word bit from a 1553A RT or following a "Status Set" condition. Again, for a failed message, either one or two message retries will occur: the bus channel (same or alternate) is independently programmable for the first and second retry attempts. Retries may be enabled or disabled on an individual message basis.

FIGURE 24. BC INTERMESSAGE GAP AND FRAME TIMING

BC MEMORY MANAGEMENT

Figure 25 illustrates the BU-61580's memory management scheme. One of the BC memory management features is the global double buffering mechanism. This provides for dual sets of the various BC mode data structures: Stack Pointer and Message Counter locations, Descriptor Stack areas, and BC message blocks. Bit 13 of Configuration Register #1 selects the current active area. At any point in time, the BU-61580's internal 1553 memory management logic may access only the various data structures within the "active" area. Figure 25 delineates the "active" and "inactive" areas by the non-shaded and shaded areas, respectively; however, at any point in time, **both the "active" and "non-active" areas are accessible by the host processor.** In most applications, the host processor will access the "non-active" area, while the 1553 bus processes the "active" area messages.

The BC may be programmed to transmit multi-message frames of up to 512 messages. The number of messages to be processed is programma ble by the Active Area Message Count location in the shared RAM, initialized by the host processor. In addition, the host processor must initialize another location, the Active Area Stack Pointer. The Stack Pointer references the four-word message block descriptor in the Stack area of shared RAM for each message to be processed.

In the BC Frame Auto-Repeat mode, the Initial Stack Pointer and Initial Message Counter locations must be loaded by the host prior to the processing of the first frame. The single frame mode does not use these two locations.

The third and fourth words of the BC block descriptor are the Intermessage Gap Time and the Message Block Address for the respective message. These two memory locations must be written by the host processor prior to the start of message processing. Use of the Intermessage Gap Time is optional. The Block Address pointer specifies the starting location for each message block. The first word of each BC message block is the BC Control Word.

At the start and end of each message, the Block Status and Time Tag Words write to the message block descriptor in the stack. The Block Status Word includes indications of message in process or message completion, bus channel, Status Set, response timeout, retry count, Status address mismatch, loop test (on-line self-test) failure, and other error conditions. Figure 20 illustrated the bit mapping of the BC Block Status word. The 16-bit Time Tag Word will reflect the current contents of the internal Time Tag Register. This read/writable register, which operates for all three modes, has programmable resolution of from 2 to 64 µs/LSB. In addition, the Time Tag register may be clocked from an external source.

FIGURE 25. BC MODE MEMORY MANAGEMENT

REMOTE TERMINAL (RT) ARCHITECTURE

The RT protocol design of the BU-65170/61580 represents DDC's fifth generation implementation of a 1553 RT. One of the salient features of the BU-65170/61580's RT architecture is its true multiprotocol functionality. This includes programmable options for support of MIL-STD-1553A, the various McAir protocols, and MIL-STD-1553B Notice 2. The BU-65170/61580 RT response time is 2 to 5 µs dead time (4 to 7 µs per 1553B), providing compliance to all the 1553 protocols. Additional multiprotocol features of the BU-65170/61580 include options for full software control of RT Status and Built-in-Test (BIT) words. Alternatively, for 1553B applications, these words may be formulated in real time by the BU-65170/61580 protocol logic.

The BU-65170/61580 RT protocol design implements all the MIL-STD-1553B message formats and dual redundant mode codes. This design basis itself largely on previous generation designs that have passed SEAFAC testing for MIL-STD-1553B compliance. The BU-65170/61580 RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. Other key features of the BU-65170/61580 RT include a set of interrupt conditions, internal command illegalization, and programmable BUSY by subaddress.

RT MEMORY ORGANIZATION

Table 4 illustrates a typical memory map for the BUS-61580 in RT mode. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. Besides the Stack Pointer, for RT mode there are several other areas of the ACE address space designated as fixed locations. All RT modes of operation require the Area A and Area B Lookup Tables. Also allocated, are several fixed locations for optional features: Command Illegalization Lookup Table, Mode Code Selective interrupt Table, Mode Code Data Table, Busy Bit Lookup Table, and Selective Message Monitor Command Stack Pointers, Data Stack Pointers, and Lookup Table. It should be noted that any unenabled optional fixed locations may be used for general purpose storage (data blocks).

The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, address range locations are 0140 to 01BF for Area A and 01C0 to 023F for Area B. The RT lookup tables include Subaddress Control Words and the individual Data Block Pointers. If used, address range 0300-03FF will be dedicated as the illegalizing section of RAM. The actual Stack RAM area and the individual data blocks may be located in any of the non-fixed areas in the shared RAM address space.

TABLE 4. TYPICAL RT MEMORY MAP (shown for 4K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	RT Command Stack Pointer A (fixed location)
0101	RESERVED
0102	Monitor Command Stack A (fixed location)
0103	Monitor Data Stack A (fixed location)
0104	Stack Pointer B (fixed location)
0105	RESERVED
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Command Illegalizing Table (fixed area)
0400-05FF	Monitor Data Stack
0600-061F	Data Block 1
0620-063F	Data Block 2
•	•
•	•
•	•
0EE0-0EFF	Data Block 72
0F00-0FFF	Monitor Command Stack A

RT MEMORY MANAGEMENT

One of the salient features of the BU-65170/61580 series products is the flexibility of its RT memory management architecture. The RT architecture allows the memory management scheme for each transmit, receive, or broadcast subaddress to be programmable on a subaddress basis. Also, in compliance with MIL-STD-1553B Notice 2, the BU-65170/61580 provides an option to separate data received from broadcast messages from non-broadcast received data.

Besides supporting a global double buffering scheme (as in BC mode), the BU-65170/61580 RT provides a pair of 128-word Lookup Tables for memory management control, programmable on a subaddress basis (refer to Table 5). The 128-word tables include 32-word tables for transmit message pointers and receive message pointers. There is also a third, optional Lookup Table for broadcast message pointers, providing Notice 2 compliance, if necessary.

The fourth section of each of the RT Lookup Tables stores the 32 Subaddress Control Words (refer to Figure 8 and Table 6). The individual Subaddress Control Words may be used to select the RT memory management option and interrupt scheme for each transmit, receive, and (optionally) broadcast subaddress.

For each transmit subaddress, there are two possible memory management schemes: (1) single message; and (2) circular buffer. For each receive (and optionally broadcast) subaddress, there

are three possible memory management schemes: (1) single message; (2) double buffered; and (3) circular buffer. For each transmit, receive and broadcast subaddress, there are two interrupt conditions programmable by the respective Subaddress Control Word: (1) after every message to the subaddress; (2) after a circular buffer rollover. An additional table in RAM may be used to enable interrupts following selected mode code messages.

When using circular buffer scheme for a given subaddress, the size of the circular buffer is programmable by three bits of the Subaddress Control Word. The options for circular buffer size are 128, 256, 512, 1024, 2048, 4096, and 8192 Data Words.

TABLE 5. RT LOOK-UP TABLES

AREA A	AREA B	DESCRIPTION	COMMENT
0140	01C0	Rx(/Bcst)_SA0	Receive (/Broadcast) Lookup Table
.	.	.	
.	.	.	
.	.	.	
015F	01DF	Rx(/Bcst)_SA31	
0160	01E0	Tx_SA0	Transmit Lookup Table
.	.	.	
.	.	.	
.	.	.	
017F	01FF	Tx_SA31	
0180	0200	Bcst_SA0	Broadcast Lookup Table (Optional)
.	.	.	
.	.	.	
.	.	.	
019F	021F	Bcst_SA31	
01A0	0220	SACW_SA0	Subaddress Control Word Lookup Table (Optional)
.	.	.	
.	.	.	
.	.	.	
01BF	023F	SACW_SA31	

TABLE 6. SUBADDRESS CONTROL WORD
Memory Management Subaddress Buffer Scheme

MM2	MM1	MM0	DESCRIPTION	COMMENT
0	0	0	Single Buffer	Circular Buffer of Specified Size
0	0	1	128-Word	
0	1	0	256-Word	
0	1	1	512-Word	
1	0	0	1024-Word	
1	0	1	2048-Word	
1	1	0	4096-Word	
1	1	1	8192-Word	

SINGLE MESSAGE MODE

Figure 26 illustrates the RT Single Message memory management scheme. When operating the BU-65170/61580 in its "AIM-HY" (default) mode, the Single Message scheme implements for **all** transmit, receive, and broadcast subaddresses. In the Single Message mode (also in the Double Buffer and Circular Buffer modes), there is a global double buffering scheme, controlled by bit 13 of Configuration Register #1. This selects from between the two sets of the various data structures shown in the figure: the Stack Pointers (fixed addresses), Descriptor Stacks (user defined addresses), RT Lookup Tables (fixed addresses), and RT Data Word blocks (user defined addresses). Figures 26, 27, and 28 delineate the "active" and "non-active" areas by non-shaded and shaded areas, respectively.

As shown, the Command Word from each message received stores in the fourth location within the message descriptor (in the stack) for the respective message. Using the T/$\overline{R}$ bit, subaddress field, and (optionally) broadcast/own address, to index into the active area Lookup Table, locates the data block pointer for the current message. The BU-65170/61580 RT memory management logic then accesses the data block pointer to locate the starting address for the Data Word block for the current message. The maximum size for an RT Data Word block is 32 words.

For a particular subaddress in the Single Message mode there is overwriting of the contents of the data blocks for receive/broadcast subaddresses — or overreading, for transmit subaddresses. In the single message mode, it is possible to access multiple data blocks for the same subaddress. This, however, requires the intervention of the host processor to update the respective Lookup Table pointer.

To implement a data wrap-around subaddress, as required by Notice 2 of MIL-STD-1553B, the Single Message scheme should be used for the wrap-around subaddress. Notice 2 recommends subaddress 30 as the wrap-around subaddress.

CIRCULAR BUFFER MODE

Figure 27 illustrates the RT circular buffer memory management scheme. The circular buffer mode facilitates bulk data transfers. The size of the RT circular buffer, shown on the right side of the figure, is programmable from 128 to 8192 words (in even powers of 2) by the respective Subaddress Control Word. As in the single message mode, the host processor initially loads the individual Lookup Table entries. At the start of each message, the Lookup Table entry stores in the third position of the respective message block descriptor in the stack area of RAM, as in the Single Message mode. Receive or Transmit Data Words then transfer to (from) the circular buffer, starting at the location referenced by the Lookup Table pointer.

At the end of a valid (or, optionally, invalid) message, the value of the Lookup Table entry updates to the next location after the last address accessed for the current message. As a result, Data Words for the next message directed to the same Tx/RX(/Bcst) subaddress will be accessed from the next contiguous block of address locations within the circular buffer. As a recommended option, the Lookup Table pointers may be programmed to **not** update following an invalid receive (or broadcast) message. This allows the 1553 bus controller to retry the failed message, resulting in the valid (retried) data overwriting the invalid data. This eliminates overhead for the RT's host processor. When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192-word boundaries in the BU-65170/61580 address space), the pointer moves to the top boundary of the circular buffer, as Figure 27 shows.

FIGURE 26. RT MEMORY MANAGEMENT: SINGLE MESSAGE MODE

FIGURE 27. RT MEMORY MANAGEMENT: CIRCULAR BUFFER MODE

Implementing Bulk Data Transfers

The use of the Circular Buffer scheme is ideal for bulk data transfers; that is, multiple messages to/from the same subaddress. The recommendation for such applications is to enable the circular buffer interrupt request. By so doing, the routine transfer of multiple messages to the selected subaddress, including errors and retries, is transparent to the RT's host processor. By strategically initializing the subaddresses's Lookup Table pointer prior to the start of the bulk transfer, the BU-65170/61580 may be configured to issue an interrupt request only after it has received the anticipated number of valid Data Words to the designated subaddress.

SUBADDRESS DOUBLE BUFFERING MODE

For receive (and broadcast) subaddresses, the BU-65170/61580 RT offers a third memory management option, Subaddress Double Buffering. Subaddress double buffering provides a means of ensuring data consistency. Figure 28 illustrates the RT Subaddress Double Buffering scheme. Like the Single Message and Circular Buffer modes, the Double Buffering mode may be selected on a subaddress basis by the Subaddress Control Word. The purpose of the Double Buffering mode is to provide the host processor a convenient means of accessing the most recent, valid data received to a given subaddress. This serves to ensure the highest possible degree of data consistency by allocating two 32-bit Data Word blocks for each individual receive (and/or broadcast) subaddress.

At a given point in time, one of the two blocks will be designated as the "active" 1553 data block while the other will be designated as the "inactive" block. The Data Words from the next receive message to that subaddress will be stored in the "active" block. Upon completion of the message, provided that the message was valid and an enabled Subaddress Double Buffering, the BU-65170/61580 will automatically switch the "active" and "inactive" blocks for the respective subaddress. The ACE accomplishes this by toggling bit 5 of the subaddress's Lookup Table Pointer and re-writing the pointer. As a result, the most recent valid block of received Data Words will always be readily accessible to the host processor.

As a means of ensuring data consistency, the host processor is able to reliably access the most recent valid, received Data

FIGURE 28. RT MEMORY MANAGEMENT: SUBADDRESS DOUBLE BUFFERING MODE

Word block by performing the following sequence:

(1) Disable the double buffering for the respective subaddress by the Subaddress Control Word. That is, temporarily switch the subaddress's memory management scheme to the Single Message mode.

(2) Read the current value of the receive (or broadcast) subaddress's Lookup Table pointer. This points to the current "active" Data Word block. By inverting bit 5 of this pointer value, it is possible to locate the start of the "inactive" Data Word block. This block will contain the Data Words received during the most recent valid message to the subaddress.

(3) Read out the words from the "inactive" (most recent) Data Word Block.

(4) Re-enable the Double Buffering mode for the respective subaddress by the Subaddress Control Word.

RT INTERRUPTS

As in BC mode, the BU-65170/61580 RT provides many maskable interrupts. RT interrupt conditions include End of (every) Message, Message Error, Selected Command word (Subaddress Control Word) Interrupt, Circular Buffer Rollover, Selected Mode Code Interrupt, and Stack Rollover.

DESCRIPTOR STACK

At the beginning and end of each message, the BU-65170/61580 RT stores a 4-word message descriptor in the active area stack. Figures 26, 27, and 28 show the four words: Block Status Word, Time Tag Word, Data Block Pointer, and the 1553 received Command Word. The RT Block Status Word includes indications of message in-progress or message complete, bus channel, RT-to-RT transfer and RT-to-RT transfer errors, message format error, loop test (self-test) failure, circular buffer rollover, illegal command, and other error conditions. Figure 21 shows the bit mapping of the RT Block Status Word.

As in BC mode, the Time Tag Word stores the current contents of the BU-65170/61580's read/writable Time Tag Register. The resolution of the Time Tag Register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. Also, incrementing of the Time Tag counter may be from an external clock source or via software command.

The contents of the accessed Lookup Table location for the current message, indicating the starting location of the Data Word block, stores as the Data Block Pointer. This serves as a convenience in locating stored message data blocks. The full 16-bit 1553 Command Word stores in the fourth location of the RT message descriptor.

RT COMMAND ILLEGALIZATION

The BU-65170/61580 provides an internal mechanism for RT command illegalization. In addition, there is a means for allowing the setting of the Busy Status Word bit to be only for a programmed subset of the transmit/receive/broadcast subaddresses.

The illegalization scheme uses a 256-word area in the BU-65170/61580's address space. A benefit of this feature is the reduction of printed circuit board requirements, by eliminating the need for an external PROM, PLD, or RAM device that does the illegalizing function. The BU-65170/61580's illegalization scheme provides the maximum flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. Another advantage of the RAM-based illegalization technique is that it provides for a high degree of self-testability.

Addressing the Illegalization Table.

Figure 29 illustrateS the addressing scheme of the illegalization RAM . As shown, the base address of the illegalizing RAM is 0300 (hex). Formulation of the index into the illegalizing RAM is by BROADCAST/OWN ADDRESS, T/$\overline{R}$ bit, Subaddress, and the MSB of the Word Count/Mode Code field (WC/MC4).

BIT	DESCRIPTION
15 MSB	0
14	0
13	0
12	0
11	0
10	0
9	1
8	1
7	BRDCST/OWN ADDR
6	T/$\overline{R}$
5	SA4
4	SA3
3	SA2
2	SA1
1	SA0
0 LSB	WC4/MC4

FIGURE 29. ILLEGALIZING RAM ADDRESS DEFINITION

The internal RAM has 256 words reserved for command illegalization. Broadcast commands may be illegalized separately from non-broadcast receive commands and mode commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to subaddress 1 may be legal, while a 2-word receive command to subaddress 1 may be illegalized.

The first 64 words of the Illegalization Table refer to broadcast receive commands (two words per subaddress). The next 64 words refer to broadcast transmit commands. Since non-mode code broadcast transmit commands are by definition invalid, this

section of the table (corresponding to addresses 30 and 31) does not need to be initialized by the user. The next 64 words correspond to non-broadcast receive commands. The final 64 words refer to non-broadcast transmit commands. Messages with Word Count/Mode Code (WC/MC) fields between 0 and 15 may be illegalized by setting the corresponding data bits for the respective even-numbered address locations in the illegalization table. Likewise, messages with WC/MC fields between 16 and 31 may be illegalized by setting the corresponding data bits for the respective odd-numbered address locations in the illegalization table.

The following should be noted with regards to command illegalization:

(1) To illegalize a particular word count for a given broadcast/own address-T/$\overline{R}$ subaddress, the appropriate bit position in the respective illegalization word should be set to logic 1. A bit value of logic 0 designates the respective Command Word as a legal command. The BUS-61559 will respond to an illegalized non-broadcast command with the Message Error bit set in its RT Status Word.

(2) For subaddresses 00001 through 11110, the "WC/MC" field specifies the Word Count field of the respective Command Word. For subaddresses 00000 and 11111, the "WC/MC" field specifies the Mode Code field of the respective Command Word.

(3) Since non-mode code broadcast transmit messages are not defined by MIL-STD-1553B, the sixty (60) words in the illegalization RAM, addresses 0342 through 037D, corresponding to these commands do not need to be initialized. The BUS-61559 will not respond to a non-mode code broadcast transmit command, but will automatically set the Message Error bit in its internal Status Register, regardless of whether or not corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the BUS-61559 will respond with its Message Error bit set.

PROGRAMMABLE BUSY

As a means of providing compliance with Notice 2 of MIL-STD-1553B, the BU-65170/61580 RT provides a software controllable means for setting the Busy Status Word bit as a function of subaddress. By a Busy Lookup Table in the BU-65170/61580 address space, it is possible to set the Busy bit based on command broadcast/own address, T/$\overline{R}$ bit, and subaddress. Another programmable option, involving a set Busy bit, allows received Data Words to be either stored or not stored for messages.

OTHER RT FUNCTIONS

The BU-65170/61580 allows the hardwired RT Address to be read by the host processor. Also, there are options for the RT FLAG Status Word bit to be set under software control and/or automatically following a failure of the loopback self-test. Other software controllable RT options include software programmable RT Status and RT BIT words, automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands, options regarding Data Word transfers for set Busy and/or Message Error (Illegal) Status Word bits, and for handling of 1553A and reserved mode codes.

MONITOR (MT) ARCHITECTURE

The BU-61580 provides three bus monitor (MT) modes:

(1) The "AIM-HY" (default) or "AIM-HY'er" Word Monitor mode.
(2) A Selective Message Monitor mode.
(3) A Simultaneous Remote Terminal/Selective Message Monitor mode.

The strong recommendation for new applications is the use of the Selective Message Monitor, rather than the Word Monitor. Besides providing monitor filtering based on RT Address, T/$\overline{R}$ bit, and Subaddress, the Message Monitor eliminates the need to determine the start and end of messages by software. The development of such software tends to be a tedious task. Moreover, at run time, it tends to entail a high degree of CPU overhead.

WORD MONITOR

In the Word Monitor mode, the BU-61580 monitors both 1553 buses. After initializing the Word Monitor and putting it on-line has, the BU-61580 stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words stores in the BU-61580's RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or "Tag" word. The ID Word contains information relating to bus channel, sync type, word validity, and inter-word time gaps. The data and ID words store in a circular buffer in the shared RAM address space. Figure 22 shows the bit mapping for the Monitor ID word.

SELECTIVE MESSAGE MONITOR MODE

The BU-61580 Selective Message Monitor provides features to greatly reduce the software and processing burden of the host CPU. The Selective Message Monitor implements selective monitoring of messages from a dual 1553 bus, with the monitor filtering based on the RT Address, T/$\overline{R}$ bit, and Subaddress fields of received 1553 Command Words. The Selective Message Monitor mode greatly simplifies the host processor software by distinguishing between Command and Status Words. The Selective Message Monitor maintains two stacks in the BU-61580 RAM: a Command Stack and a Data Stack.

The Selective Message Monitor may function as a purely passive monitor or may be programmed to function as a simul-

taneous RT/Monitor. The RT/Monitor mode provides complete Remote Terminal (RT) operation for the BU-61580's strapped RT address and bus monitor capability for the other 30 non-broadcast RT addresses. This allows the BU-61580 to simultaneously operate as a full function RT and "snoop" on all or a subset of the bus activity involving the other RTs on a bus. This type of operation is sometimes needed to implement a backup bus controller. The combined RT/Selective Monitor maintains three stack areas in the BU-61580 address space: an RT Command Stack, a Monitor Command Stack, and a Monitor Data Stack. The pointers for the various stacks have fixed locations in the BU-61580 address space.

Selective Message Monitor Memory Organization

Table ? illustrates a typical memory map for the ACE in the Selective Message Monitor. This mode of operation defines several fixed locations in the RAM. These locations allocate in a manner that is compatible with the combined RT/Selective Message Monitor mode. Refer to Table 7 for an example of a typical RT/Selective Message Monitor Memory Map. The fixed memory map consists of two Monitor Command Stack Pointers (location 102 (hex) and 1-6), two Monitor Data Stack Pointers (locations 103 and 107), and a Selective Message Monitor Lookup Table (0280-02FF) based on RT Address, T/$\overline{R}$, and subaddress. Assume a Monitor Command Stack size of 1K words, and a Monitor Data Stack size of 2K words.

TABLE 7. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (shown for 4K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack A (fixed location)
0103	Monitor Data Stack A (fixed location)
0104-105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

Refer to Figure 30 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the BU-61580 will reference the Selective Monitor Lookup Table (a fixed block of addresses) to check for the condition (dis-

FIGURE 30. SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT

able/enabled) of the current command. If disabled, the BU-61580 will ignore (and not store) the current message; if enabled, the BU-61580 will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

Similar to RT mode, a Block Status Word, 16-bit Time Tag Word, and Data Block Pointer store in the Message Descriptor, along with the received 1553 Command Word following reception of the Command Word. The Block Status and Time Tag Words write at both the start and end of the message. The Monitor Block Status Word contains indications of message in-progress or message complete, bus channel, Monitor Data Stack Rollover, RT-to-RT transfer and RT-to-RT transfer errors, message format error, and other error conditions. Figure 23 shows the Message Monitor Block Status Word. The Data Block Pointer references the first word stored in the Monitor Data Stack (the first word following the Command Word) for the current message. The BU-61580 will then proceed to store the subsequent words from the message (possible second Command Word, Data Word(s), Status Word(s)) into consecutive locations in the Monitor Data Stack.

The size of the Monitor Command Stack is programmable to 256, 1K, 4K, or 16k words. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K, or 64K words.

Monitor interrupts may be enabled for Monitor Command Stack Rollover, Monitor Data Stack Rollover, End-of-Message, and/or Monitor Trigger conditions.

MONITOR TRIGGER WORD

There is a Trigger Word Register that provides additional flexibility for the Selective Message Monitor mode. The value of the 16-bit Trigger Word stores in the MT Trigger Word Register. The contents of this register represent the value of the Trigger Command Word. The BU-61580 has programmable options to start or stop the Selective Message Monitor, and/or to issue an interrupt request following receipt of the Trigger Command Word from the 1553 bus.

PROCESSOR AND MEMORY INTERFACE

The BU-65170/61580 provides much flexibility for interfacing to a host processor and optional external memory. Figure 1 shows that there are 14 control signals, 6 of which are dual purpose, for the processor/memory interface. Figures 30 through 35 illustrate six of the configurations that may be used for interfacing a BU-65170 or BU-61580 to a host processor bus. The various possible configurations serve to reduce to an absolute minimum the amount of glue logic required to interface to 8, 16, and 32-bit processor buses. Also included, are features to facilitate interfacing to processors that do not have a "wait state" type of handshake acknowledgement. Finally, the ACE supports a reliable interface to an external dual port RAM. This type of interface minimizes the portion of the available processor bandwidth required to access the 1553 RAM.

The 16-bit buffered mode (Figure 31) is the most common configuration used. It provides a direct, shared RAM interface to a 16-bit or 32-bit microprocessor. In this mode, the ACE's internal address and data buffers provide the necessary isolation between the host processor's address and data buses and the corresponding internal memory buses. In the buffered mode, the 1553 shared RAM address space limit is the BU-65170/61580's internal 4K words of internal RAM. The 16-bit buffered mode provides a pair of pin-programmable options:

(1) The logic sense of the RD/$\overline{WR}$ control input is selectable by the POLARITY_SEL input; for example, write when RD/$\overline{WR}$ is low for Motorola 680X0 processors; write when RD/$\overline{WR}$ is high for the Intel i960 series microprocessors.

(2) By strapping the input signal $\overline{ZERO\_WAIT}$ to logic "1", the ACE terminals may interface to processors that have an acknowledge type of handshake input to accommodate hardware controlled wait states; most current processor chips have such an input. In this case, the BU-65170/61580 will assert its $\overline{READYD}$ output low only after it has latched WRITE data internally or has presented READ data on D15-D0.

By strapping $\overline{ZERO\_WAIT}$ to logic "0", it is possible to easily interface the BU-65170/61580 to processors that **do not** have an acknowledge type of handshake input. An example of such a processor is Analog Device's ADSP2101 DSP chip. In this configuration, the processor can clear its strobe output **before** the completion of access to the BU-65170/61580 internal RAM or register. In this case $\overline{READYD}$ will go high following the rising edge of $\overline{STRBD}$ and will stay high until completion of the transfer. $\overline{READYD}$ will normally be low when $\overline{ZERO\_WAIT}$ is low.

Similar to the 16-bit buffered mode, the 16-bit transparent mode (Figure 32) supports a shared RAM interface to a host CPU. The transparent mode offers the advantage of allowing the buffer RAM size to be expanded to up to 64K words, using external RAM. A disadvantage of the transparent mode is that it requires external address and data buffers to isolate the processor buses from the memory/BU-65170/61580 buses.

A modified version of the transparent mode involves the use of dual port RAM, rather than conventional static RAM. Refer to Figure 33. This allows the host to access RAM very quickly, the only limitation being the access time of the dual port RAM. This configuration eliminates the BU-65170/61580 arbitration delays for memory accesses. The worst case delay time occurs only during a simultaneous access by the host and the BU-65170/61580 1553 logic to the **same memory address**. In general, this will occur very rarely and the delay limit is approximately 250ns.

FIGURE 31. 16-BIT BUFFERED MODE

FIGURE 32. 16-BIT TRANSPARENT MODE

FIGURE 33. 16-BIT TRANSPARENT MODE USING DUAL PORT RAM

Figure 34 illustrates the connections for the 16-bit Direct Memory Access (DMA) mode. In this configuration the host processor, rather than the ACE terminal, arbitrates the use of the address and data buses. The arbitration involves the two DMA output signals Request ($\overline{DTREQ}$) and Acknowledge ($\overline{DTACK}$), and the input signal Grant ($\overline{DTGRT}$). The DMA interface allows the ACE components to interface to large amounts of system RAM. For system address spaces larger than 64K words, it is necessary for the host processor to provide a page register for the upper address bits (above A15) when the BU-65170/61580 accesses the RAM (while asserting $\overline{DTACK}$ low).

FIGURE 34. 16-BIT DIRECT MEMORY ACCESS (DMA) MODE

The internal RAM is accessible through the standard ACE interface ($\overline{\text{SELECT}}$, $\overline{\text{STRBD}}$, $\overline{\text{READYD}}$, etc). The host CPU may access external RAM by the ACE's arbitration logic and output control signals, as illustrated in Figure 34. Alternatively, control of the RAM may be shared by both the host processor and the ACE, as illustrated in Figure 35. The latter requires the use of external logic, but allows the processor to access the RAM directly at the full access speed of the RAM, rather than waiting for the ACE handshake acknowledge output ($\overline{\text{READYD}}$).

FIGURE 35. 16-BIT DMA MODE WITH EXTERNAL LOGIC TO REDUCE PROCESSOR ACCESS TIME TO EXTERNAL RAM

Figure 36 illustrates the 8-bit buffered mode. This interface allows a direct connection to 8-bit microprocessors and 8-bit microcontrollers. As in the 16-bit buffered configuration, the buffer RAM limit is the BU-65170/61580's 4K words of internal RAM. In the 8-bit mode, the host CPU accesses the BU-65170/61580's internal registers and RAM by a pair of 8-bit registers embedded in the ACE interface. The 8-bit interface may be further configured by three strappable inputs: ZERO_WAIT, POLARITY_SEL, and TRIGGER_SEL. By connecting ZERO_WAIT to logic "0", the BU-65170/61580 may be interfaced with minimal "glue" logic to 8-bit microcontrollers, such as the Intel 8051 series, that do not have an Acknowledge type of handshake input. The programmable inputs POLARITY_SEL and TRIGGER_SEL allow the BU-65170/61580 to accommodate the different byte ordering conventions and "A0" logic sense utilized by different 8-bit processor families.

FIGURE 36. 8-BIT BUFFERED MODE

6.0 PROCESSOR INTERFACE TIMING

Figures 37 and 38 illustrate the timing for the host processor to access the ACE's internal RAM or registers in the 16-bit, non-zero wait buffered mode. Figure 37 illustrates the 16-bit buffered, non-zero wait state mode read cycle timing while Figure 38 shows the 16-bit, buffered, non-zero wait state mode write cycle timing.

During a CPU transfer cycle, the signals $\overline{\text{STRBD}}$ and $\overline{\text{SELECT}}$ must be sampled low on the rising edge of the system clock to request access to the BU-65170/61580's internal shared RAM. The transfer will begin on the first rising system clock edge when ($\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$) is low and the 1553 protocol/memory management unit is not accessing the internal RAM. The falling edge of the output signal $\overline{\text{IOEN}}$ indicates the start of the transfer. The signals MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ latch internally on the first falling clock edge after the start of the transfer cycle. The address inputs latch internally on the first rising clock edge after the signal $\overline{\text{IOEN}}$ goes low. Note that the address lines may be latched at any time using the ADDR_LAT input signal.

The output signal $\overline{\text{READYD}}$ will be asserted low on the third rising system clock edge after $\overline{\text{IOEN}}$ goes low. The assertion of $\overline{\text{READYD}}$ low indicates to the host processor that read data is available on the parallel data bus, or that write data has been stored. Now, the CPU should bring the signal $\overline{\text{STRBD}}$ high, completing the transfer cycle.

7.0 MISCELLANEOUS

SELF-TEST

The BU-65170/61580 products incorporate several self-test features. These features include an on-line wrap-around self-test for all messages in BC and RT modes, an off-line wrap-around self-test for BC mode, and several other internal self-test features.

The BC/RT on-line loop test involves a wraparound test of the encoder/decoder and transceiver. The BC off-line self-test involves the encoder/decoder, but not the transceiver. These tests entail checking the received version of every transmitted word for validity (sync, encoding, bit count, parity) and checking the received version of the last transmitted word for a bit-by-bit comparison with the encoded word. The loopback test also fails if there is a timeout of the internal transmitter watchdog timer. Note that the timeout value of the watchdog timer depends on the mode of operation selected (1553A or 1553B). A failure of the loop test results in setting a bit in the message's Block Status Word and, if enabled, will issue an interrupt request. With appropriate host processor software, the BC off-line test is able to exercise the parallel and serial data paths, encoder, decoder, and a substantial portion of the BC protocol and memory management logic.

There are additional built-in self-test features, involving the use of three configuration register bits and the eight test registers. This allows a test of approximately 99% of the J' chip's internal logic. These tests include an encoder test, a decoder test, a register test, a protocol test, and a test of the fail-safe (transmitter timeout) timer.

There is also a test mode. In the test mode, the host processor can emulate arbitrary activity on the 1553 buses by writing to a pair of test registers. The test mode can be operated in conjunction with the Word Monitor mode to facilitate end-to-end self-tests.

RAM PARITY GENERATION AND CHECKING

The architecture of the J' Monolithic is such that the amount of buffered RAM may be extended beyond the 4K words of on-chip J' RAM. For this off-chip buffered RAM, the J' chip includes provisions to implement parity generation and checking. Parity generation and checking provides a mechanism for checking the data integrity of the internal, buffered memory. Contact the factory for the availability of these devices.

In this case, 17-bit, rather than 16-bit, wide buffered RAM would be used. For this RAM, the J' chip will generate the 17th bit (parity bit) for all (host and 1553) write accesses and check the parity bit for all read accesses. If a parity error occurs, an interrupt request may be issued, and the corresponding bit in the Interrupt Status Register would be set.

CPU READING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NON-ZERO WAIT MODE)					
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Address setup time prior to $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (note)	0			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge	10			ns
t3	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access)			85	ns
t3	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (contended access)			2.6	µs
t4	$\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling	0			ns
t5	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to clock falling edge (note)				ns
t6	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ hold time following clock falling edge (note)	0			ns
t7	Address hold time following clock rising edge (note)	20			ns
t8	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@16MHz)	175	187.5	200	ns
t8	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@12MHz)	235	250	265	ns
t9	Output Data valid prior to $\overline{\text{READYD}}$ falling (@16MHz)	33			ns
t9	Output Data valid prior to $\overline{\text{READYD}}$ falling (@12MHz)	54			ns
t10	Clock rising delay to $\overline{\text{READYD}}$ falling			40	ns
t11	$\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time			∞	ns
t12	$\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ rising, $\overline{\text{READYD}}$ rising			31	ns
t13	Output Data hold time following $\overline{\text{STRBD}}$ rising	0			ns
t14	$\overline{\text{STRBD}}$ rising delay to output Data tri-state			25	ns

FIGURE 37. CPU READING RAM (SHOWN FOR 16-BIT, BUFFERED, NON-ZERO WAIT STATE MODE)

CPU WRITING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NON-ZERO WAIT MODE)					
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Address and input Data setup time prior to $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (note)	0			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge	10			ns
t3	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access)			85	ns
t3	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (contended access)			2.6	µs
t4	$\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling	0			ns
t5	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to clock falling edge (note)				ns
t6	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ hold time following clock falling edge (note)	0			ns
t7	Address and Data hold time following clock rising	20			ns
t8	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@16MHz)	175	187.5	200	ns
t8	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@12MHz)	235	250	265	ns
t9	Clock rising delay to $\overline{\text{READYD}}$ falling			40	ns
t10	$\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time			∞	ns
t11	$\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ rising, $\overline{\text{READYD}}$ rising			31	ns

FIGURE 38. CPU WRITING RAM (SHOWN FOR 16-BIT, NON-ZERO WAIT STATE, BUFFERED MODE)

1.0 BU-65170 SIGNAL DESCRIPTIONS

BU-65170/61580 70-PIN PACKAGE

PROCESSOR/MEMORY INTERFACE AND CONTROL (15)		
SIGNAL NAME	PIN	DESCRIPTION
TRANSPARENT/ $\overline{\text{BUFFERED}}$ (I)	64	Used to select between the Transparent/DMA mode (when strapped to logic 1) and the Buffered mode (when strapped to logic 0) for the host processor interface.
$\overline{\text{STRBD}}$ (I)	4	Strobe Data. Used with $\overline{\text{SELECT}}$ to initiate and control the data transfer cycle between the host processor and the BU-65170/61580.
$\overline{\text{SELECT}}$ (I)	3	Generally connected to a CPU address decoder output to select the BU-65170/61580 for a transfer to/from either RAM or register. May be tied to $\overline{\text{STRBD}}$.
MEM/$\overline{\text{REG}}$ (I)	5	Memory/Register. Generally connected to either a CPU address line or address decoder output. Selects between memory access (MEM/$\overline{\text{REG}}$ = 1) or register access (MEM/$\overline{\text{REG}}$ = 0).
RD/$\overline{\text{WR}}$ (I)	6	Read/Write. For a host processor access, selects between reading and writing. In the 16-bit buffered mode, if polarity select is logic 0, them RD/$\overline{\text{WR}}$ is low (logic 0) for read accesses and high (logic 1) for write accesses. If polarity select is logic 1 or the configuration of the interface is a mode other than 16-bit buffered mode, then RD/$\overline{\text{WR}}$ is high (logic 1) for read accesses and low (logic 0) for write accesses.
$\overline{\text{IOEN}}$ (O)	67	Tri-state control for external address and data buffers. Generally not needed in the buffered mode. When low, external buffers should be enabled to allow the host processor access to the BU-65170/61580's RAM and registers.
$\overline{\text{READYD}}$ (O)	66	Handshake output to host processor. For a non-zero wait state read access, signals that data is available to be read on D15 through D0. For a non-zero wait state write cycle, signals the completion of data transfer to a register or RAM location. In the buffered zero wait state mode, active high output signal (following the rising edge of $\overline{\text{STRBD}}$) used to indicate the latching of address and data (write only) and that an internal transfer between the address/data latches and the ram/registers is on-going.
$\overline{\text{INT}}$ (O)	65	Interrupt request output. If the LEVEL/$\overline{\text{PULSE}}$ interrupt bit (bit 3) of Configuration Register #2 is low, a negative pulse of approximately 500 ns in width is output on $\overline{\text{INT}}$. If bit 3 is high, a low level interrupt request output will be asserted on $\overline{\text{INT}}$.

PROCESSOR/MEMORY INTERFACE AND CONTROL (15)		
SIGNAL NAME	PIN	DESCRIPTION
$\overline{\text{DTREQ}}$ (O) /16/$\overline{8}$ (I)	31	Data Transfer Request or 16-bit/8-bit Transfer Mode Select. In transparent mode, active low output signal used to request access to the processor interface bus (address,data, and control buses). In buffered mode, input signal used to select between the 16-bit data transfer mode (16/$\overline{8}$ = Logic 1) and the 8 bit data transfer mode (16/$\overline{8}$ = Logic 0).
$\overline{\text{DTGRT}}$ (I) /MSB/LSB (I)	26	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In transparent mode, active low input signal asserted, in response to the $\overline{\text{DTREQ}}$ output, to indicate granted control, of the processor interface bus, to the BU-65170/61580. In 8-bit buffered mode, input signal used to indicate which byte is being transferred (MSB or LSB). The POLARITY_SEL input controls the logic sense of MSB/LSB. (Note: only the 8-bit buffered mode uses MSB/LSB.) See description of POLARITY_SEL signal. N/C in 16-bit buffered mode.
$\overline{\text{DTACK}}$ (O)/ POLARITY_SEL (I)	32	Data Transfer Acknowledge or Polarity Select. In transparent mode, active low output signal used to indicate acceptance of the processor interface bus in response to a data transfer grant ($\overline{\text{DTGRT}}$). In 16-bit buffered mode (TRANSPARENT/ $\overline{\text{BUFFERED}}$ = LOGIC 0 AND 16/$\overline{8}$ = LOGIC 1), input signal used to control the logic sense of the RD/$\overline{\text{WR}}$ signal. When connecting POLARITY_SEL to a logic 1, RD/$\overline{\text{WR}}$ should be asserted high (logic 1) for a read operation and low (logic 0) for a write operation. When connecting POLARITY_SEL to a logic 0, RD/$\overline{\text{WR}}$ should be asserted low (logic 0) for a read operation and high (logic 1) for a write operation. In 8-bit buffered mode (TRANSPARENT/BUFFERED = LOGIC 0 AND 16/$\overline{8}$ = LOGIC 0), input signal used to control the logic sense of the MSB/$\overline{\text{LSB}}$ signal. When connecting POLARITY_SEL connected to a logic 0, MSB/$\overline{\text{LSB}}$ should be asserted low (logic 0) to indicate the transfer of the least significant byte and high (logic 1) to indicate the transfer of the most significant byte. When connecting POLARITY_SEL to a logic 1, MSB/$\overline{\text{LSB}}$ should be asserted high (logic 1) to indicate the transfer of the least significant byte and low (logic 0) to indicate the transfer of the most significant byte.
$\overline{\text{MEMENA-OUT}}$ (O)	28	Memory Enable Output. Asserted low during both host processor and 1553 protocol/memory management memory transfer cycles. Used as a memory chip select ($\overline{\text{CS}}$) signal for external RAM in the transparent mode.

PROCESSOR/MEMORY INTERFACE AND CONTROL (15)		
SIGNAL NAME	PIN	DESCRIPTION
MEMENA-IN (I) TRIGGER_SEL (I)	33	Memory Enable Input or Trigger Select. In transparent mode, MEMENA-IN is an active low Chip Select (CS) input to the 4K X 16 of internal shared RAM. When only using internal RAM, connect directly to MEMENA-OUT. In 8-bit buffered mode, the input signal (TRIGGER_SEL) indicates the order of byte pairs transfer to or from the BU-65170/61580 by the host processor. This signal has no operation (can be N/C) in the 16-bit buffered mode. In the 8-bit buffered mode, TRIGGER_SEL should be asserted high (logic 1) if the byte order for both read operations and write operations is MSB with a following LSB. TRIGGER_SEL should be asserted low (logic 0) if the byte order for both read operations and write operations is LSB with a following MSB.
MEMOE (O)/ ADDR_LAT (I)	29	Memory Output Enable or Address Latch. In transparent mode, MEMOE output will be used to enable data outputs for external RAM read cycles (normally connected to the OE signal on external RAM chips). In buffered mode, ADDR_LAT input will be used to configure address buffers in latched mode (when low) or transparent mode (when high).
MEMWR (O) /ZERO_WAIT (I)	30	Memory Write or Zero Wait State. In transparent mode, active low output signal (MEMWR) will be asserted low during memory write transfers to strobe data into internal or external RAM (normally connected to the WR signal on external RAM chips). In buffered mode, input signal (ZERO_WAIT) will be used to select between the zero wait state mode (ZERO_WAIT = logic 0) and the non-zero wait state mode (ZERO_WAIT = logic 1).

POWER AND GROUND (8)		
SIGNAL NAME	PIN	DESCRIPTION
+5V LOGIC	54	Logic +5V Supply
LOGIC GND	18	Logic Ground
-15(-12)VA	70	CH. A -15V(-12V) Supply*
+5VA	68	CH. A +5V Supply
GNDA	69	CH. A Transceiver Ground
-15(-12)VB	36	CH. B -15V(-12V) Supply*
+5VB	38	CH. B +5V Supply
GNDB	37	CH. B Transceiver Ground

NOTE: * No Connects (N/Cs) for BU-65170/61580 and TX_INH input for BU-65170/61580X6.

DATA BUS (16)		
SIGNAL NAME	PIN	DESCRIPTION
D15 (MSB)	62	16-bit bidirectional data bus. This bus interfaces the host processor to the internal registers and 4K words of RAM. In addition, in the transparent mode, this bus allows data transfers to take place between the internal protocol/memory management logic and up to 64K X 16 of external RAM. Most of the time, the outputs for D15 through D0 are in their high impedance state. They drive outward when the host CPU reads the internal RAM or registers, or when the protocol/memory management logic is accessing (either reading or writing) internal RAM or writing to external RAM when in the transparent mode. A logic 0 output level on the signal IOEN indicates a CPU access. In the transparent mode
D14	61	
D13	60	
D12	59	
D11	58	
D10	57	
D09	56	
D08	55	
D07	53	
D06	52	
D05	51	
D04	50	
D03	49	
D02	48	
D01	47	
D00 (LSB)	46	

ADDRESS BUS (16)		
SIGNAL NAME	PIN	DESCRIPTION
A15 (MSB)	8	16-bit bidirectional address bus. In both the buffered and transparent modes, the host CPU accesses the BU-65170/61580 registers and 4K words of internal RAM by A11 through A0. In the buffered mode, A15-A0 are inputs only. In the transparent mode, A15-A0 are inputs during CPU accesses and drive outward (towards the CPU) when the 1553 protocol/memory management logic accesses up to 64K X 16 of external RAM. The address bus drives outward only in the transparent when the signal DTACK is low (indicating that the 61580 has control of the processor interface bus) and IOEN is high (indicating that this is not a CPU access). Most of the time, including immediately after power turn-on RESET, the A15-A0 outputs will be in their disabled (high impedance) state.
A14	9	
A13	10	
A12	11	
A11	12	
A10	13	
A09	14	
A08	15	
A07	16	
A06	17	
A05	20	
A04	21	
A03	22	
A02	23	
A01	24	
A00	25	

1553 ISOLATION TRANSFORMER INTERFACE (4)		
SIGNAL NAME	PIN	DESCRIPTION
TX/RX-A (I/O)	1	Analog Transmit/Receive Input/Outputs. Connect directly to 1553 isolation transformers.
$\overline{\text{TX/RX-A}}$ (I/O)	2	
TX/RX-B (I/O)	34	
$\overline{\text{TX/RX-B}}$ (I/O)	35	

RT ADDRESS (6)		
SIGNAL NAME	PIN	DESCRIPTION
RTAD4 (MSB) (I)	43	Remote Terminal Address Inputs
RTAD3 (I)	42	
RTAD2 (I)	41	
RTAD1 (I)	40	
RTAD0 (LSB) (I)	39	
RTADP (I)	44	Remote Terminal Address Parity. Must provide odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands.

MISCELLANEOUS (7)		
SIGNAL NAME	PIN	DESCRIPTION
CLOCK IN (I)	19	16MHz (or optional 12MHz) clock input.
$\overline{\text{MSTCLR}}$ (I)	7	Master Clear. Negative true Reset input, normally asserted low following power turn-on. Requires a minimum ??ns negative pulse to reset all internal logic to its "power turn-on" state.
$\overline{\text{INCMD}}$ (O)	45	In Command. In BC mode, asserted low throughout processing cycle for each message. In RT mode or Message Monitor mode, asserted low following receipt of Command Word and kept low until completion of current message sequence. In Word Monitor mode, goes low following MONITOR START command, kept low while monitor is on-line, goes high following RESET command.

MISCELLANEOUS (7)		
SIGNAL NAME	PIN	DESCRIPTION
$\overline{\text{SSFLAG}}$ (I)/ EXT_TRIG (I)	27	Subsystem Flag or External Trigger input. In the Remote Terminal mode, asserting this input , will set the Subsystem Flag bit in the BU-65170/61580's RT Status Word. A low on the $\overline{\text{SSFLAG}}$ input overrides a logic "1" of the respective bit (bit 8) of Configuration Register #1. In the Bus Controller mode, An enabled external BC Start option (bit 7 of Configuration Register #1) and a low-to-high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the Monitor mode, an enabled external trigger (bit 7 of Configuration Register #1) and a low-to-high transition on this input will issue a monitor trigger.
TAG_CLK (I)	63	External Time Tag Clock input. Use may be designated by bits 7, 8, and 9 of Configuration Register #2. If not used, should be connected to +5V or ground.
TX_INH_A (I)	70	Option for BU-65170/61580X6. Inhibits (disables) the respective (A/B) MIL-STD-1553 transmitter when asserted to logic "1."
TX_INH_B (I)	36	

BU61580/65170 PIN LISTING (70-Pin DIP, Flatpack, or J-Lead)	
PIN	NAME
1	TX/RX-A
2	$\overline{\text{TX/RX-A}}$
3	$\overline{\text{SELECT}}$
4	$\overline{\text{STRBD}}$
5	$\overline{\text{MEM/REG}}$
6	$\overline{\text{RD/WR}}$
7	$\overline{\text{MSTCLR}}$
8	A15
9	A14
10	A13
11	A12
12	A11
13	A10
14	A09
15	A08
16	A07
17	A06
18	GND
19	CLK
20	A05
21	A04
22	A03
23	A02
24	A01
25	A00
26	$\overline{\text{DTGRT}}$/MSB/LSB
27	$\overline{\text{SSFLAG}}$/EXT_TRIG
28	$\overline{\text{MEMENA\_OUT}}$
29	$\overline{\text{MEMOE}}$/ADDR_LAT
30	$\overline{\text{MEMWR}}$/ZEROWAIT
31	$\overline{\text{DTREQ}}$/16/$\overline{8}$
32	$\overline{\text{DTACK}}$/POLARITY_SEL
33	$\overline{\text{MEMENA\_IN}}$/TRIGGER_SEL
34	TX/RX-B
35	$\overline{\text{TX/RX-B}}$
36	-VB
37	GNDB
38	+5VB
39	RTAD0
40	RTAD1
41	RTAD2
42	RTAD3
43	RTAD4
44	RTADP
45	$\overline{\text{INCMD}}$
46	D00
47	D01
48	D02
49	D03
50	D04
51	D05
52	D06
53	D07
54	+5V LOGIC
55	D08

BU61580/65170 PIN LISTING (70-Pin DIP, Flatpack, or J-Lead)	
PIN	NAME
56	D09
57	D10
58	D11
59	D12
60	D13
61	D14
62	D15
63	TAG_CLK
64	TRANSPARENT/$\overline{\text{BUFFERED}}$
65	$\overline{\text{INT}}$
66	$\overline{\text{READYD}}$
67	$\overline{\text{IOEN}}$
68	+5VA
69	GNDA
70	-VA

4.10 INTERFACE TO MIL-STD-1553 BUS

Figure 39 illustrates the interface from the various versions of the ACE series terminals to a 1553 bus. The figure also indicates connections for both direct (short stub) and transformer (long stub) coupling, plus the peak-to-peak voltage levels that appear at various points (when transmitting).

Table 8 lists the characteristics of the required isolation transformers for the various ACE terminals, the DDC, and the Beta Transformer Technology Corporation corresponding part number, and the MIL (DESC) drawing number (if applicable). Beta Transformer Technology is a direct subsidiary of DDC.

For both coupling configurations, the isolation transformer is the transformer that interfaces directly to the ACE component. For the transformer (long stub) coupling configuration, the transformer that interfaces the stub to the bus is the coupling transformer. The turns ratio of the isolation transformer varies, depending upon the peak-to-peak output voltage of the specific ACE terminal.

The transmitter voltage of each model of the BU-65170/61580 varies directly as a function of the power supply voltage. The turns ratios of the respective transformers will yield a secondary voltage of approximately 28 volts peak-to-peak on the outer taps (used for direct coupling) and 20 volts peak-to-peak on the inner taps (used for stub coupling).

In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is 1.0 to 1.4. Both coupling configurations require an isolation resistor to be in series with each leg connecting to the 1553 bus; this protects the bus against short circuit conditions in the transformers, stubs, or terminal components.

TABLE 8. ISOLATION TRANSFORMER GUIDE

ACE PART NUMBER	TURNS RATIO		RECOMENDED XFORMER	
	DIRECT COUPLED	XFORMER COUPLED	PLUG-IN	SURFACE MOUNT
BU-65170X1 or BU-61580X1	1.41:1	2:1	BUS-25679, B-2203, M21038/27-02	B-2387, M21038/27-12, B-2343, M21038/27-17, LPB-5002, LPB-5009, HLP-6002, HLP-6009
BU-65170X2 or BU-61580X2	1.25:1	1.179:1	BUS-29854, B-2204, M21038/27-03	B-2388, M21038/27-13, B-2344, M21038/27-18, LPB-5004, LPB-5011, HLP-6004, HLP-6011
BU-65170X3 or BU-61580X3	1.25:1	1:1.79	B-3067	B-3072

Notes:
(1) Shown for one of two redundant buses that interface to the BU-65170 or BU-61580.
(2) Transmitted voltage level on 1553 bus is 6 Vp-p min, 7 Vp-p nominal, 9 Vp-p max.
(3) Required tolerance on isolation resistors is 2%. Instantaneous power dissipation (when transmitting) is approximately 0.5 W (typ), 0.8 W (max).
(4) Transformer pin numbering is correct for the DDC (e.g., BUS-25679) transformers. For the Beta transformers (e.g., B-2203) or the QPL-21038-31 transformers (e.g., M21038/27-02), the winding sense and turns ratio are mechanically the same, but with reversed pin numbering; therefore, it is necessary to reverse pins 8 and 4 or pins 7 and 5 for the Beta or QPL transformers (Note: DDC transformer part numbers begin with a BUS- prefix, while Beta transformer part numbers begin with a B- prefix).

FIGURE 39. BU-65170/61580 INTERFACE TO A 1553 BUS (1 of 2)

FIGURE 39. BU-65170/61580 INTERFACE TO A 1553 BUS (2 of 2)

FIGURE 40

FIGURE 41

FIGURE 42

ORDERING INFORMATION

BU-61580D3-110

Test Criteria:
0 = None

Screening:
0 = Standard DDC Procedures
1 = Full 883B Screening
2 = 883B Screening without QCI Testing

Temperature Range:
0 = –55 to +125 °C
0 = –25 to +85 °C
3 = 0 to +70 °C

Voltage/Transceiver Option:
0 = Transeiverless
1 = +5/-15V (1760 compliant)
2 = +5/-12V
3 = +5V only
6 = +5V only with Tx Inhibits brought out on negative supply pins

Package:
D = Dip
F = Flatpack
J = J-Lead
P = PGA

Product Type:
65170 = 70 Pin RT
65171 = 70 Pin RT with latchable RT address option
61580 = 70 Pin BC/RT/MT
61581 = 70 Pin BC/RT/MT with latchable RTaddress option
65620 = 144 pin monolithic

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