



FDD6760A

N-Channel PowerTrench® MOSFET

25 V, 3.2 mΩ

Features

- Max $r_{DS(on)}$ = 3.2 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 27\text{ A}$
- Max $r_{DS(on)}$ = 6.0 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 21\text{ A}$
- 100% UIL test
- RoHS Compliant

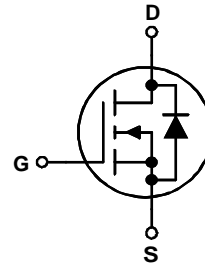
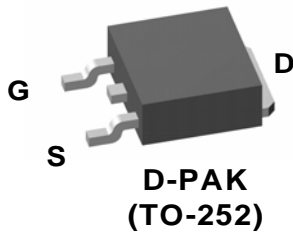


General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.

Applications

- Vcore DC-DC for Desktop Computers and Servers
- VRM for Intermediate Bus Architecture



MOSFET Maximum Ratings $T_C = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$	50	A
	-Continuous (Silicon limited) $T_C = 25\text{ °C}$	131	
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	27	
	-Pulsed	200	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	72	mJ
P_D	Power Dissipation $T_C = 25\text{ °C}$	65	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	3.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD6760A	FDD6760A	D-PAK (TO-252)	13 "	12 mm	2500 units

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Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		16		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 27\text{ A}$		2.3	3.2	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 21\text{ A}$		4.4	6.0	
		$V_{GS} = 10\text{ V}, I_D = 27\text{ A}, T_J = 150\text{ }^\circ\text{C}$		3.5	4.9	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 27\text{ A}$		186		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		2380	3170	pF
C_{oss}	Output Capacitance			525	700	pF
C_{rss}	Reverse Transfer Capacitance			470	710	pF
R_g	Gate Resistance		$f = 1\text{ MHz}$		1.3	

Switching Characteristics

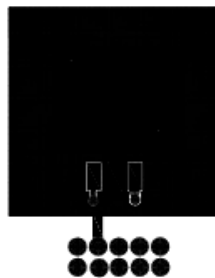
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{ V}, I_D = 27\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		10	20	ns	
t_r	Rise Time			9	18	ns	
$t_{d(off)}$	Turn-Off Delay Time			28		ns	
t_f	Fall Time			6		ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		44	62	nC
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to } 5\text{ V}$	$V_{DD} = 13\text{ V},$ $I_D = 17\text{ A}$	25	35	nC
Q_{gs}	Gate to Source Charge			6		nC	
Q_{gd}	Gate to Drain "Miller" Charge			9.9		nC	

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 3.1\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 27\text{ A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 27\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		21	34	ns
Q_{rr}	Reverse Recovery Charge			8	16	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) $40\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $96\text{ }^\circ\text{C/W}$ when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3: E_{AS} of 72 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 12\text{ A}$, $V_{DD} = 23\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 29\text{ A}$.

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Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

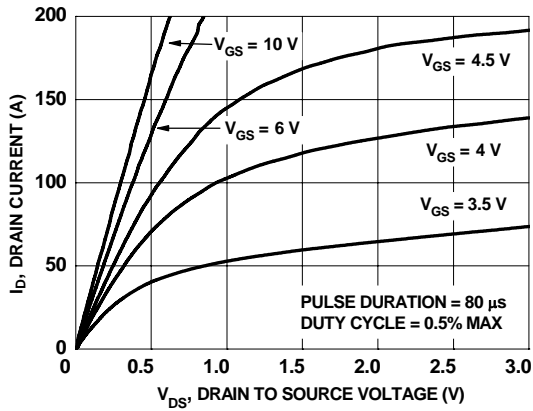


Figure 1. On-Region Characteristics

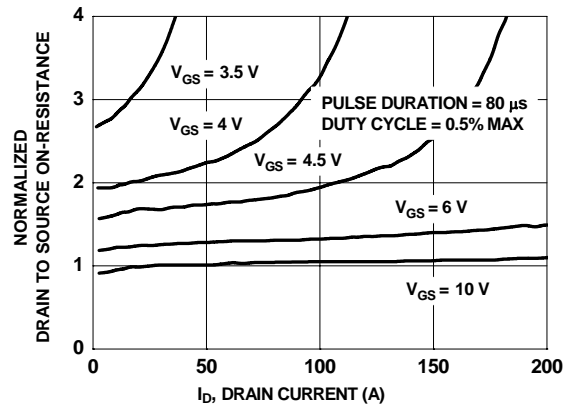


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

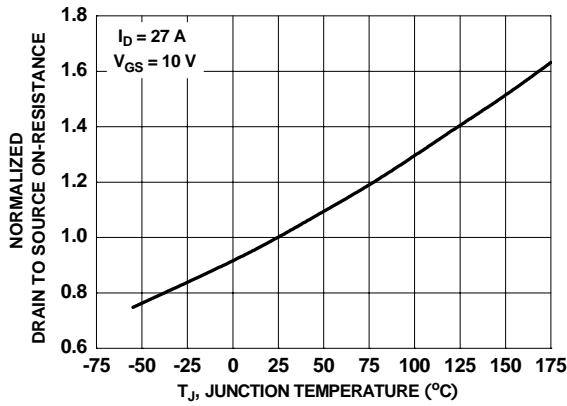


Figure 3. Normalized On-Resistance vs Junction Temperature

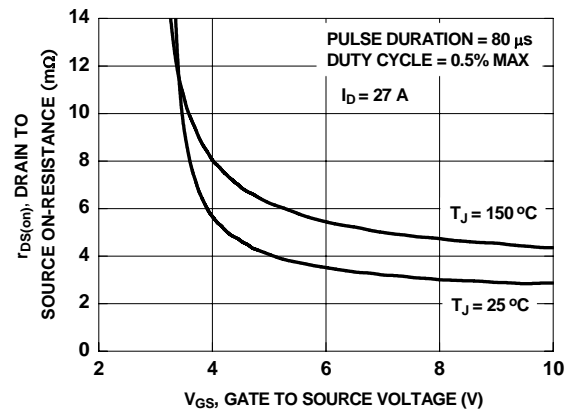


Figure 4. On-Resistance vs Gate to Source Voltage

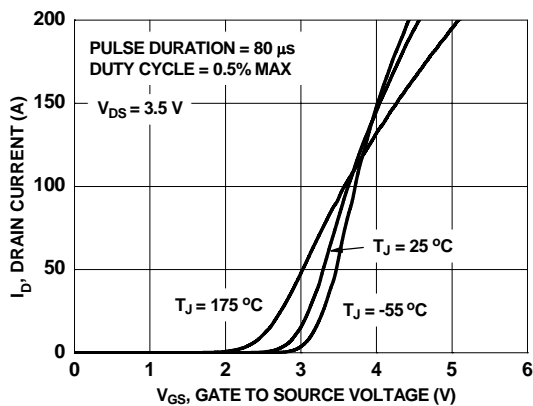


Figure 5. Transfer Characteristics

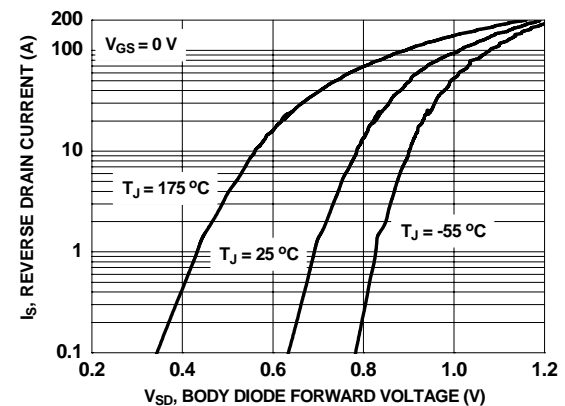


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

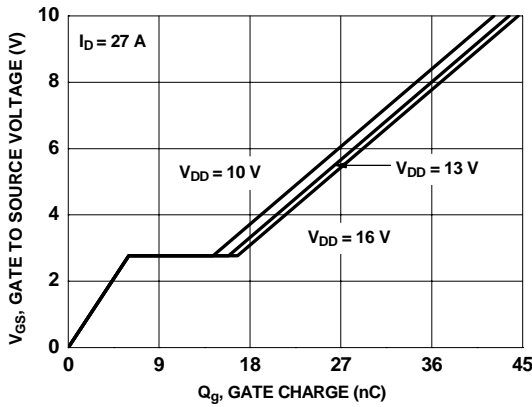


Figure 7. Gate Charge Characteristics

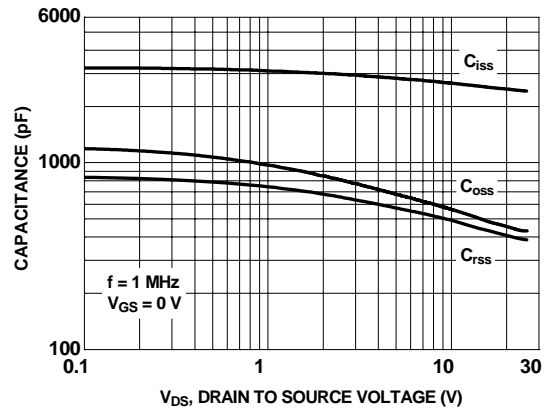


Figure 8. Capacitance vs Drain to Source Voltage

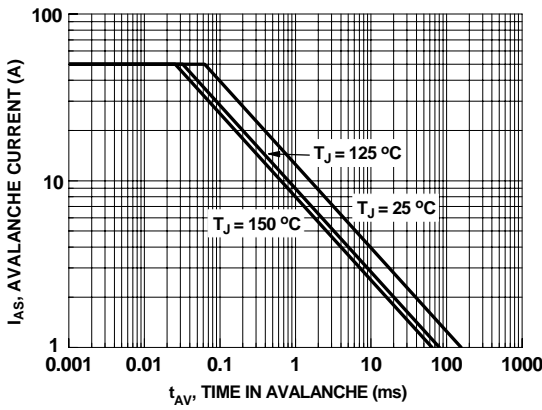


Figure 9. Unclamped Inductive Switching Capability

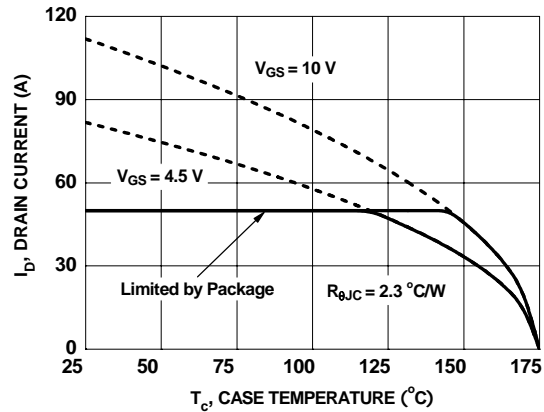


Figure 10. Maximum Continuous Drain Current vs Case Temperature

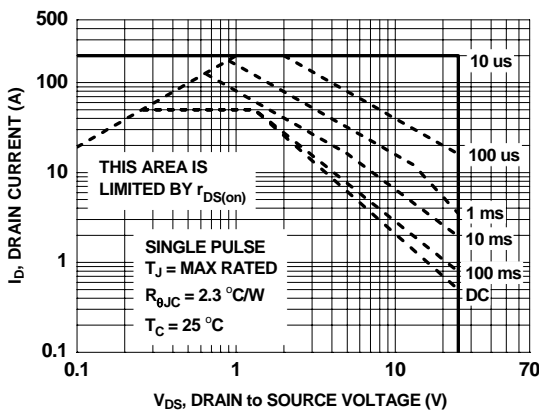


Figure 11. Forward Bias Safe Operating Area

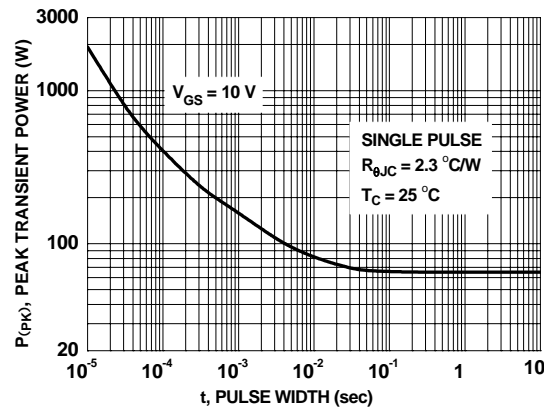


Figure 12. Single Pulse Maximum Power Dissipation

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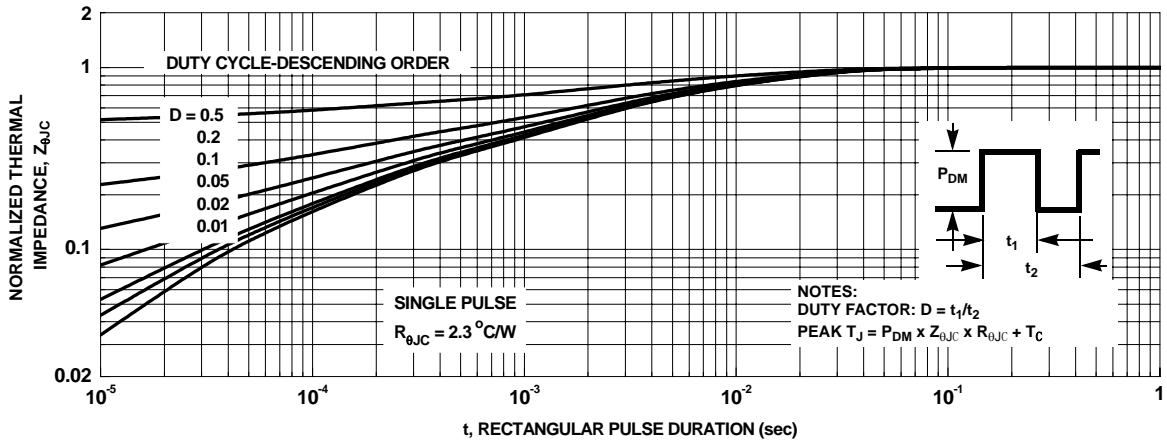


Figure 13. Transient Thermal Response Curve

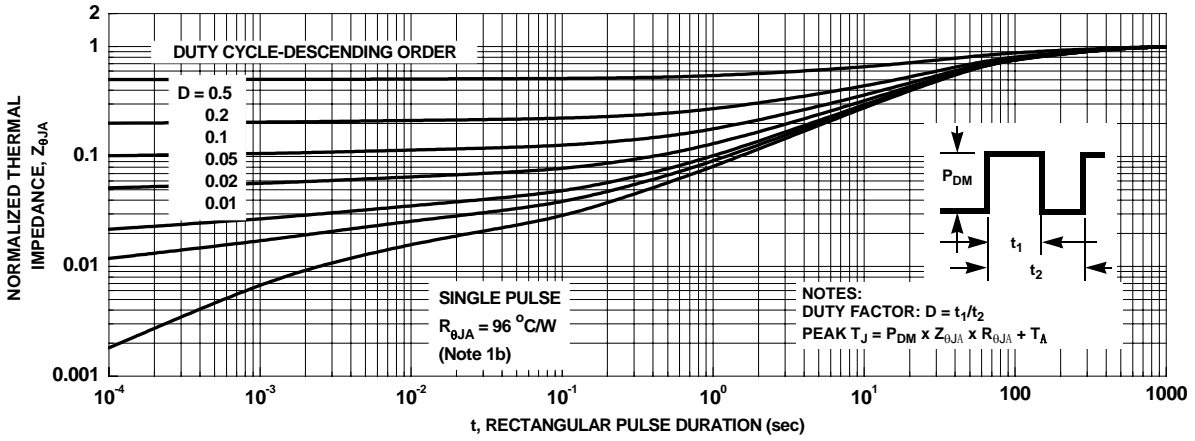


Figure 14. Transient Thermal Response Curve

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