

ESD5Z2.5T1/D SERIES

Transient Voltage Suppressors

Micro-Packaged Diodes for ESD Protection

The ESD5Z Series is designed to protect voltage sensitive components from ESD and transient voltage events. Excellent clamping capability, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its small size, it is suited for use in cellular phones, portable devices, digital cameras, power supplies and many other portable applications.

Specification Features:

- Low Clamping Voltage
- Small Body Outline Dimensions:
0.047" x 0.032" (1.20 mm x 0.80 mm)
- Low Body Height: 0.028" (0.7 mm)
- Stand-off Voltage: 2.5 V – 12 V
- Peak Power up to 240 Watts @ 8 x 20 μ s Pulse
- Low Leakage
- Response Time is Typically < 1 ns
- ESD Rating of Class 3 (> 16 kV) per Human Body Model
- IEC61000-4-2 Level 4 ESD Protection
- IEC61000-4-4 Level 4 EFT Protection
- Pb-Free Packages are Available

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V-0

LEAD FINISH: 100% Matte Sn (Tin)

MOUNTING POSITION: Any

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

Device Meets MSL 1 Requirements

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|----------------|----------------------|------------------|
| IEC 61000-4-2 (ESD) Contact Air | | ± 30 ± 30 | kV |
| IEC 61000-4-4 (EFT) | | 40 | A |
| ESD Voltage Per Human Body Model Per Machine Model | | 16 400 | kV V |
| Total Power Dissipation on FR-5 Board (Note 1) @ $T_A = 25^\circ\text{C}$ | P_D | 200 | mW |
| Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Lead Solder Temperature – Maximum (10 Second Duration) | T_L | 260 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

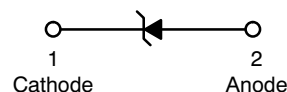
1. FR-5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.



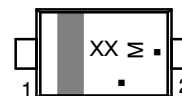
ON Semiconductor®

<http://onsemi.com>



SOD-523
CASE 502
PLASTIC

MARKING DIAGRAM



XX = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------|--------------------|------------------|
| ESD5ZxxxT1 | SOD-523 | 3000/Tape & Reel |
| ESD5ZxxxT1G | SOD-523 Pb-Free | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

See specific marking information in the device marking column of the Electrical Characteristics tables starting on page 2 of this data sheet.

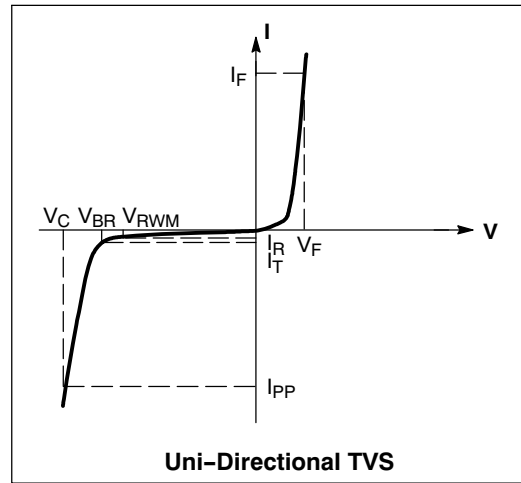
ESD5Z2.5T1 SERIES

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter |
|-----------|---|
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Working Peak Reverse Voltage |
| I_R | Maximum Reverse Leakage Current @ V_{RWM} |
| V_{BR} | Breakdown Voltage @ I_T |
| I_T | Test Current |
| I_F | Forward Current |
| V_F | Forward Voltage @ I_F |
| P_{pk} | Peak Power Dissipation |
| C | Max. Capacitance @ $V_R = 0$ and $f = 1\text{ MHz}$ |

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, $V_F = 1.1\text{ V Max.}$ @ $I_F = 10\text{ mA}$ for all types)

| Device** | Device Marking | V_{RWM} (V) | I_R (μA) @ V_{RWM} | V_{BR} (V) @ I_T (Note 2) | I_T mA | V_C (V) @ $I_{PP} = 5.0\text{ A}^\dagger$ | V_C (V) @ Max I_{PP}^\dagger | I_{PP} (A) [†] | P_{pk} (W) [†] | C (pF) | V_C Per IEC61000-4-2 (Note 3) |
|----------------|----------------|---------------|-------------------------------------|-------------------------------|----------|---|----------------------------------|---------------------------|---------------------------|--------|------------------------------------|
| | | Max | Max | Min | | Typ | Max | Max | Max | Typ | |
| ESD5Z2.5T1, G* | ZD | 2.5 | 6.0 | 4.0 | 1.0 | 6.5 | 10.9 | 11.0 | 120 | 145 | Figures 1 and 2 See Below (Note 4) |
| ESD5Z3.3T1, G* | ZE | 3.3 | 0.05 | 5.0 | 1.0 | 8.4 | 14.1 | 11.2 | 158 | 105 | |
| ESD5Z5.0T1, G* | ZF | 5.0 | 0.05 | 6.2 | 1.0 | 11.6 | 18.6 | 9.4 | 174 | 80 | |
| ESD5Z6.0T1, G* | ZG | 6.0 | 0.01 | 6.8 | 1.0 | 12.4 | 20.5 | 8.8 | 181 | 70 | |
| ESD5Z7.0T1, G* | ZH | 7.0 | 0.01 | 7.5 | 1.0 | 13.5 | 22.7 | 8.8 | 200 | 65 | |
| ESD5Z12T1, G* | ZM | 12 | 0.01 | 14.1 | 1.0 | 17 | 25 | 9.6 | 240 | 55 | |

*The "G" suffix indicates Pb-Free package available.

**Other voltages available upon request.

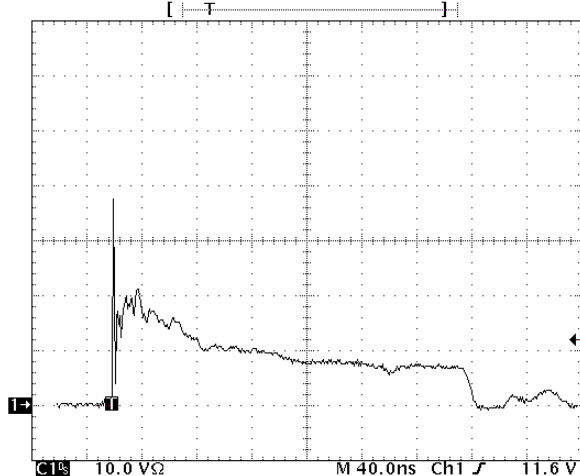
†Surge current waveform per Figure 5.

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C .

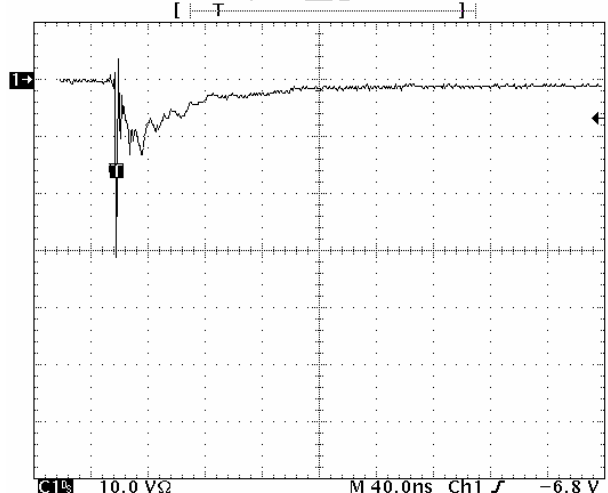
3. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

4. ESD5Z5.0T1G shown below. Other voltages available upon request.

Tek Run: 1.25GS/s Sample 1102



Tek Run: 1.25GS/s Sample 1102



ESD5Z2.5T1 SERIES

IEC61000-4-2 Spec
查询 ESD5Z2.5T1-D"供应商

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

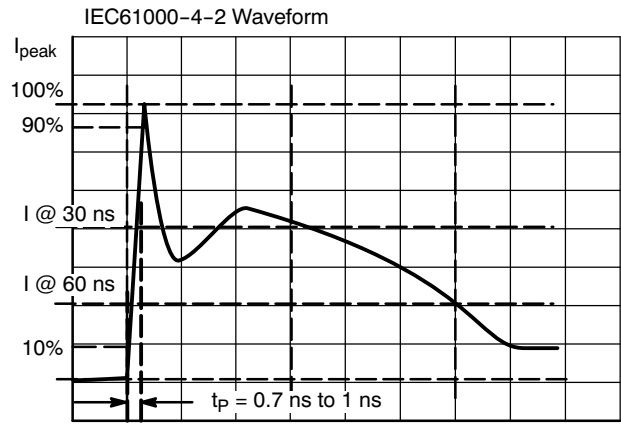


Figure 3. IEC61000-4-2 Spec

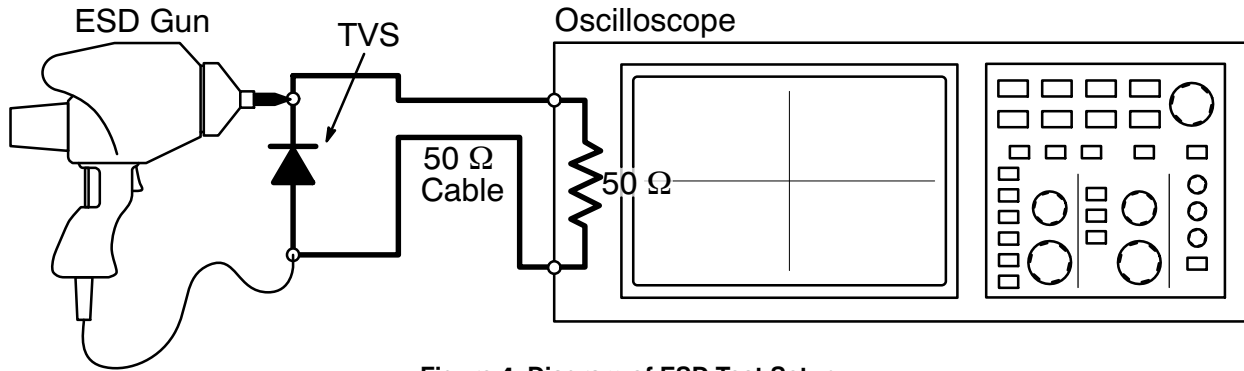


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note
AND8308/D – Interpretation of Datasheet Parameters
for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

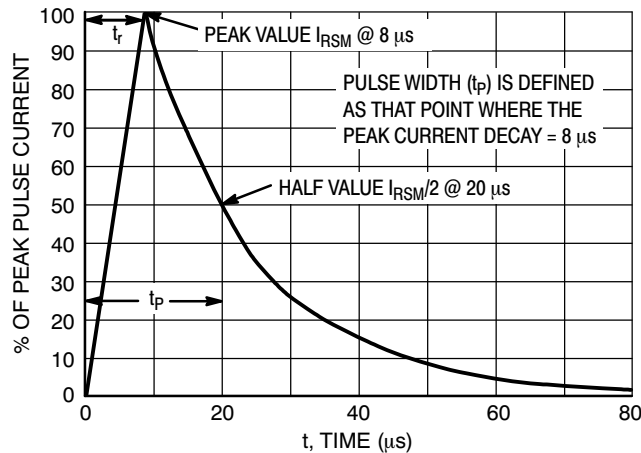


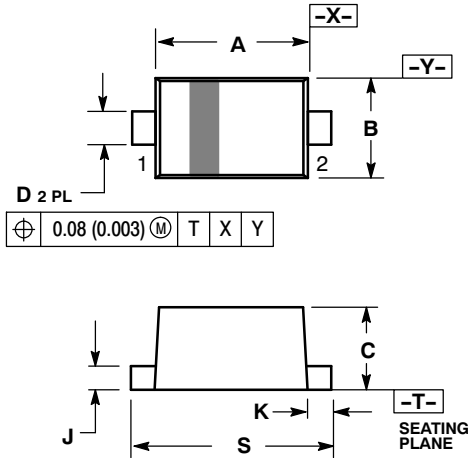
Figure 5. 8 X 20 μ s Pulse Waveform

ESD5Z2.5T1 SERIES

[查询"ESD5Z2.5T1-D"供应商](#)

PACKAGE DIMENSIONS

SOD-523
CASE 502-01
ISSUE C

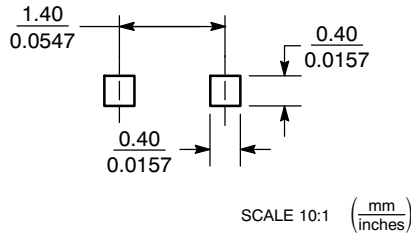


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|--------|--------|--------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.10 | 1.20 | 1.30 | 0.043 | 0.047 | 0.051 |
| B | 0.70 | 0.80 | 0.90 | 0.028 | 0.032 | 0.035 |
| C | 0.50 | 0.60 | 0.70 | 0.020 | 0.024 | 0.028 |
| D | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| J | 0.07 | 0.14 | 0.20 | 0.0028 | 0.0055 | 0.0079 |
| K | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| S | 1.50 | 1.60 | 1.70 | 0.059 | 0.063 | 0.067 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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