

Octal registered transceiver (3-State)

74ABT2952

查询 54ABT2952/BKA 供应商

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT2952 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{\text{CEXX}}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{\text{OEXX}}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

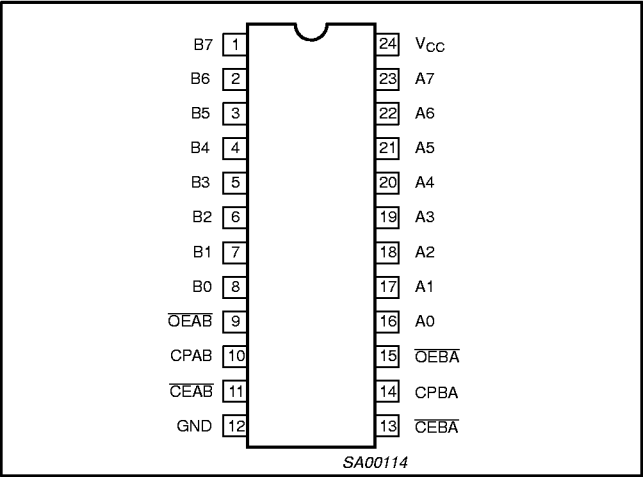
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}$; $\text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	$C_{\text{L}} = 50\text{pF}$; $V_{\text{CC}} = 5\text{V}$	5.7	ns
C_{IN}	Input capacitance	$V_{\text{I}} = 0\text{V}$ or V_{CC}	4	pF
$C_{\text{I/O}}$	I/O capacitance	Outputs disabled; $V_{\text{O}} = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$	110	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	−40°C to +85°C	74ABT2952 N	74ABT2952 N	SOT222-1
24-Pin plastic SO	−40°C to +85°C	74ABT2952 D	74ABT2952 D	SOT137-1
24-Pin Plastic SSOP Type II	−40°C to +85°C	74ABT2952 DB	74ABT2952 DB	SOT340-1
24-Pin Plastic TSSOP Type I	−40°C to +85°C	74ABT2952 PW	74ABT2952PW DH	SOT355-1

PIN CONFIGURATION



PIN DESCRIPTION

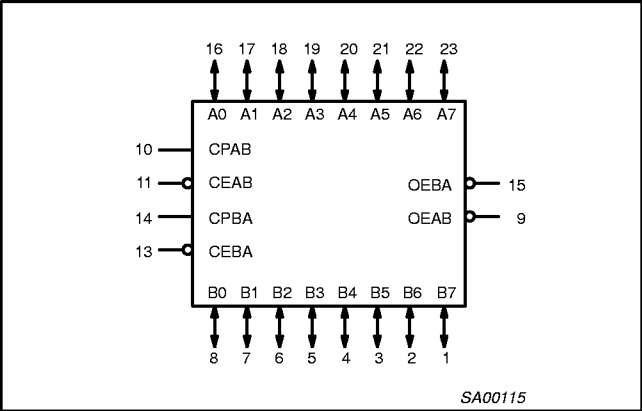
PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{\text{CEAB}}$ / $\overline{\text{CEBA}}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
1, 2, 3, 4, 5, 6, 7, 8	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{\text{OEAB}}$ / $\overline{\text{OEBA}}$	Output enable inputs
12	GND	Ground (0V)
24	VCC	Positive supply voltage

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LOGIC SYMBOL



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{\text{CE}}\text{XX}$		
X	X	H	NC	Hold data
L H	$\uparrow$ $\uparrow$	L L	L H	Load data

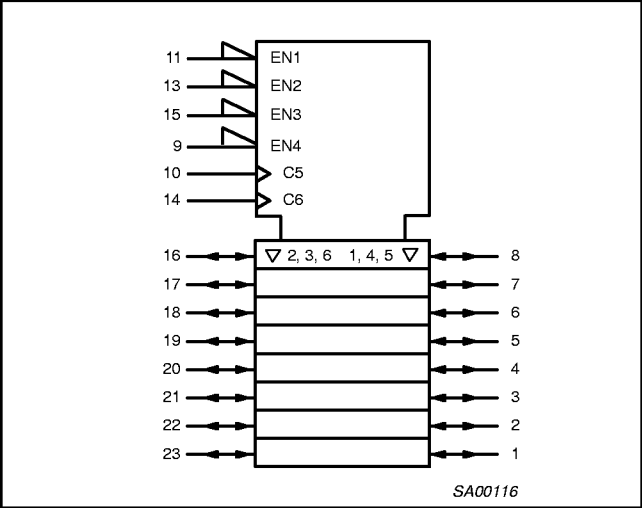
H = High voltage level
L = Low voltage level
 $\uparrow$ = Low-to-High transition
X = Don't care
XX= AB or BA
NC= No change

FUNCTION TABLE for Output Enable

INPUTS		INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{\text{OE}}\text{XX}$				
H	X		Z	Disable outputs
L L	L H		L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX= AB or BA
Z = High impedance "off" state

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

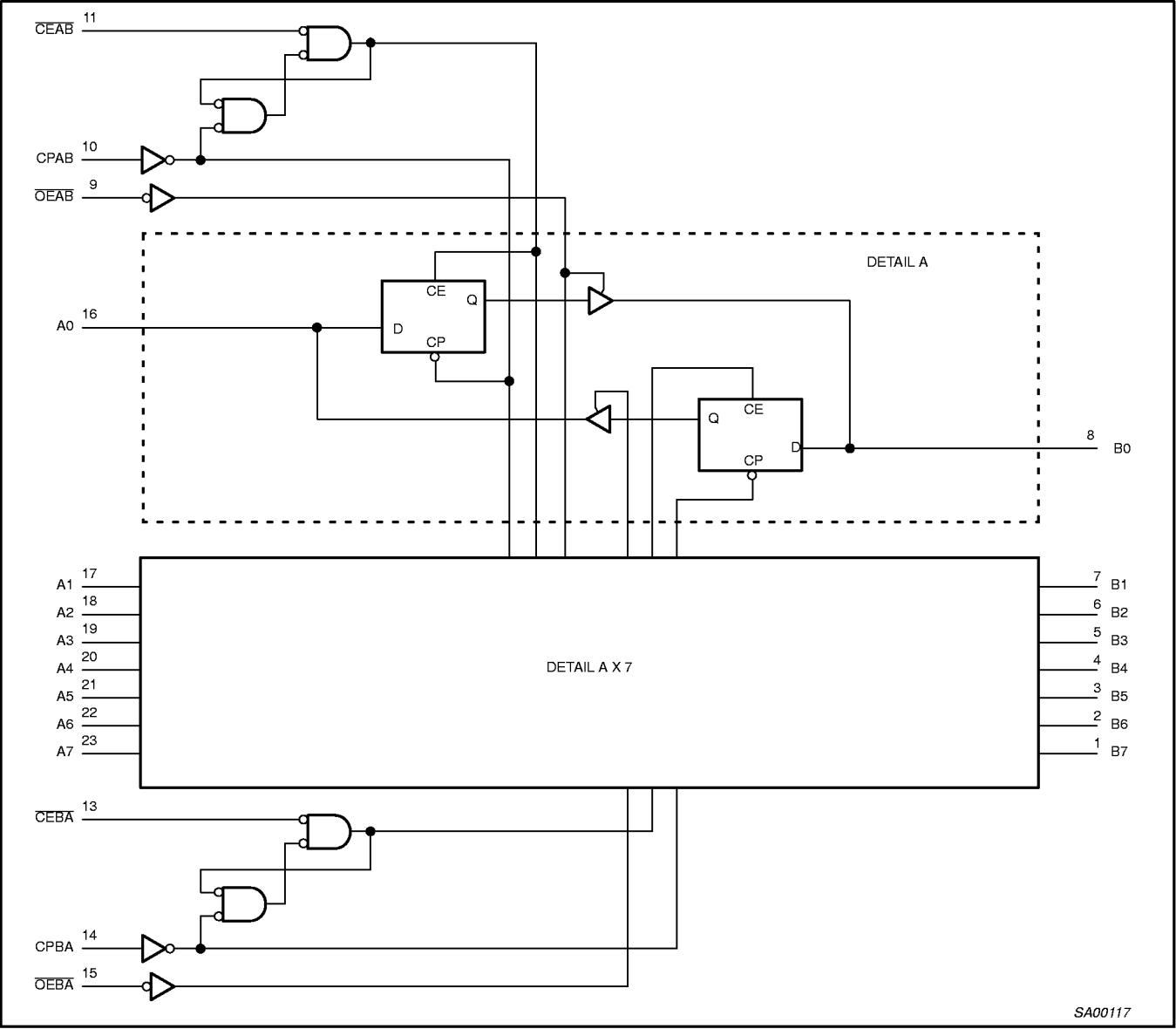
NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage		V _{CC} = 4.5V; I _{IK} = −18mA		−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage		V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	2.5	3.5		2.5		V
			V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	3.0	4.0		3.0		V
			V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}	2.0	2.6		2.0		V
V _{OL}	Low-level output voltage		V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³		V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	Control pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
		Data pins	V _{CC} = 5.5V; V _I = GND or 5.5V		5	100		100	μA
I _{OFF}	Power-off leakage current		V _{CC} = 0.0V; V _O = 4.5V; V _I = 0.0V or 5.5V		±5.0	±100		±100	μA
I _{PU} /I _{PD}	Power-up/down 3-State output current ⁴		V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	μA
I _{OZH}	3-State output High current		V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{OZL}	3-State output Low current		V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		−5.0	−50		−50	μA
I _{CEX}	Output High leakage current		V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹		V _{CC} = 5.5V; V _O = 2.5V	−50	−80	−180	−50	−180	mA
I _{CCH}	Quiescent supply current		V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		110	250		250	μA
I _{CCL}			V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		20	30		30	mA
I _{CCZ}			V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		110	250		250	μA
ΔI _{CC}	Additional supply current per input pin ²		V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.3	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100μsec is permitted.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40°C to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	150	250		150		MHz
t _{PLH} t _{PHL}	Propagation delay CPBA to An, CPAB to Bn	1	2.0 2.5	3.2 3.8	6.6 7.2	2.0 2.5	7.6 8.2	ns
t _{PZH} t _{PZL}	Output enable time OEBA to An, OEAB to Bn	3 4	1.0 2.2	3.2 4.4	4.8 6.2	1.0 2.2	5.8 7.5	ns
t _{PHZ} t _{PLZ}	Output disable time OEBA to An, OEAB to Bn	3 4	2.0 1.5	3.6 2.8	7.6 7.1	2.0 1.5	8.1 7.6	ns

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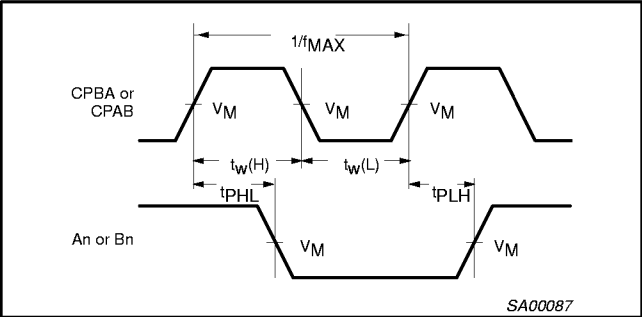
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AC SETUP REQUIREMENTS

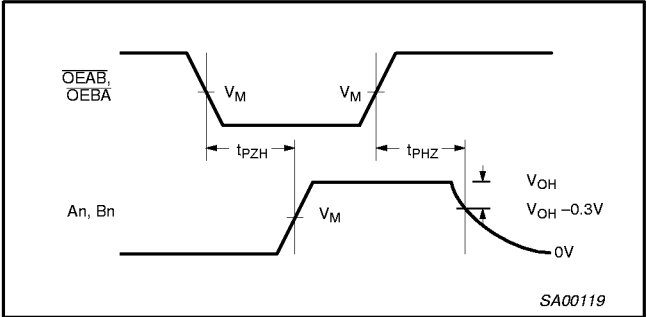
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = +25^{\circ}C$ $V_{CC} = +5.0V$		$T_{amb} = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = +5.0V \pm 0.5V$	
			Min	Typ	Min	
$t_{S(H)}$ $t_{S(L)}$	Setup time An to CPAB or Bn to CPBA	2	4.5 3.5	2.2 1.6	4.5 3.5	ns
$t_{H(H)}$ $t_{H(L)}$	Hold time An to CPAB or Bn to CPBA	2	0.0 0.0	-0.8 -1.4	0.0 0.0	ns
$t_{S(H)}$ $t_{S(L)}$	Setup time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	2	4.0 3.0	0.8 0.8	4.0 3.0	ns
$t_{H(H)}$ $t_{H(L)}$	Hold time $\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA	2	0.0 0.0	-0.7 -0.7	0.0 0.0	ns
$t_{W(H)}$ $t_{W(L)}$	CPAB or CPBA pulse width, High or Low	1	3.0 3.5	0.8 0.9	3.0 3.5	ns

AC WAVEFORMS

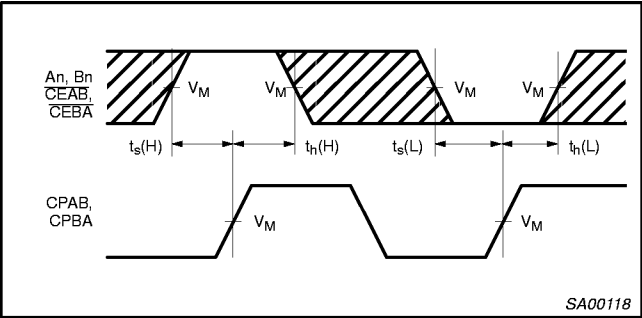
$V_M = 1.5V$, $V_{IN} = GND \text{ to } 3.0V$



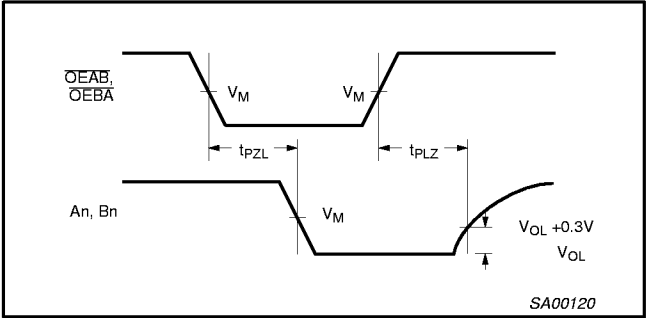
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Data Setup and Hold Times

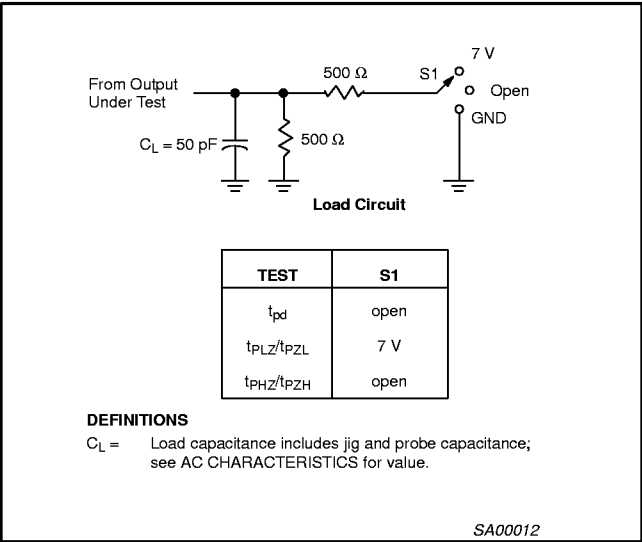


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

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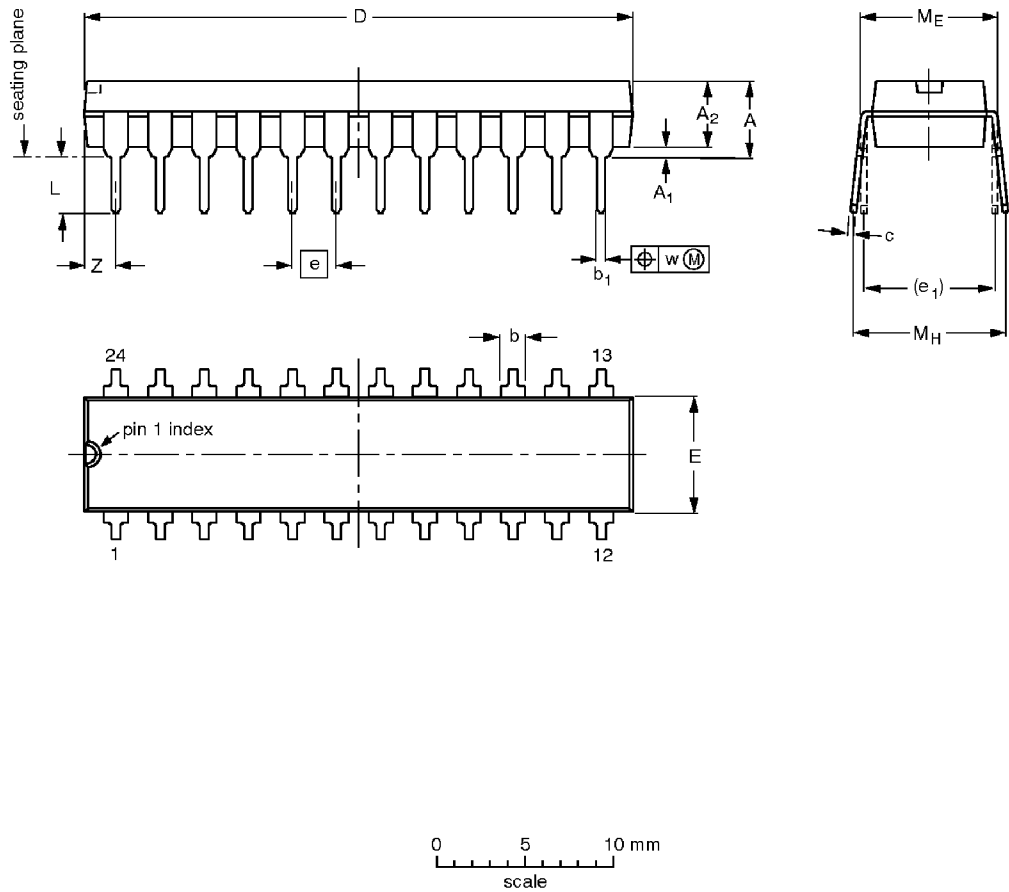


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74ABT2952

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

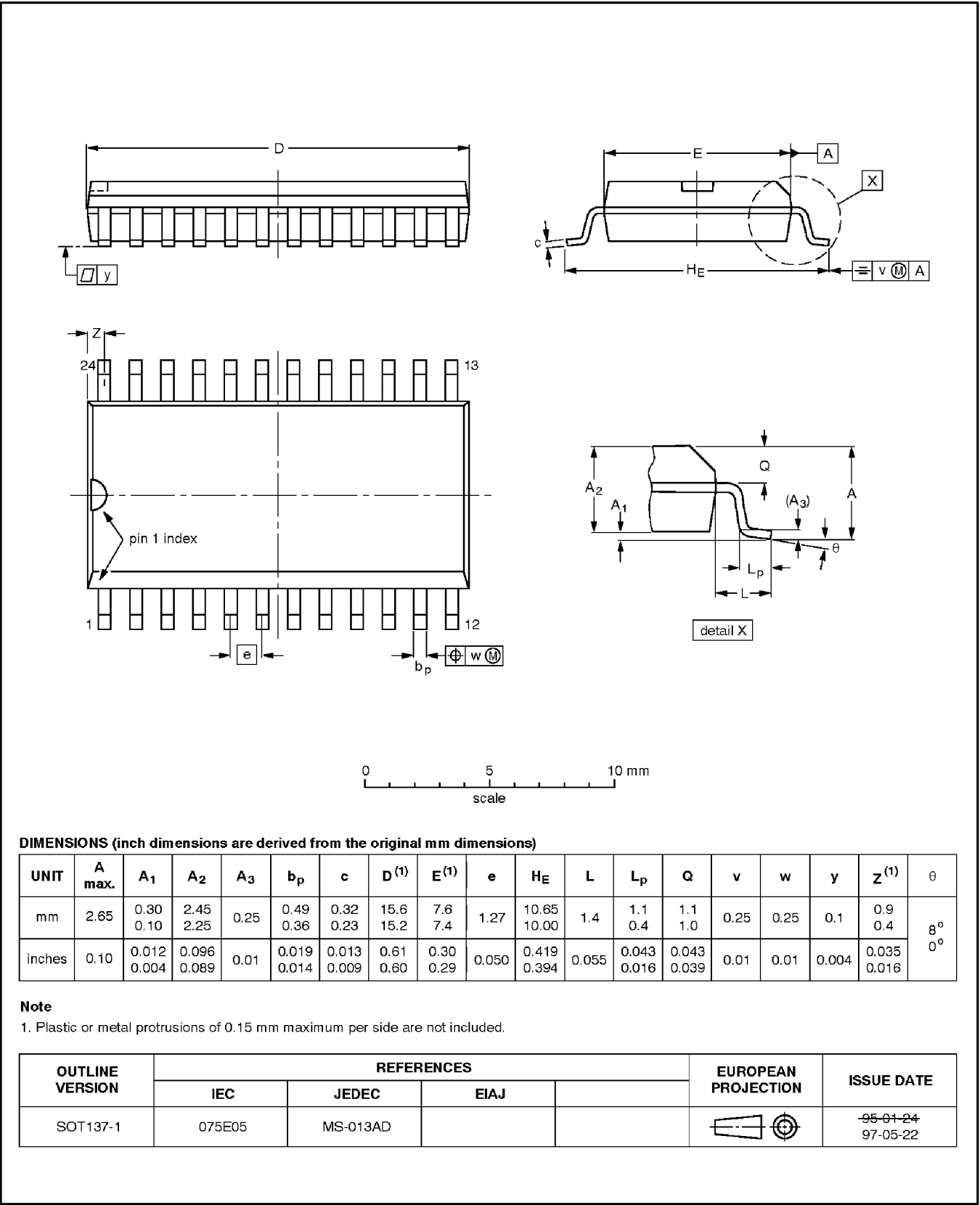
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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



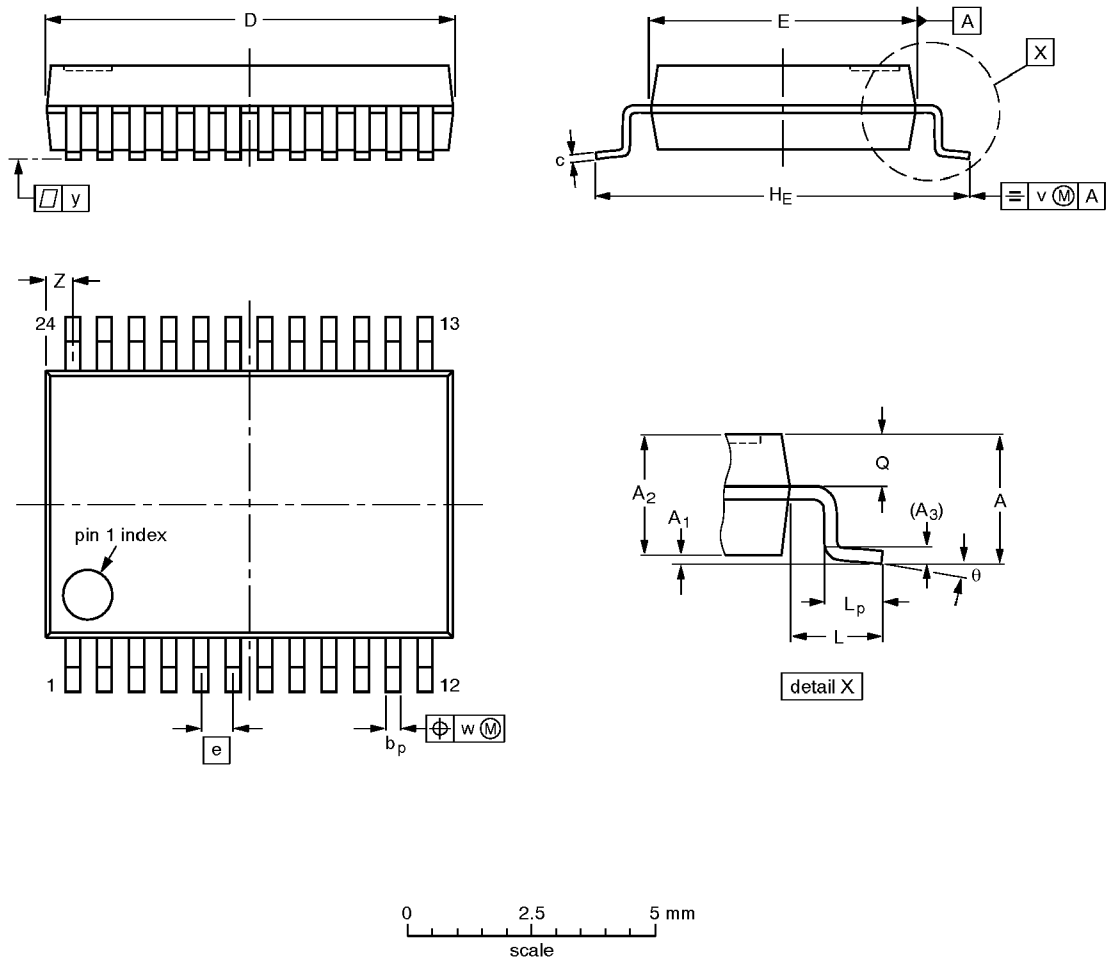
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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

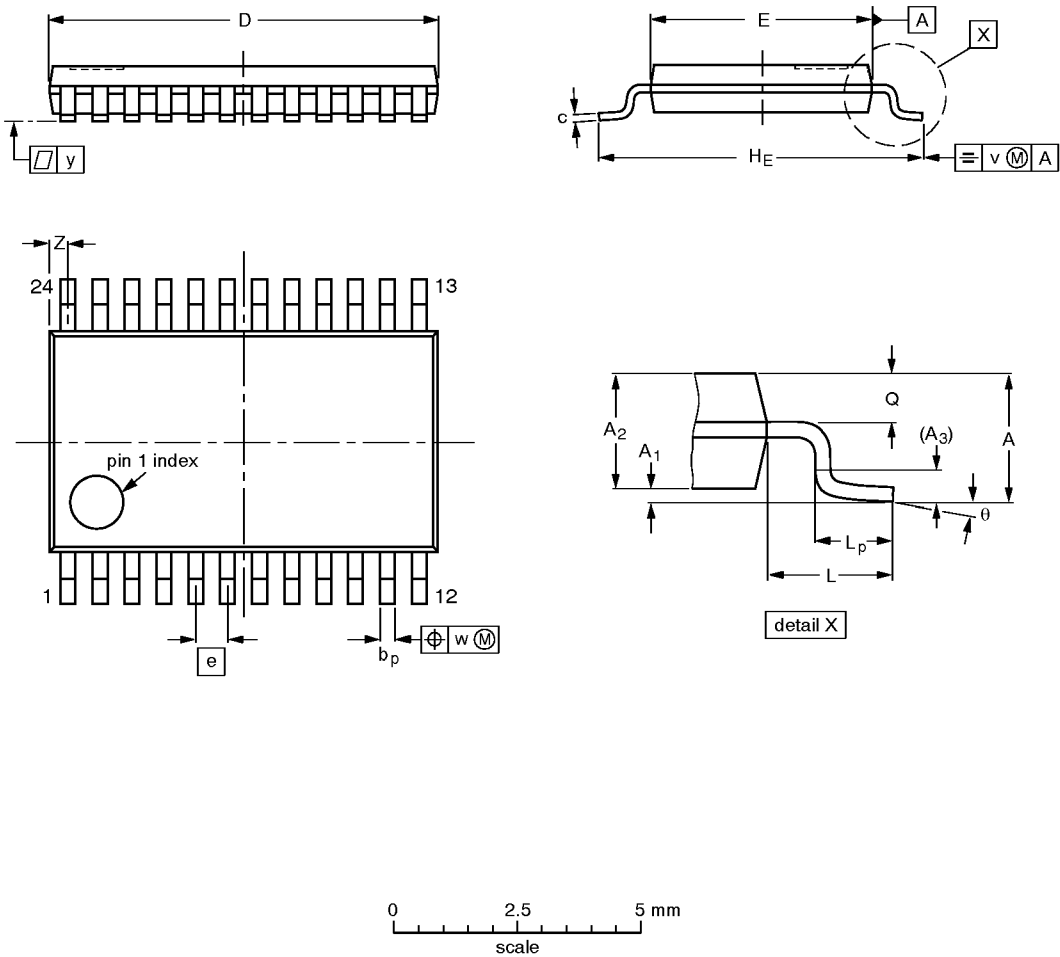
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08- 95-02-04

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74ABT2952

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04