

Power MOSFET

16 V, 51 A, Single N-Channel, DPAK/IPAK

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Three Package Variations for Design Flexibility
- These are Pb-Free Devices

Applications

- DC-DC Converters
- High Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DSS}	16	V		
Gate-to-Source Voltage	V_{GS}	± 16	V		
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	13.8		
		$T_A = 85^\circ\text{C}$	10.7		
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	2.6	W		
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	9.6		
		$T_A = 85^\circ\text{C}$	7.4		
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	1.2	W		
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	$T_C = 25^\circ\text{C}$	51		
		$T_C = 85^\circ\text{C}$	39		
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	34.9	W		
Pulsed Drain Current	$t_p = 10\mu\text{s}$	$T_A = 25^\circ\text{C}$	I_{DM}	114	A
Current Limited by Package	$T_A = 25^\circ\text{C}$	$I_{DmaxPkg}$	35	A	
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$		
Source Current (Body Diode)	I_S	29	A		
Drain to Source dV/dt	dV/dt	6	V/ns		
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_L = 10\text{ A}_{pk}$, $L = 0.3\text{ mH}$, $R_G = 25\ \Omega$)	EAS	15	mJ		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$		

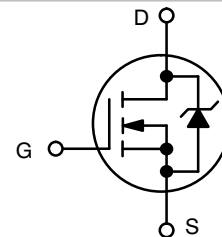
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



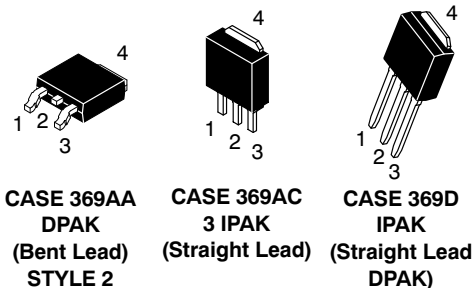
ON Semiconductor®

<http://onsemi.com>

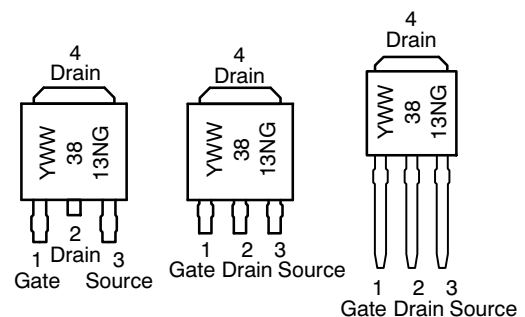
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
16 V	8.75 m Ω @ 10 V	51 A
	14.5 m Ω @ 4.5 V	



N-CHANNEL MOSFET



MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
 WW = Work Week
 3813N = Device Code
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NTD3813N

THEMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.3	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	3.6	
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	58	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	121	

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	16			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			16.8		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5		2.5	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.3		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$		7.2	8.75	m Ω
		$V_{GS} = 4.5\text{ V}$	$I_D = 15\text{ A}$		11	14.5	
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		40		S	

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 12\text{ V}$		963		pF
Output Capacitance	C_{OSS}			338		
Reverse Transfer Capacitance	C_{RSS}			191		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 12\text{ V}, I_D = 15\text{ A}$		8.5	12.8	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.93		
Gate-to-Source Charge	Q_{GS}			3.1		
Gate-to-Drain Charge	Q_{GD}			3.8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 12\text{ V}, I_D = 15\text{ A}$		16.7		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 12\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		12		ns
Rise Time	t_r			38		
Turn-Off Delay Time	$t_{d(OFF)}$			14		
Fall Time	t_f			5.0		
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 12\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		8.0		ns
Rise Time	t_r			33		
Turn-Off Delay Time	$t_{d(OFF)}$			20		
Fall Time	t_f			8.0		

3. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.
5. Assume standoff of 110 mm.

NTD3813N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 15 A	T _J = 25°C	0.88	1.2	V
			T _J = 125°C	0.76		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 15 A		14.4		ns
Charge Time	t _a			6.8		
Discharge Time	t _b			7.6		
Reverse Recovery Charge	Q _{RR}			3.7		

PACKAGE PARASITIC VALUES

Source Inductance	L _S	T _A = 25°C		2.49		nH
Drain Inductance, DPAK	L _D			0.0164		
Drain Inductance, IPAK (Note 5)	L _D			1.88		
Gate Inductance	L _G			3.46		
Gate Resistance	R _G			0.4		

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.
- Assume standoff of 110 mm.

TYPICAL PERFORMANCE CURVES

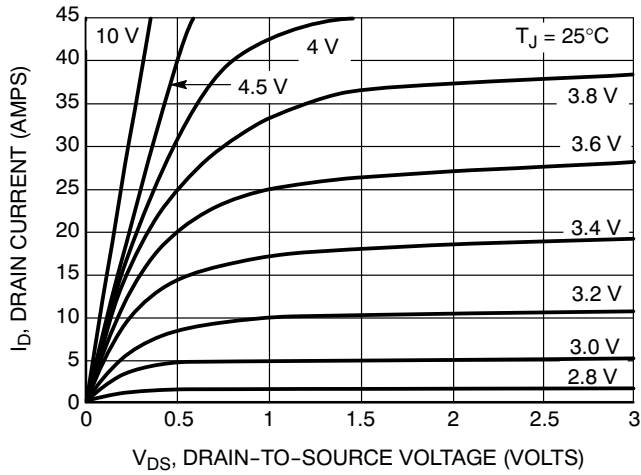


Figure 1. On-Region Characteristics

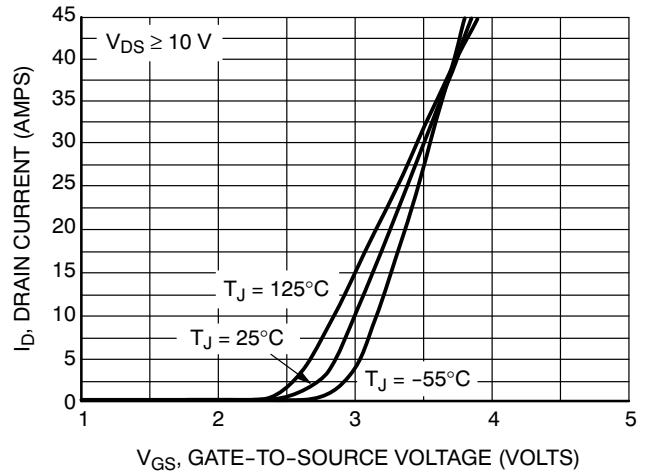


Figure 2. Transfer Characteristics

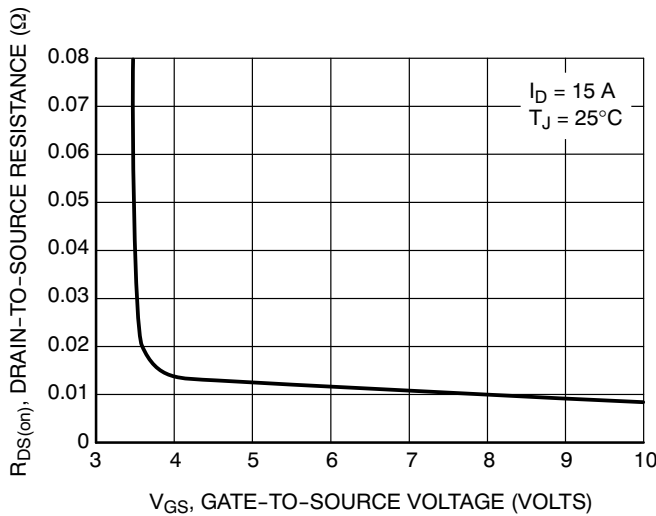


Figure 3. On-Resistance vs. Gate-to-Source Voltage

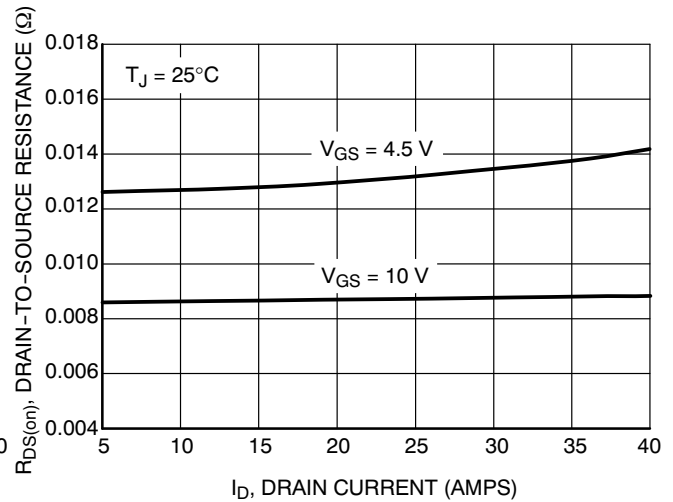


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

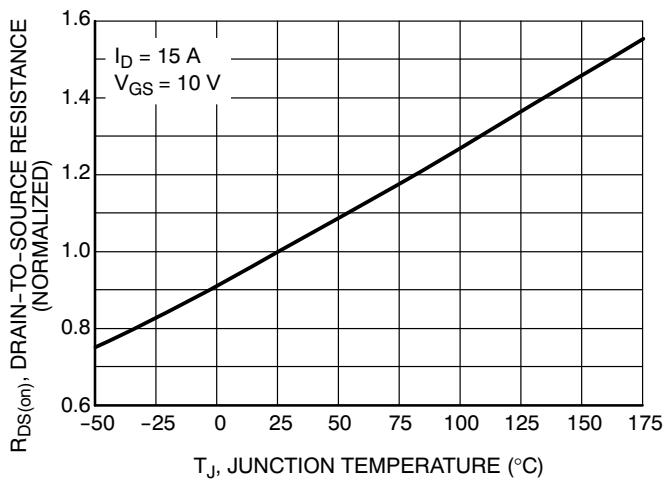


Figure 5. On-Resistance Variation with Temperature

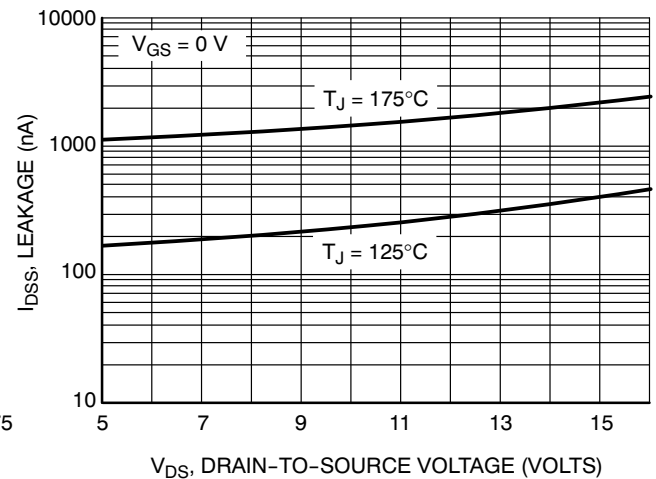


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

TYPICAL PERFORMANCE CURVES

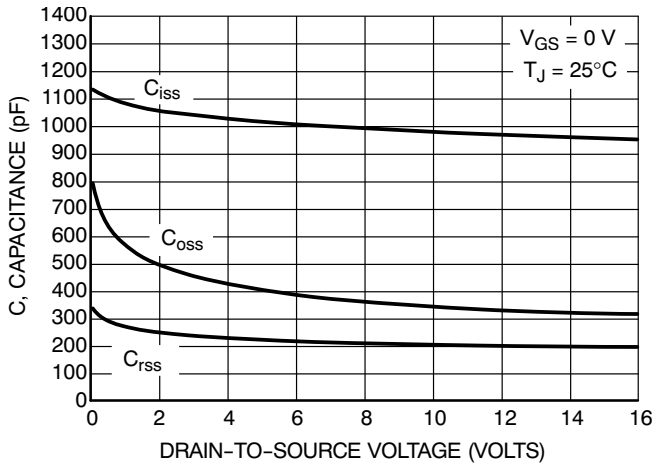


Figure 7. Capacitance Variation

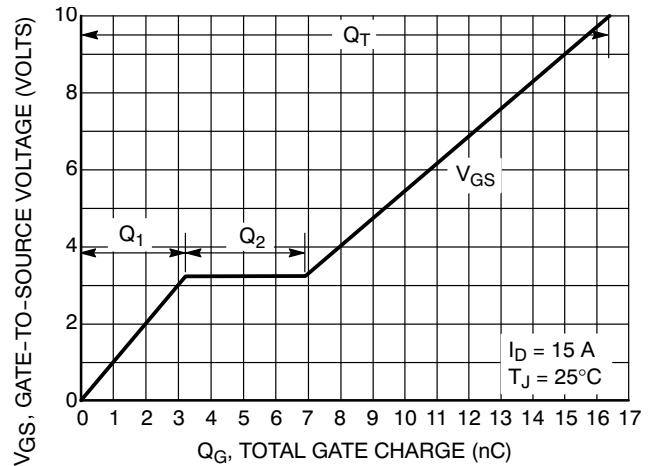


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

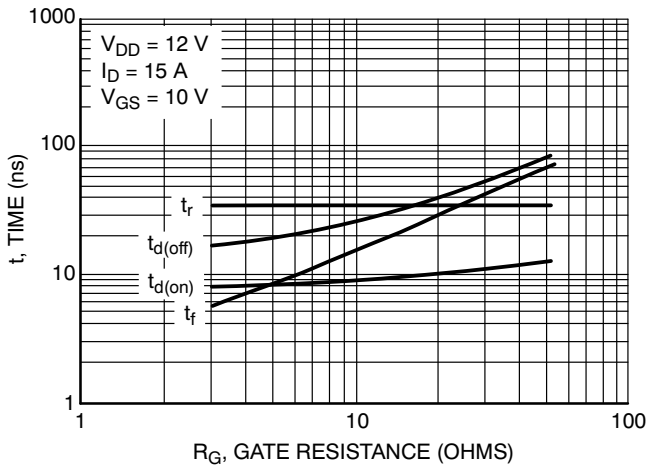


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

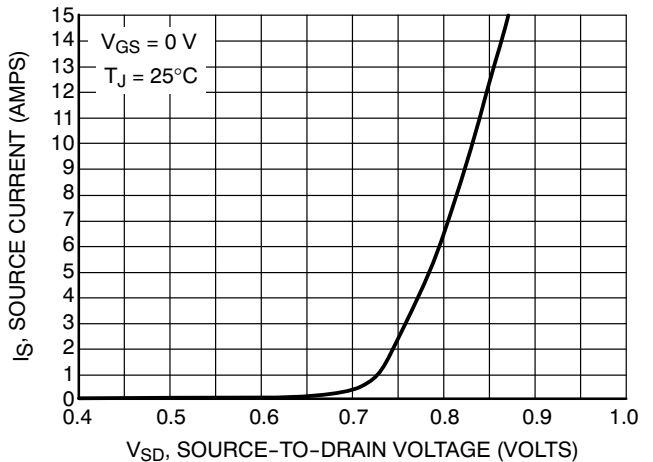


Figure 10. Diode Forward Voltage vs. Current

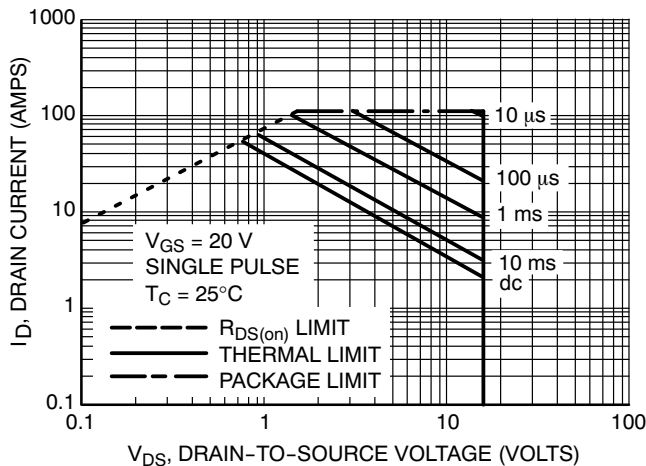


Figure 11. Maximum Rated Forward Biased Safe Operating Area

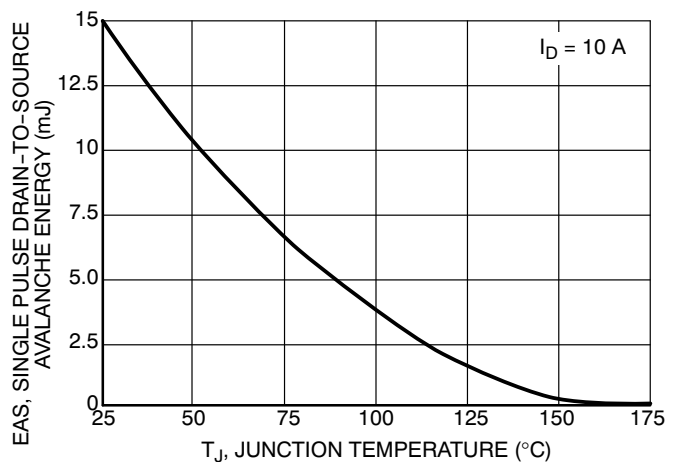


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTD3813N

ORDERING INFORMATION [查询 NTD3813N-D 供应商](#)

Device	Package	Shipping†
NTD3813NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD3813N-1G	IPAK (Pb-Free)	75 Units / Rail
NTD3813N-35G	IPAK Trimmed Lead (3.5 ± 0.15 mm) (Pb-Free)	75 Units / Rail

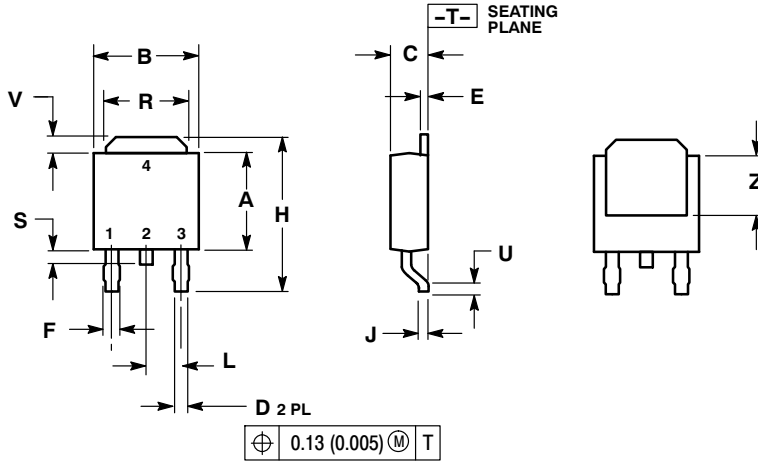
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD3813N

[查询"NTD3813N-D"供应商](#)

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369AA-01
ISSUE A

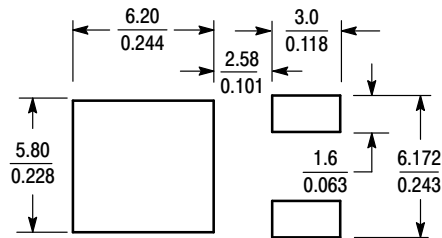


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

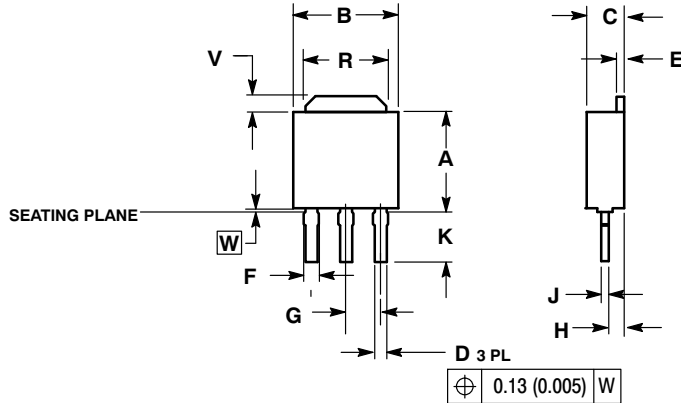
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD3813N

查询"NTD3813N-D"供应商

PACKAGE DIMENSIONS

3 IPAK, STRAIGHT LEAD CASE 369AC-01 ISSUE O

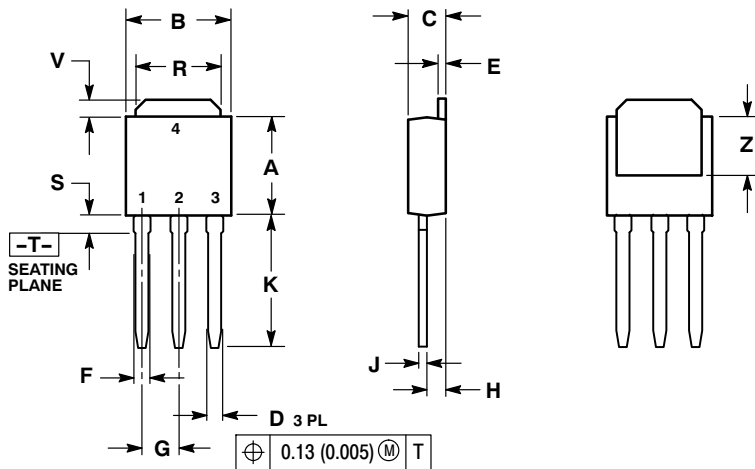


NOTES:

- 1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2.. CONTROLLING DIMENSION: INCH.
3. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
4. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.134	0.142	3.40	3.60
R	0.180	0.215	4.57	5.46
V	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

IPAK (STRAIGHT LEAD DPAK) CASE 369D-01 ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative