

HD74HC595

8-bit Shift Register/Latch (with 3-state outputs)

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Description



This device each contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

Features

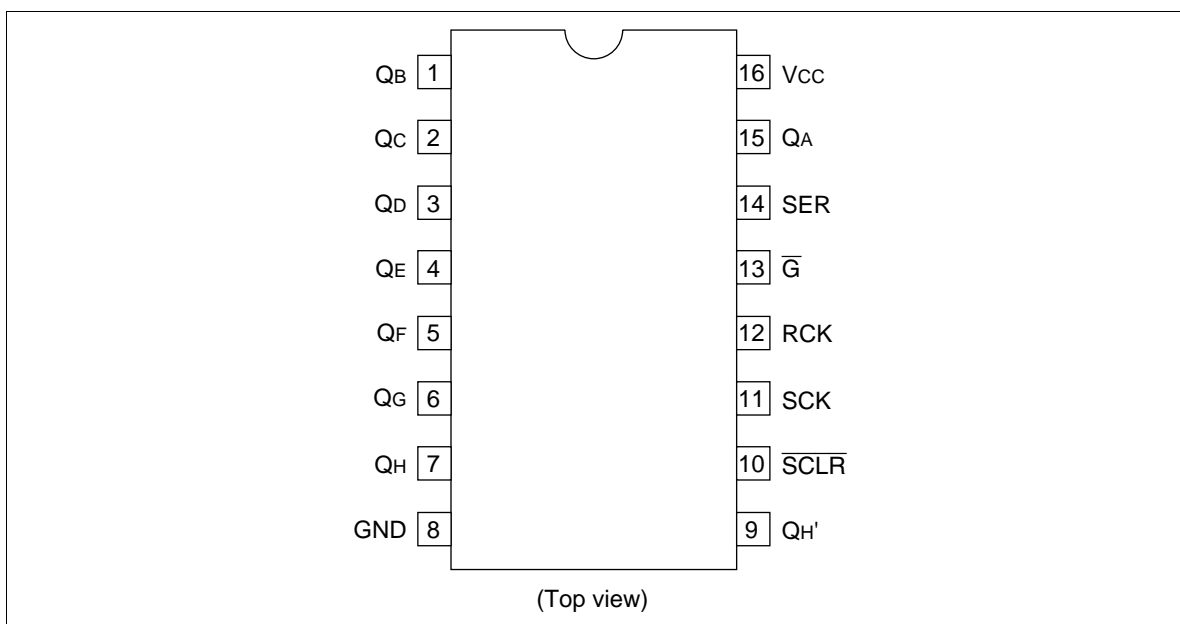
- High Speed Operation: t_{pd} (RCK to Q) = 17 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads (Q_A to Q_H outputs)
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

RCK	SCK	$\overline{\text{SCLR}}$	$\overline{\text{G}}$	Function
X	X	X	H	Q_A to Q_H high impedance
X	X	L	X	Shift register cleared $Q_n' = L$
X		H	X	Shift register clocked $Q_n = Q_{n-1}$, $Q_A = \text{SER}$
	X	H	X	Contents of shift register transferred to output latches

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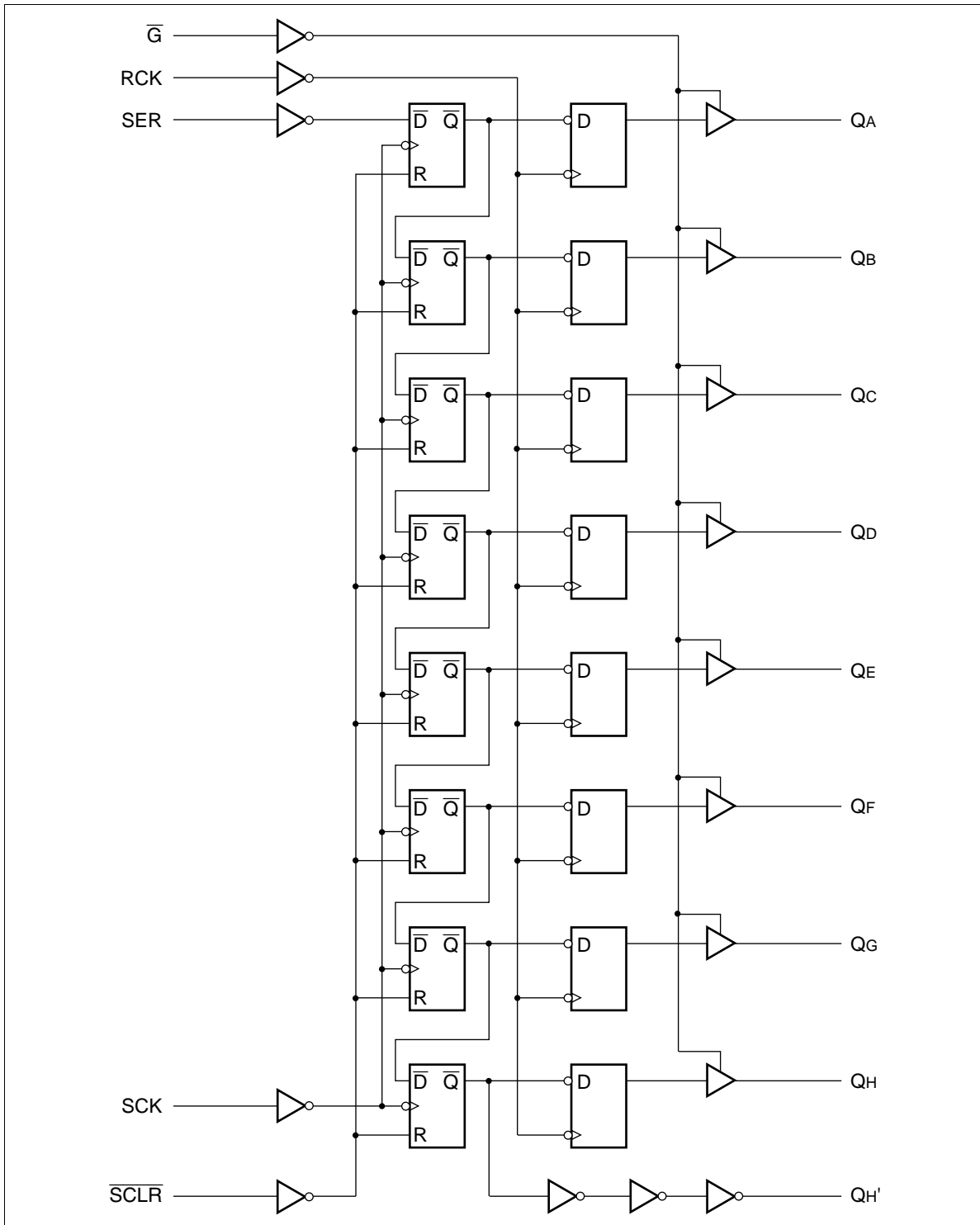
Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Output current	I_{OUT}	± 35	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	± 75	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power dissipation per package	P_T	500	mW
Storage Temperature	Tstg	-65 to +150	°C

Logic Diagram



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DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V			
		4.5	3.15	—	—	3.15	—				
		6.0	4.2	—	—	4.2	—				
	V _{IL}	2.0	—	—	0.5	—	0.5	V			
		4.5	—	—	1.35	—	1.35				
		6.0	—	—	1.8	—	1.8				
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Q _A to Q _H Vin = V _{IH} or V _{IL}	I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—				
		6.0	5.9	6.0	—	5.9	—				
		4.5	4.18	—	—	4.13	—			I _{OH} = -6 mA	
		6.0	5.68	—	—	5.63	—			I _{OH} = -7.8 mA	
		V _{OL}	2.0	—	0.0	0.1	—			0.1	V
	4.5		—	0.0	0.1	—	0.1				
	6.0		—	0.0	0.1	—	0.1				
	4.5		—	—	0.26	—	0.33	I _{OL} = 6 mA			
	6.0		—	—	0.26	—	0.33	I _{OL} = 7.8 mA			
	Output voltage		V _{OH}	2.0	1.9	2.0	—	1.9	—	V	
		4.5		4.4	4.5	—	4.4	—			
6.0		5.9		6.0	—	5.9	—				
4.5		4.18		—	—	4.13	—	I _{OH} = -4 mA			
6.0		5.68		—	—	5.63	—	I _{OH} = -5.2 mA			
V _{OL}		2.0		—	0.0	0.1	—	0.1	V		Q' _H Vin = V _{IH} or V _{IL}
		4.5	—	0.0	0.1	—	0.1				
		6.0	—	0.0	0.1	—	0.1				
		4.5	—	—	0.26	—	0.33	I _{OL} = 4 mA			
		6.0	—	—	0.26	—	0.33	I _{OL} = 5.2 mA			
		Off-state output current	I _{OZ}	6.0	—	—	±0.5	—		±5.0	
Input current		I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA		

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

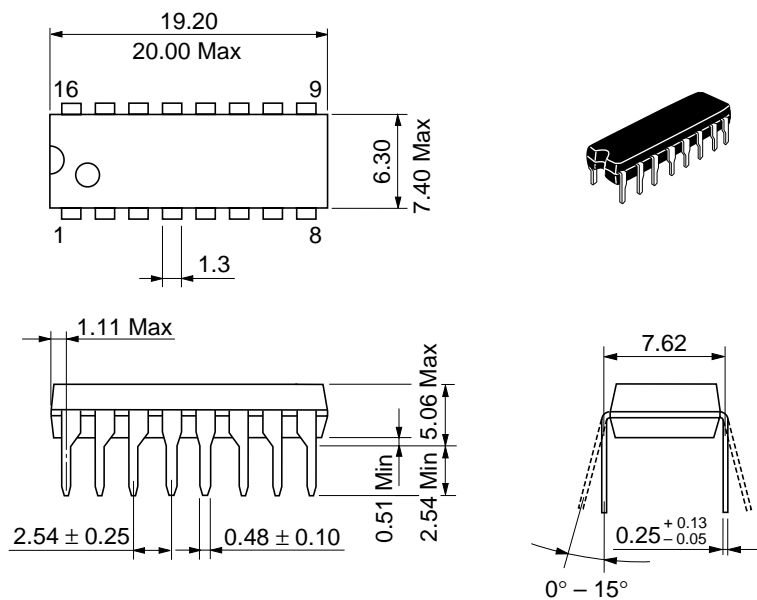
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	31	—	24		
Propagation delay time	t_{PLH}	2.0	—	—	115	—	145	ns	SCK to Q_H'
		4.5	—	12	23	—	29		
		6.0	—	—	20	—	25		
	t_{PHL}	2.0	—	—	150	—	190	ns	RCK to Q
		4.5	—	17	30	—	38		
		6.0	—	—	26	—	33		
t_{PLH}	2.0	—	—	175	—	220	ns	$\overline{\text{SCLR}}$ to Q_H'	
	4.5	—	20	35	—	44			
	6.0	—	—	30	—	37			
Output enable time	t_{ZL}	2.0	—	—	150	—	190	ns	
	t_{ZH}	4.5	—	13	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{LZ}	2.0	—	—	150	—	190	ns	
	t_{HZ}	4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	SER to SCK
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	200	—	—	250	—	ns	SCK to RCK
		4.5	40	8	—	50	—		
		6.0	34	—	—	43	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		

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AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns) (cont)

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	1	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	Q_H'
	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
		2.0	—	—	60	—	75	ns	Q
	4.5	—	4	12	—	15			
	6.0	—	—	10	—	13			
Input capacitance	C_{in}	—	—	5	10	—	5	pF	

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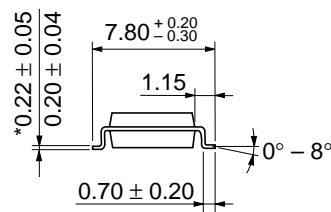
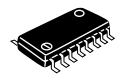
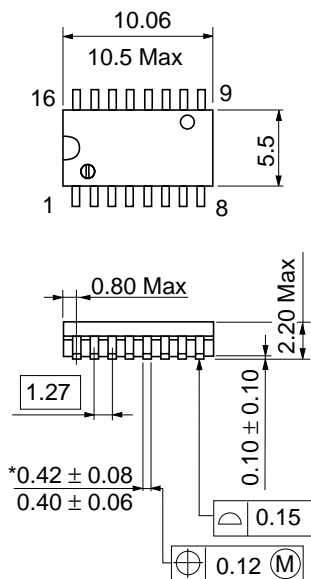


Unit: mm

Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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Unit: mm

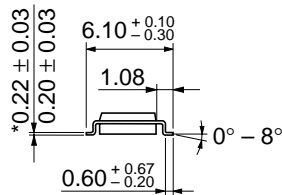
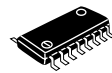
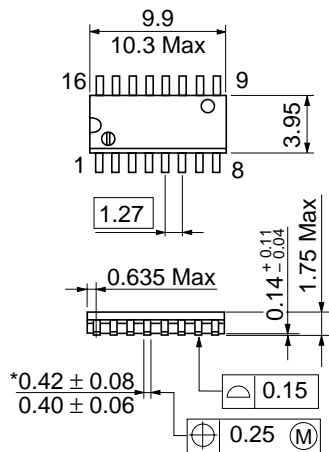


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

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Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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