



September 1983  
Revised May 2005

# MM74HC688

## 8-Bit Magnitude Comparator (Equality Detector)

### General Description

The MM74HC688 equality detector utilizes advanced silicon-gate CMOS technology to compare bit for bit two 8-bit words and indicates whether or not they are equal. The  $\overline{P=Q}$  output indicates equality when it is LOW. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 74LS688. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

### Features

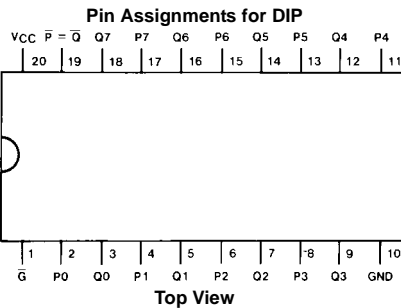
- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80  $\mu$ A (74 Series)
- Large output current: 4 mA (74 Series)
- Same as HC521

### Ordering Code:

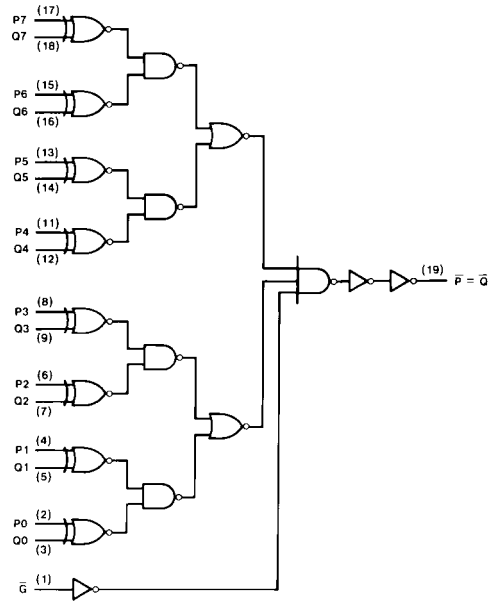
Order Number	Package Number	Package Description
MM74HC688WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC688SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC688MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC688N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Logic Diagram



### Truth Table

Inputs		$\overline{P=Q}$
Data P,Q	Enable $\overline{G}$	
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

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Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions			
(Note 2)			<b>Min</b>	<b>Max</b>	<b>Units</b>
Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V	Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$	DC Input or Output Voltage	0	$V_{CC}$	V
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$	( $V_{IN}, V_{OUT}$ )			
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA	Operating Temperature Range ( $T_A$ )	-40	+85	$^{\circ}C$
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA	Input Rise or Fall Times			
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA	( $t_r, t_f$ ) $V_{CC} = 2.0V$		1000	ns
Storage Temperature Range ( $T_{STG}$ )	-65 $^{\circ}C$ to +150 $^{\circ}C$	$V_{CC} = 4.5V$		500	ns
Power Dissipation ( $P_D$ )		$V_{CC} = 6.0V$		400	ns
(Note 3)	600 mW				
S.O. Package only	500 mW	<b>Note 1:</b> Absolute Maximum Ratings are those values beyond which damage to the device may occur.			
Lead Temperature ( $T_L$ )	260 $^{\circ}C$	<b>Note 2:</b> Unless otherwise specified all voltages are referenced to ground.			
(Soldering 10 seconds)		<b>Note 3:</b> Power Dissipation temperature derating — plastic "N" package: -12 mW/ $^{\circ}C$ from 65 $^{\circ}C$ to 85 $^{\circ}C$ .			

**DC Electrical Characteristics (Note 4)**

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^{\circ}C$			$T_A = -40$ to $85^{\circ}C$		$T_A = -55$ to $125^{\circ}C$		Units
				Typ	Guaranteed Limits						
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5			V	
			4.5V		3.15	3.15	3.15		V		
			6.0V		4.2	4.2	4.2		V		
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5			V	
			4.5V		1.35	1.35	1.35		V		
			6.0V		1.8	1.8	1.8		V		
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9		V		
			4.5V	4.5	4.4	4.4	4.4		V		
			6.0V	6.0	5.9	5.9	5.9		V		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7		V		
			6.0V	5.7	5.48	5.34	5.2		V		
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1		V		
			4.5V	0	0.1	0.1	0.1		V		
			6.0V	0	0.1	0.1	0.1		V		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4		V		
			6.0V	0.2	0.26	0.33	0.4		V		
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu A$		
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160		$\mu A$		

**Note 4:** For a power supply of 5V  $\pm 10\%$  the worst case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics					
$V_{CC} = 5V, T_A = 25^{\circ}C, C_L = 15\text{ pF}, t_r = t_f = 6\text{ ns}$					
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, any P or Q to Output		21	30	ns
$t_{PLH}, t_{PHL}$	Maximum Propagation Delay, Enable to any Output		14	20	ns

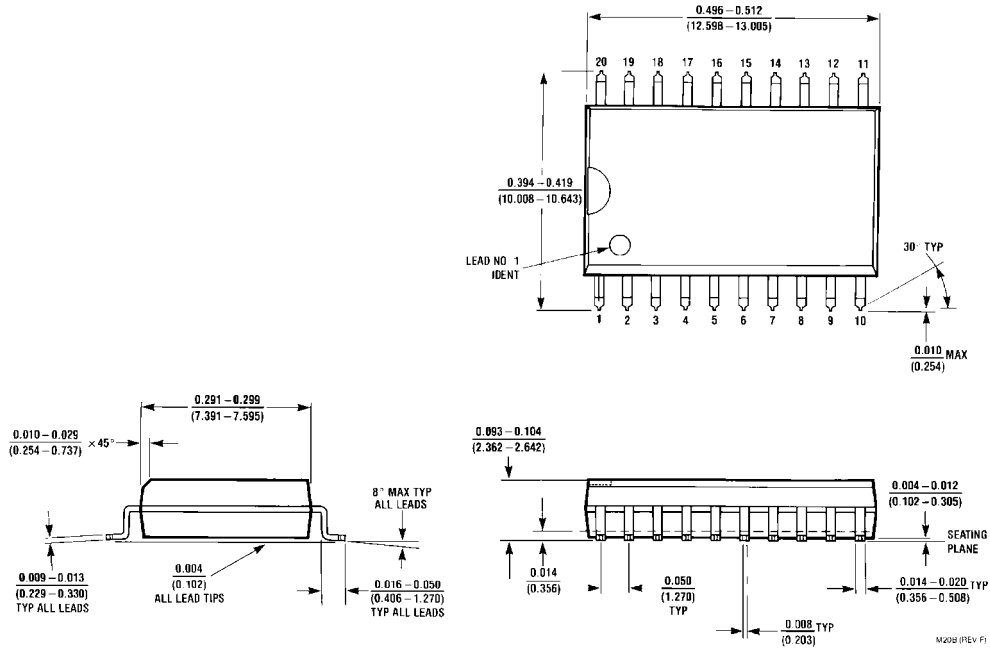
  

AC Electrical Characteristics								
$V_{CC} = 2.0V\text{ to }6.0V, C_L = 50\text{ pF}, t_r = t_f = 6\text{ ns (unless otherwise specified)}$								
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^{\circ}C$	$T_A = -40\text{ to }85^{\circ}C$	$T_A = -55\text{ to }125^{\circ}C$	Units	
				Typ	Guaranteed Limits			
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, P or Q to Output		2.0V	60	175	220	263	ns
			4.5V	22	35	44	53	ns
			6.0V	19	30	38	45	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Enable to Output		2.0V	45	120	150	180	ns
			4.5V	15	24	30	36	ns
			6.0V	13	20	25	30	ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)			45				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

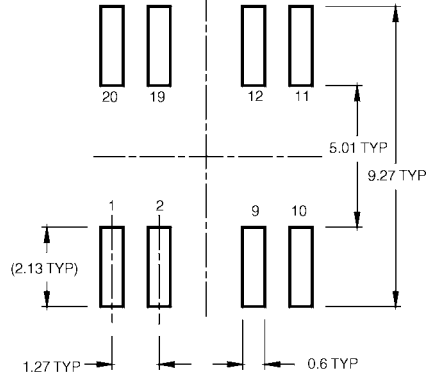
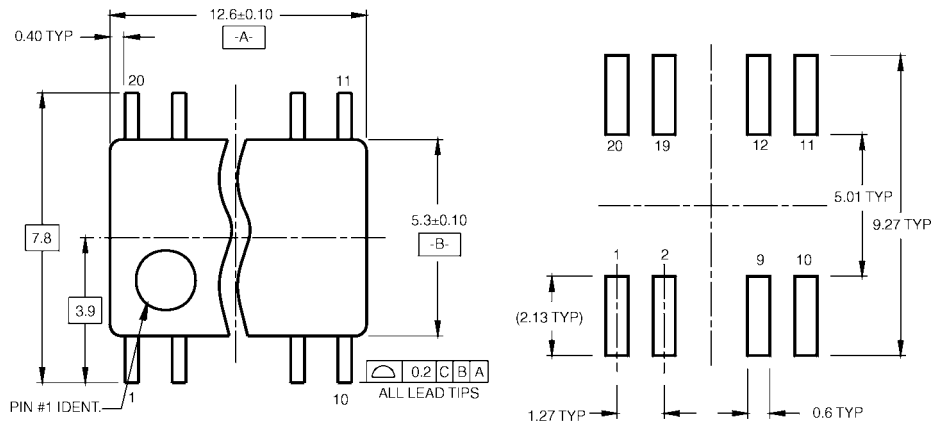
MM74HC688

**Physical Dimensions** inches (millimeters) unless otherwise noted

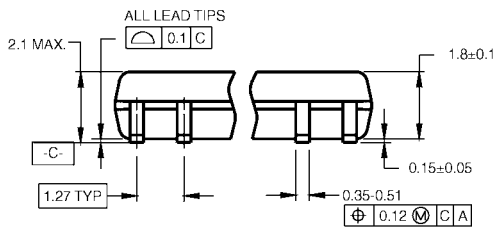


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**

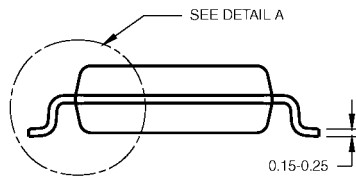
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

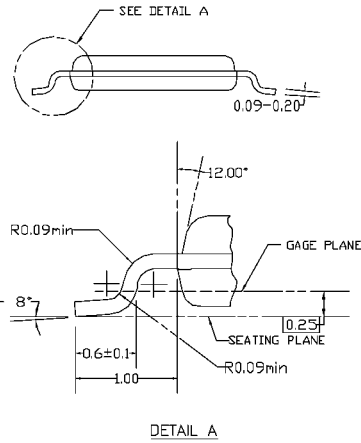
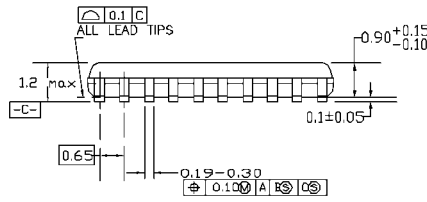
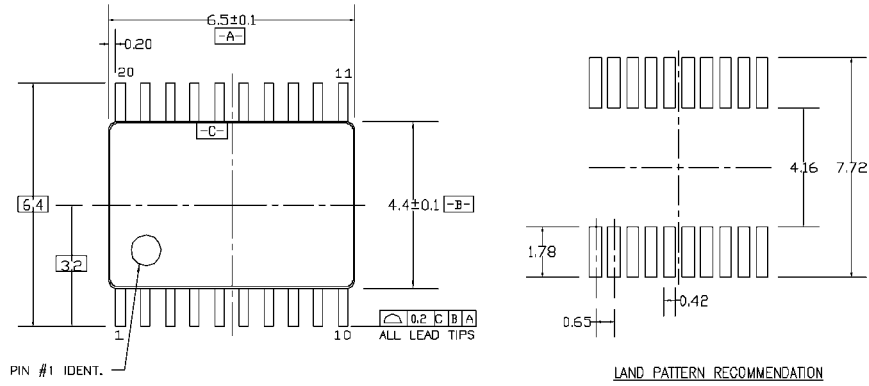
- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

MM74HC688

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20**

