

## 2, 4-CHANNEL ESD SOLUTION FOR SUPER-SPEED (6 GBPS) USB 3.0 INTERFACE

Check for Samples: [TPD2EUSB30](#), [TPD4EUSB30](#)

### FEATURES

- Single and Dual-Pair Differential Lines to Protect the Differential Data and Clock Lines of the USB3.0, eSATA, or LVD Interface
- Flow-Through Pin Mapping for the High-Speed Lines Ensures Zero Additional Skew Due to Board Layout While Placing ESD-Protection Chip Near the Connector
- Supports Data Rates in Excess of 6 Gbps
- ESD Protection Meets or Exceeds IEC61000-4-2 (Level 4)
- Low Capacitance 0.05pF (IO to IO)
- 5-A Peak Pulse Current (per 8/20  $\mu$ s Pulse)
- Industrial Temperature Range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Space-Saving DRT, DQA Packages

### APPLICATIONS

- Notebooks
- Set-Top Boxes
- DVD Players
- Media Players
- Portable Computers

### DESCRIPTION/ORDERING INFORMATION

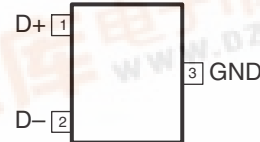
The TPD2EUSB30 and TPD4EUSB30 provide 2 and 4 channel ESD clamp circuits with flow-through pin mapping for ease of board layout. These devices have been designed to protect sensitive components which are connected to ultra high-speed data and transmission lines. The TPDxEUSB30 offer protection from stress caused by ESD (electrostatic discharge). These devices also offer 5 A (8/20  $\mu$ s) peak pulse current ratings per IEC 61000-4-5 (lightning) specification.

The monolithic silicon technology allows matching between the differential signal pairs. The differential 0.05-pF capacitance ensures that the signal distortion due to added ESD clamp remains minimal at high-speed differential data transmission.

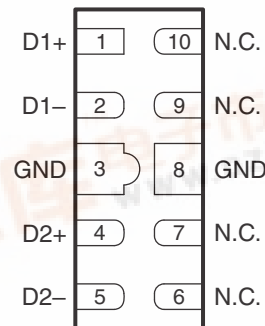
The TPD2EUSB30 and TPD4EUSB30 conform to IEC61000-4-2 (Level 4) ESD protection. The TPD2EUSB30 is offered in space saving DRT (1 mm  $\times$  1 mm) package. The TPD4EUSB30 is offered in space saving DQA (1 mm  $\times$  2.5 mm) package.

The TPD2EUSB30 and TPD4EUSB30 are characterized for operation over ambient air temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

TPD2EUSB30DRTR PACKAGE  
(TOP VIEW)



TPD4EUSB30DQAR PACKAGE  
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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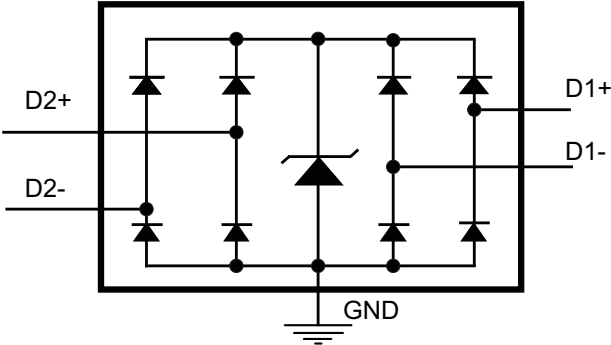
**ORDERING INFORMATION**

| T <sub>A</sub> | PACKAGE <sup>(1)</sup> (2) |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------------|---------------|-----------------------|------------------|
|                |                            |               |                       |                  |
| –40°C to 85°C  | SOT – DRT                  | Tape and reel | TPD2EUSB30DRTR        | 5PX              |
|                | SON – DQA                  | Tape and reel | TPD4EUSB30DQAR        | 66R              |

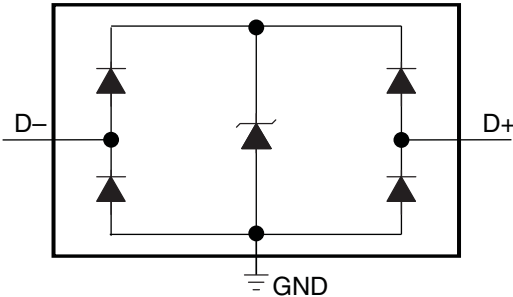
- (1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).  
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**CIRCUIT DIAGRAMS**

**TPD4EUSB30DQA Circuit**



**TPD2EUSB30DRT Circuit**



**TERMINAL FUNCTIONS**

| TERMINAL |             |             | TYPE     | DESCRIPTION   |
|----------|-------------|-------------|----------|---|
| NAME     | DRT PIN NO. | DQA PIN NO. |          |   |
| Dx+, Dx– | 1, 2        | 1, 2, 4, 5  | ESD port | High-speed ESD clamp, provides ESD protection to the high-speed differential data lines |
| GND      | 3           | 3, 8        | GND      | Ground  |
| N.C.     |             | 6, 7, 9, 10 |          | Not normally connected  |

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |   |             | MIN | MAX | UNIT |
|------------------|---|-------------|-----|-----|------|
|                  | IO voltage tolerance                          | D+, D– pins | 0   | 6   |      |
| T <sub>A</sub>   | Operating free-air temperature range          |             | –40 | 85  | °C   |
| T <sub>stg</sub> | Storage temperature range                     |             | –65 | 125 | °C   |
| ESD protection   | IEC 61000-4-2 Contact Discharge               | D+, D– pins |     | ±8  | kV   |
|                  | IEC 61000-4-2 Air-Gap Discharge (TPD2EUSB30)  | D+, D– pins |     | ±8  | kV   |
|                  | IEC 61000-4-2 Air-Gap Discharge (TPD4EUSB30)  | D+, D– pins |     | ±9  | kV   |
|                  | Peak pulse current (t <sub>p</sub> = 8/20 μs) | D+, D– pins |     | 5   | A    |
|                  | Peak pulse power (t <sub>p</sub> = 8/20 μs)   | D+, D– pins |     | 45  | W    |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS   | MIN | TYP  | MAX  | UNIT |
|---|---|-----|------|------|------|
| V <sub>RWM</sub> Reverse stand-off voltage          | D+,D– pins to ground  |     |      | 5.5  | V    |
| V <sub>clamp</sub> Clamp voltage                    | D+,D– pins to ground, I <sub>IO</sub> = 1 A                                   |     |      | 8    | V    |
| I <sub>IO</sub> Current from IO port to supply pins | V <sub>IO</sub> = 2.5 V, I <sub>D</sub> = 8 mA                                |     | 0.01 | 0.1  | μA   |
| V <sub>D</sub> Diode forward voltage                | D+,D– pins, lower clamp diode, V <sub>IO</sub> = 2.5 V, I <sub>D</sub> = 8 mA | 0.6 | 0.8  | 0.95 | V    |
| R <sub>dyn</sub> Dynamic resistance                 | D+,D– pins I = 1 A  |     | 1    |      | Ω    |
| C <sub>IO-IO</sub> Capacitance IO to IO             | D+,D– pins V <sub>IO</sub> = 2.5 V  |     | 0.05 |      | pF   |
| C <sub>IO-GND</sub> Capacitance IO to GND           | D+,D– pins (DRT)  |     | 0.7  |      | pF   |
|   | D1+, D1–, D2+, D2– (DQA )   |     | 0.8  |      |      |
| V <sub>BR</sub> Break-down voltage                  | I <sub>IO</sub> = 1 mA  | 7   |      |      | V    |

## TYPICAL OPERATING CHARACTERISTICS

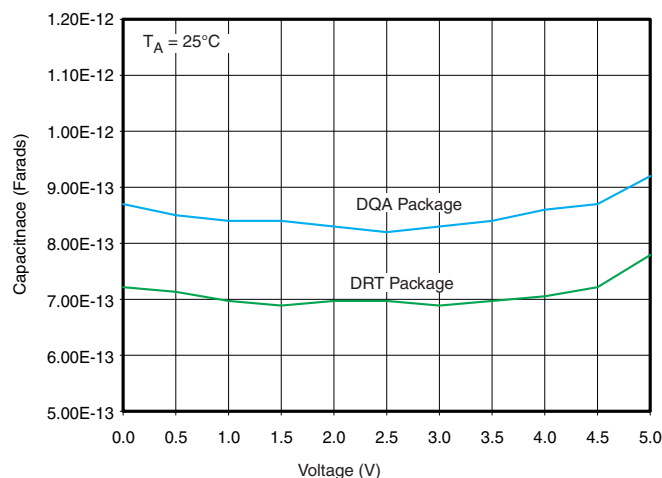


Figure 1. IO Capacitance vs IO Voltage

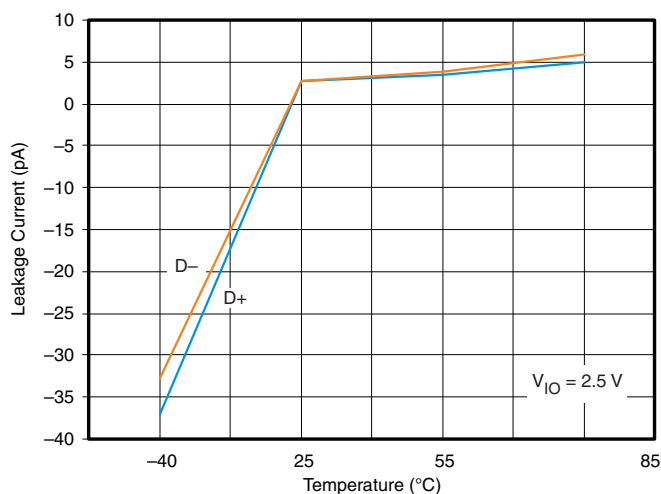


Figure 2. Leakage Current vs Temperature

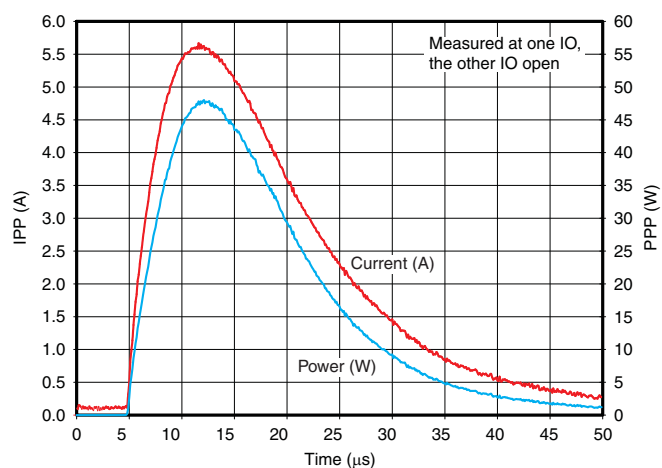


Figure 3. Peak Pulse Waveforms

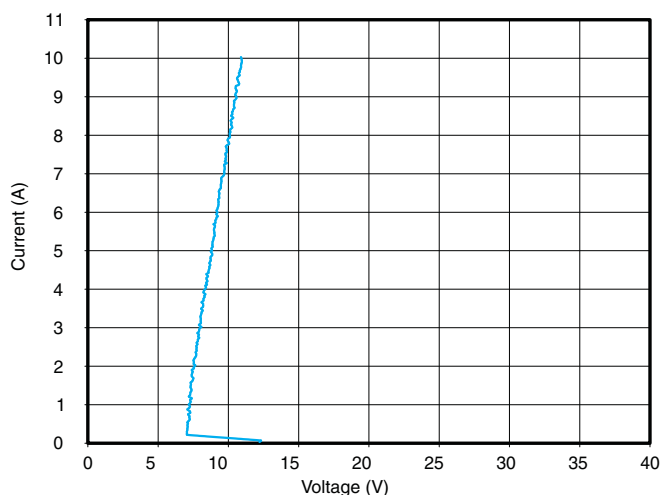


Figure 4. D+, D- Transmission Line Pulsar Plot (100 ns Pulse, 10 ns Rise Time)

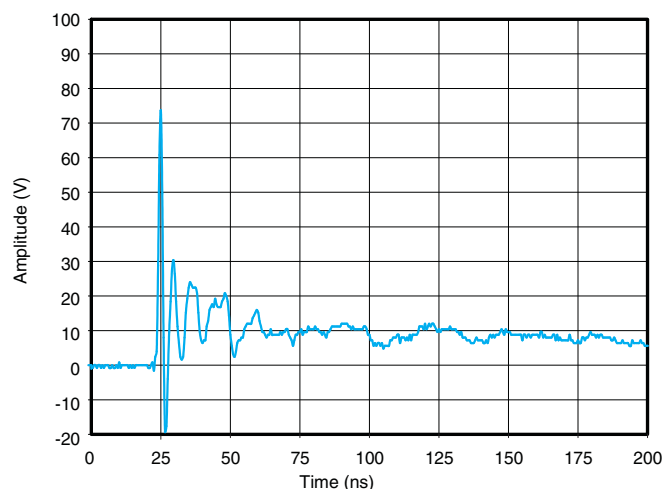


Figure 5. IEC Clamping Waveforms (8 kV Contact)

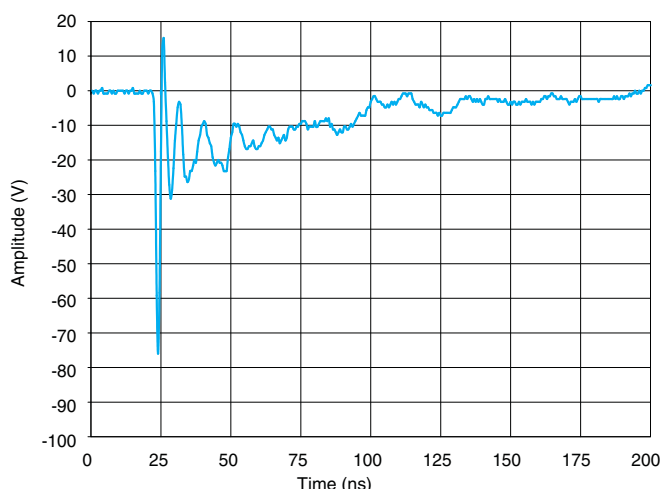


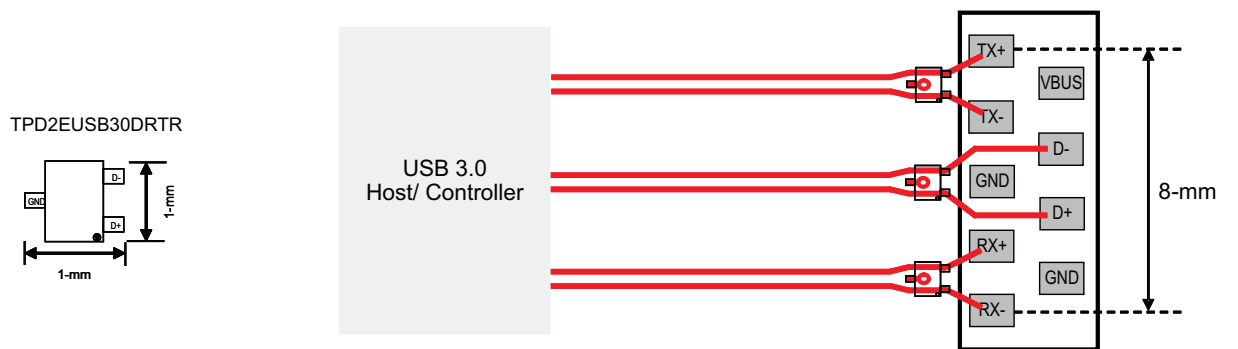
Figure 6. IEC Clamping Waveforms (-8 kV Contact)

## APPLICATION INFORMATION

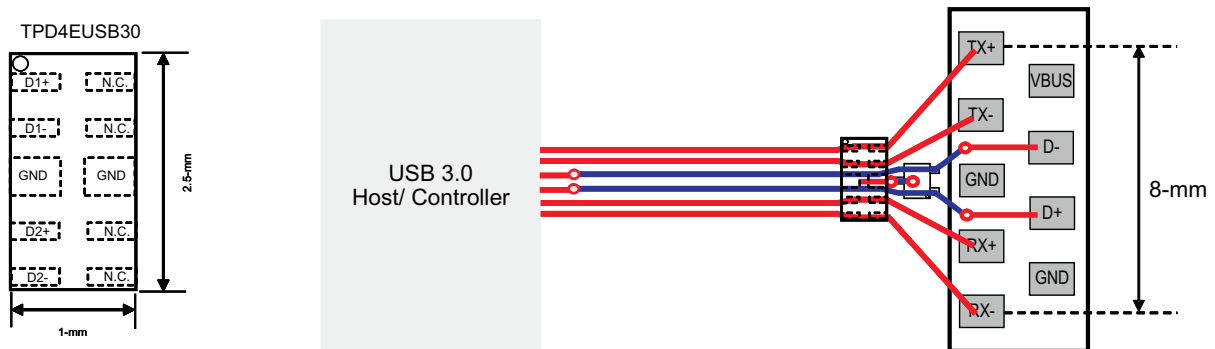
### Layout Guide with TPDxEUSB30DRTR

Refer to [Figure 7](#), the TPD2EUSB30DRTR is offered in space saving DRT package. The DRT package is a 1mm\* 1mm package with flow-through pin-mapping for the high-speed differential lines. The TPD4EUSB30DRTR is offered in space saving DQA package. The DQA is a 1mm\* 2.5mm package with flow-through pin-mapping for the high-speed differential lines. It is recommended to place the package right next to the USB 3.0 connector. The GND pin should be connected to GND plane of the board through a large VIA. If a dedicated GND plane is not present right underneath, it is recommended to route to the GND plane through a wide trace. The current associated with IEC ESD stress can be in the range of 30Amps or higher momentarily. A good, low impedance GND path ensures the system robustness against IEC ESD stress.

The TPDxEUSB30 can provide system level ESD protection to the high-speed differential ports (>6 Gbps data rate). The flow-through package offers flexibility for board routing with traces up to 15 mills wide. It allows the differential signal pairs couple together right after they touch the ESD ports of the TPDxEUSB30.



Three TPD2EUSB30 to Protect USB3.0 Class A connector (One Layer Routing)



One TPD4EUSB30 & One TPD2EUSB30 to Protect USB3.0 Class A connector (Two Layer Routing)

Figure 7. Layout Guide with the TPDxEUSB30 at the USB3.0 Class A Connector

### TPDxEUSB30 Eye Pattern Test

See [Figure 9](#) for a demonstration of the TPDxEUSB30 performance the lab set-up. [Figure 8](#) shows a lab board that was designed to demonstrate the degradation of the eye pattern quality with and without the TPD2EUSB30 in the USB 3.0 signal path. [Figure 10](#) shows that there is only ~2 ps jitter penalty to the differential signal when the TPD2EUSB30 device was added in the signal path. Similar setup was employed to measure eye pattern for the TPD4EUSB30.

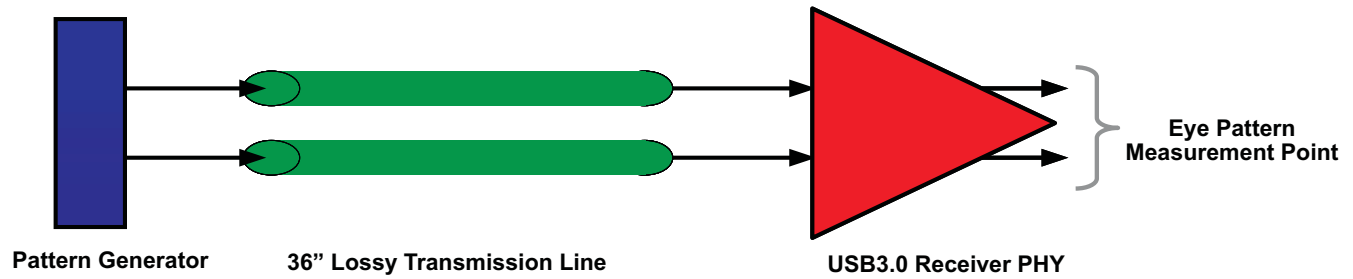


Figure 8. Measurement Setup to collect the Eye Pattern on a Reference Board with TPD2EUSB30

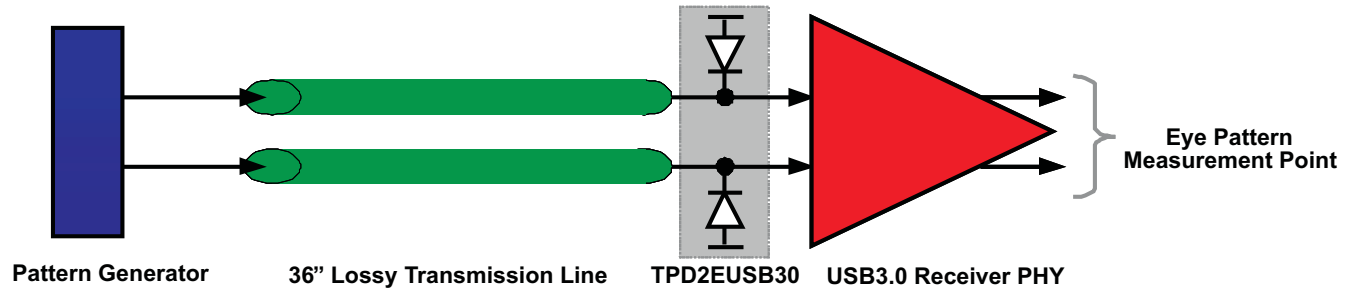


Figure 9. Measurement Setup to collect the Eye Pattern on a Reference Board with TPD2EUSB30

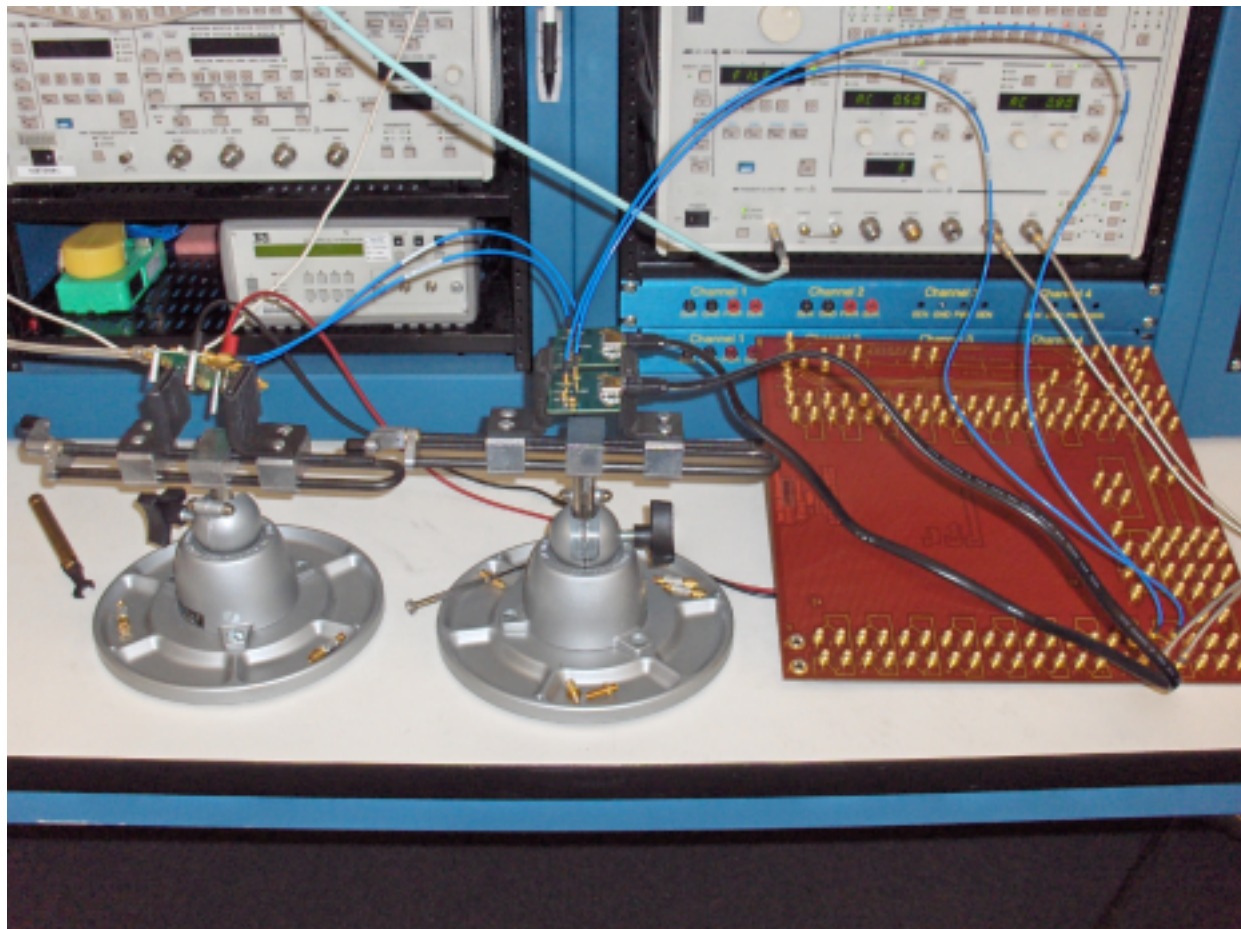
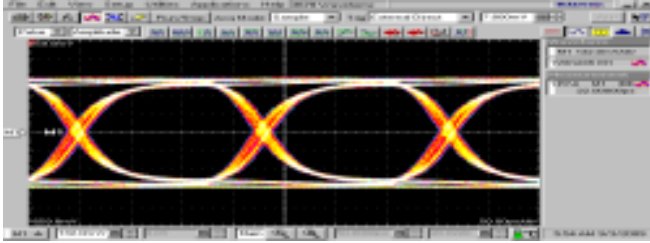
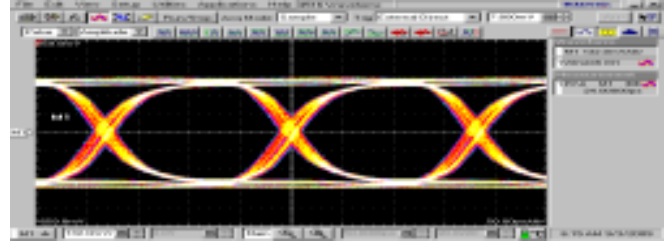


Figure 10. Lab Setup for the Eye-Pattern Measurement with TPDxEUSB30

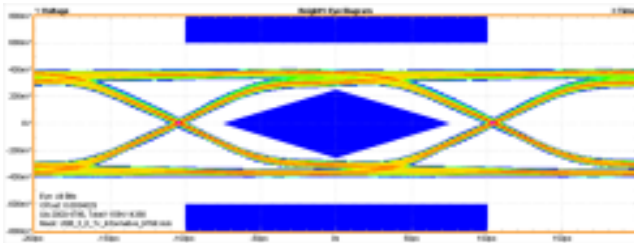




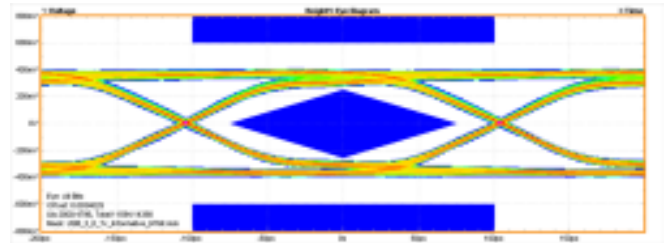
**Figure 11. Output Eye Diagram Without TPD2EUSB30 (Figure 8 Setup, 5 Gbps Data Rate)**



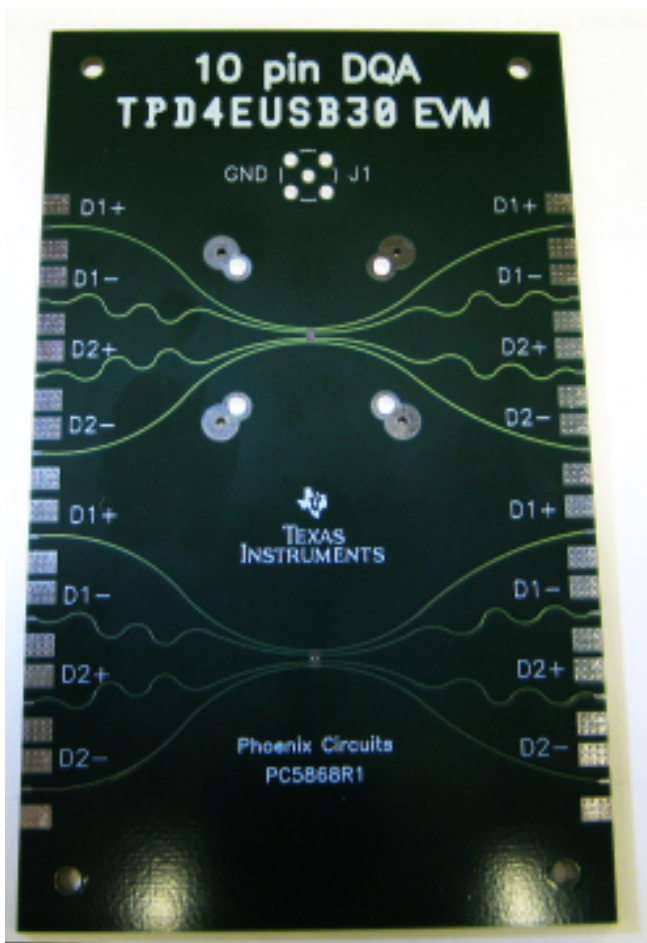
**Figure 12. Output Eye Diagram with the TPD2EUSB30 (Figure 8 Setup, 5 Gbps Data Rate)**



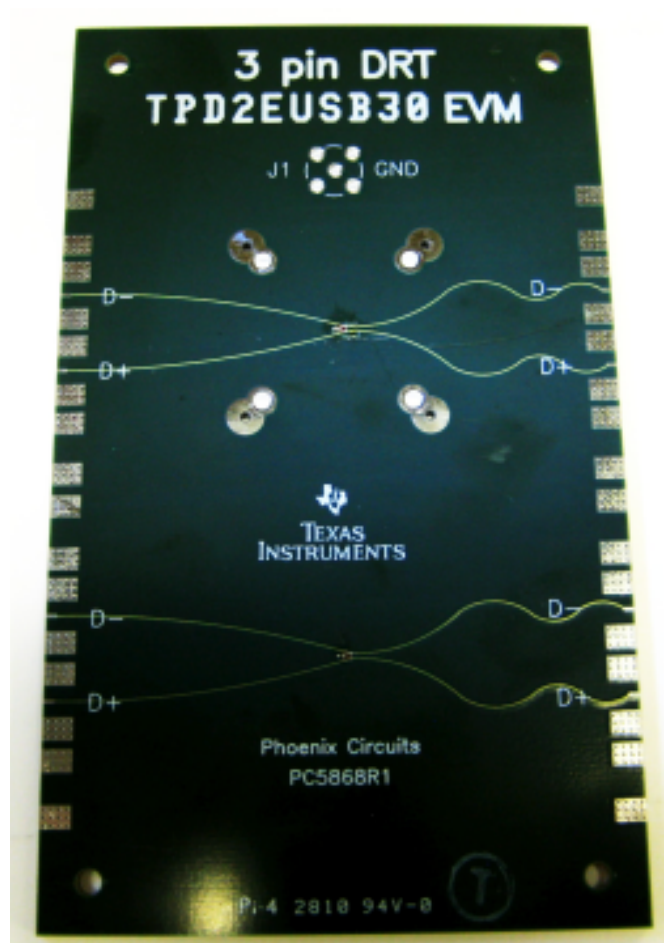
**Figure 13. Output Eye Diagram Without the TPD4EUSV30 (5 Gbps Data Rate)**



**Figure 14. Output Eye Diagram with the TPD4EUSV30 (5 Gbps Data Rate)**



**Figure 15. TPDxEUSV30 EVM – TPD4EUSB30 Side**



**Figure 16. TPDxEUSV30 EVM – TPD2EUSB30 Side**



## PACKAGING INFORMATION

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/<br>Ball Finish | MSL Peak Temp. <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|-------------------------------|
| TPD2EUSB30DRTR   | ACTIVE                | SOT          | DRT             | 3    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C                  |
| TPD4EUSB30DQAR   | ACTIVE                | SON          | DQA             | 10   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C                  |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/rohs> for more information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for high temperature soldering processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die attach between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br and Sb are not permitted in homogeneous material).

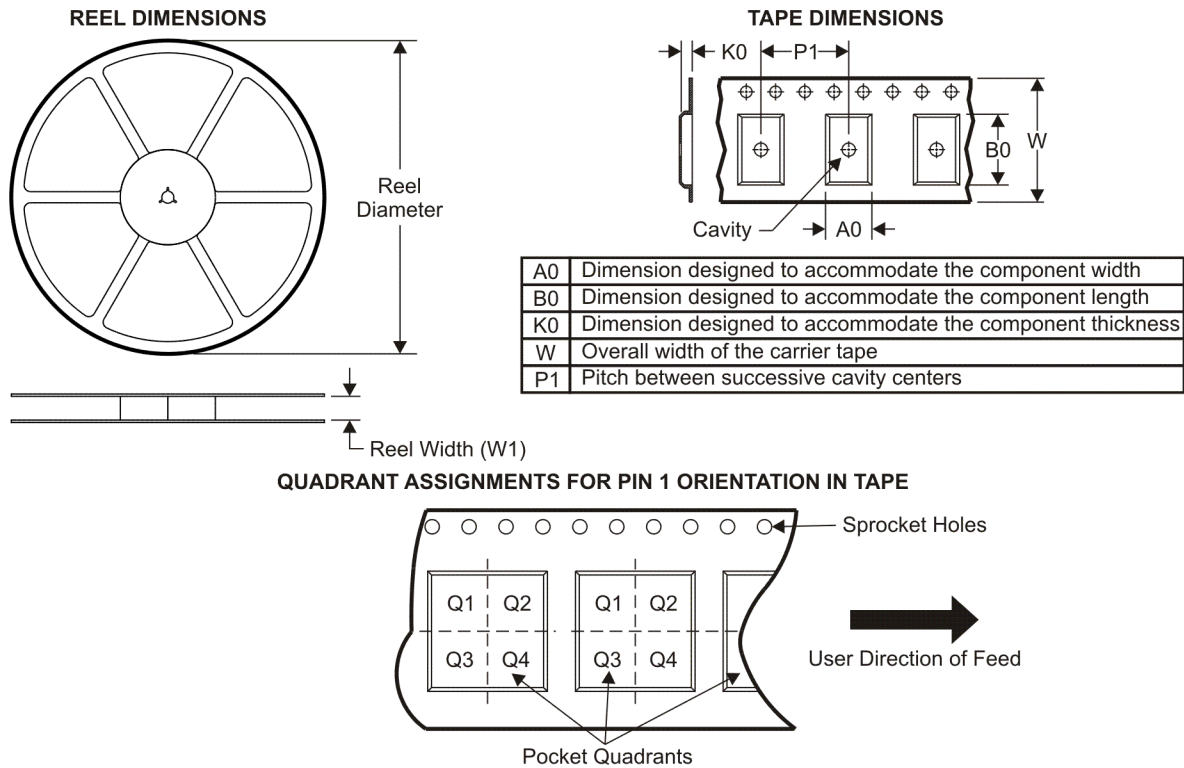
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPD2EUSB30DRTR | SOT          | DRT             | 3    | 3000 | 180.0              | 8.4                | 1.16    | 1.16    | 0.63    | 4.0     | 8.0    | Q3            |
| TPD4EUSB30DQAR | SON          | DQA             | 10   | 3000 | 180.0              | 8.4                | 1.3     | 2.83    | 0.65    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS

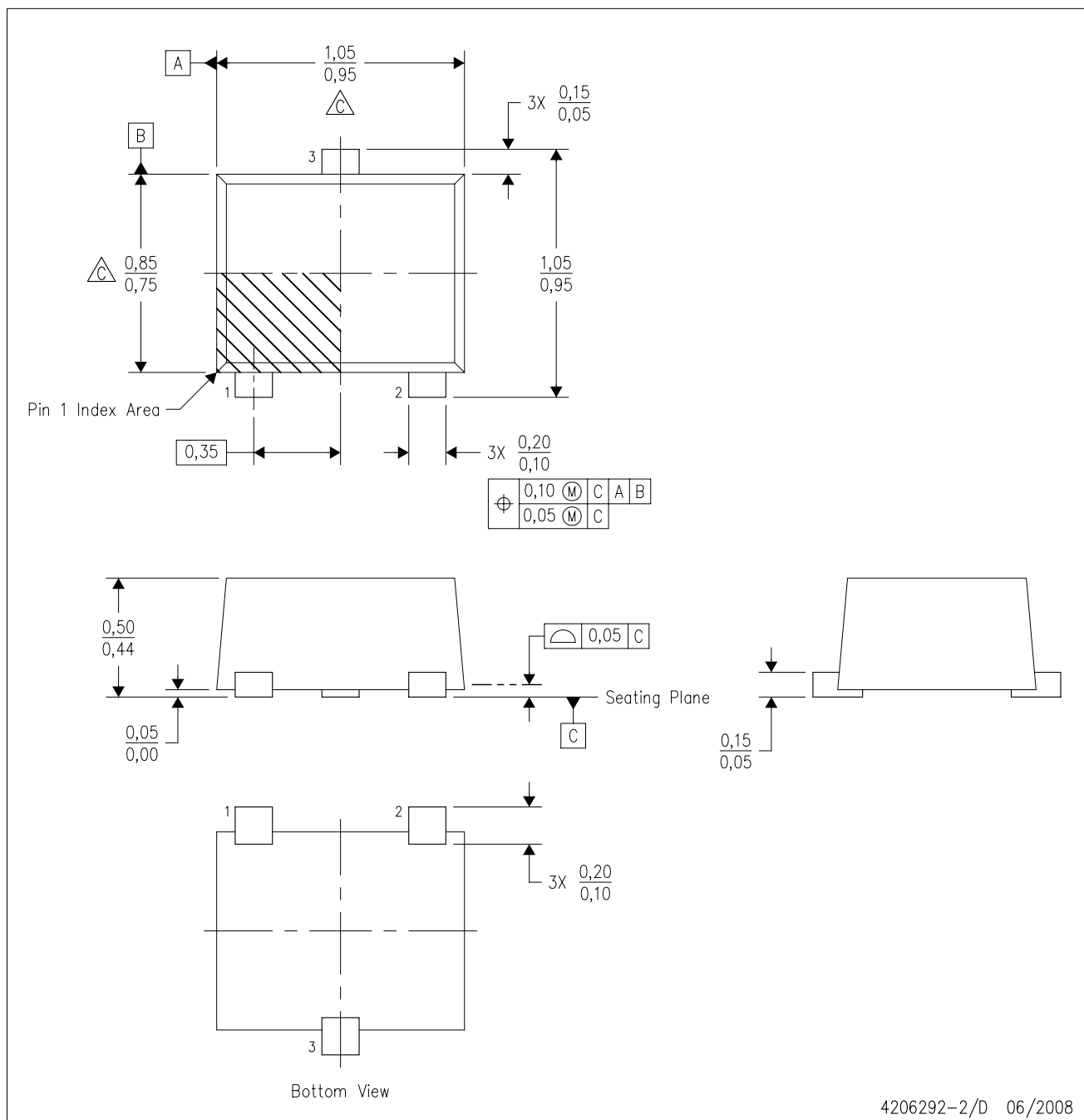


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPD2EUSB30DRTR | SOT          | DRT             | 3    | 3000 | 202.0       | 201.0      | 28.0        |
| TPD4EUSB30DQAR | SON          | DQA             | 10   | 3000 | 202.0       | 201.0      | 28.0        |

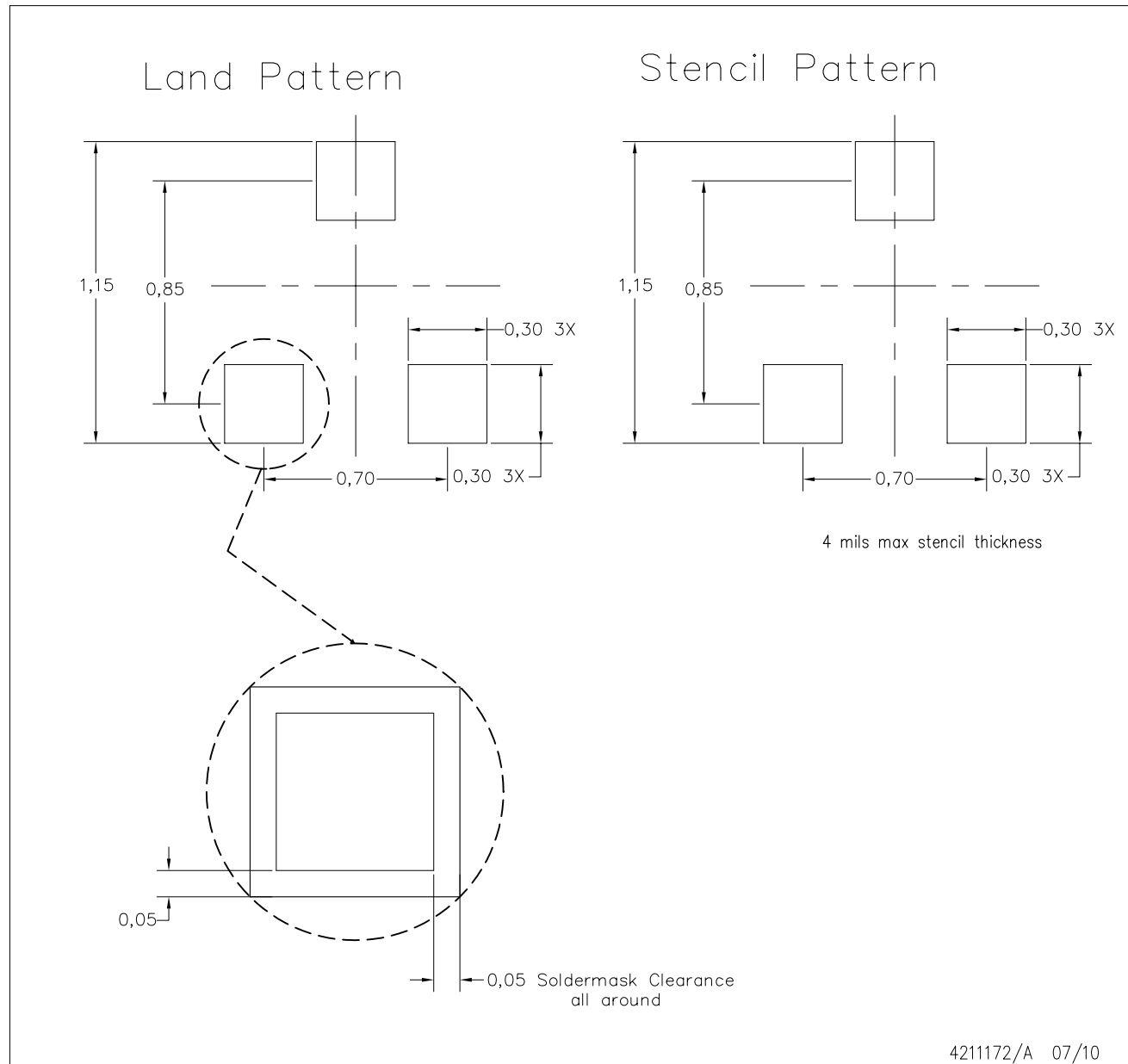
DRT (R-PDSO-N3)

PLASTIC SMALL OUTLINE



4206292-2/D 06/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,10 per end or side.
  - D. JEDEC package registration is pending.

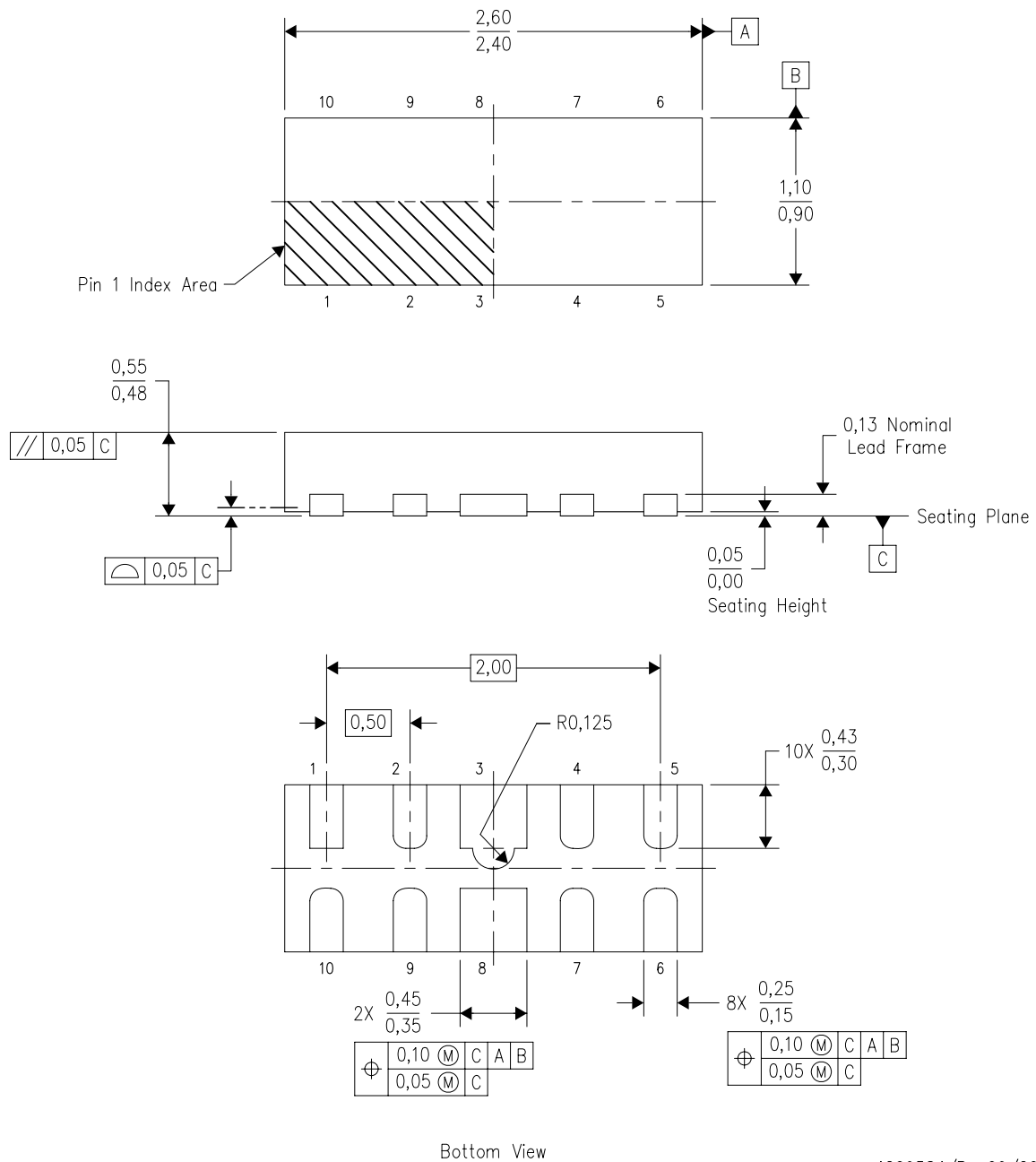


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

[查询"TPD2EUSB30"供应商](#)

DQA (R-PSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD

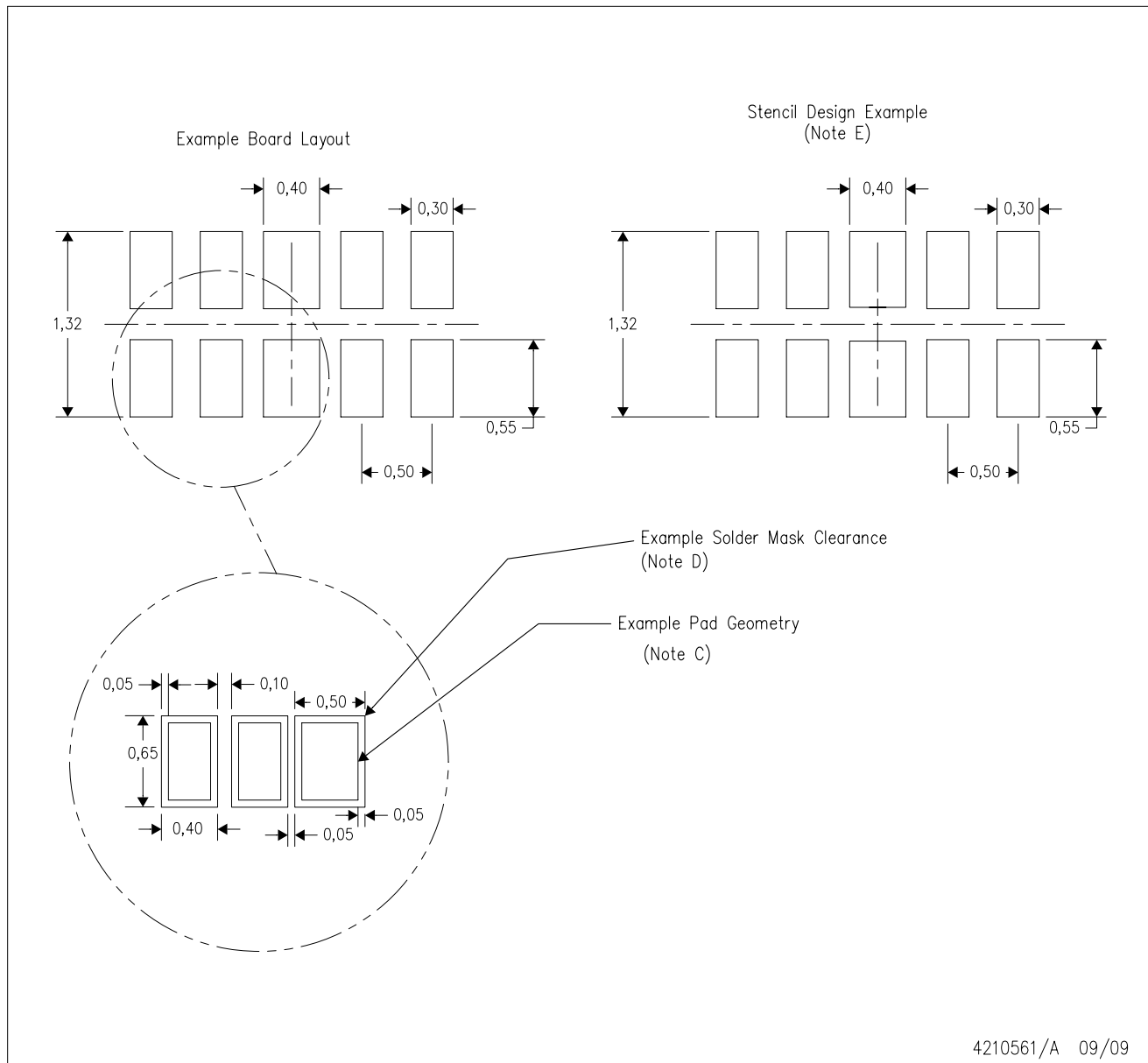


4209584/B 09/2009

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - SON (Small Outline No-Lead) package configuration.



DQA (R-PSON-N10)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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|-----------------------------|--|----------------------------|--|
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| Data Converters             | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>     | Automotive                 | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| DLP® Products               | <a href="http://www.dlp.com">www.dlp.com</a>                       | Communications and Telecom | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| DSP                         | <a href="http://dsp.ti.com">dsp.ti.com</a>                         | Computers and Peripherals  | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Clocks and Timers           | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>           | Consumer Electronics       | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Interface                   | <a href="http://interface.ti.com">interface.ti.com</a>             | Energy                     | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Logic                       | <a href="http://logic.ti.com">logic.ti.com</a>                     | Industrial                 | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Power Mgmt                  | <a href="http://power.ti.com">power.ti.com</a>                     | Medical                    | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Microcontrollers            | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> | Security                   | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| RFID                        | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>               | Space, Avionics & Defense  | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| RF/IF and ZigBee® Solutions | <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>               | Video and Imaging          | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |
|                             |  | Wireless                   | <a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>                   |