Description

The ACS8527 is a highly integrated, single-chip, MUX with PLL solution for protection switching between two SECs (SDH/SONET Equipment Clocks) from Master and Slave SETS (Synchronous Equipment Timing Source) clock cards, for line cards in a PDH, SONET or SDH Network Element. The ACS8527 has fast activity monitors on the inputs and will raise a flag on a pin if there is a loss of activity on the currently selected input. The protection switching between the input reference clock sources is controlled by an external pin.

The ACS8527 has two SEC reference clock input ports, configured for expected frequency by setting hardware pins.

The ACS8527 can perform frequency translation, converting, for example, an 8 kHz SEC input clock from a backplane into a 155.52 MHz clock for local line cards.

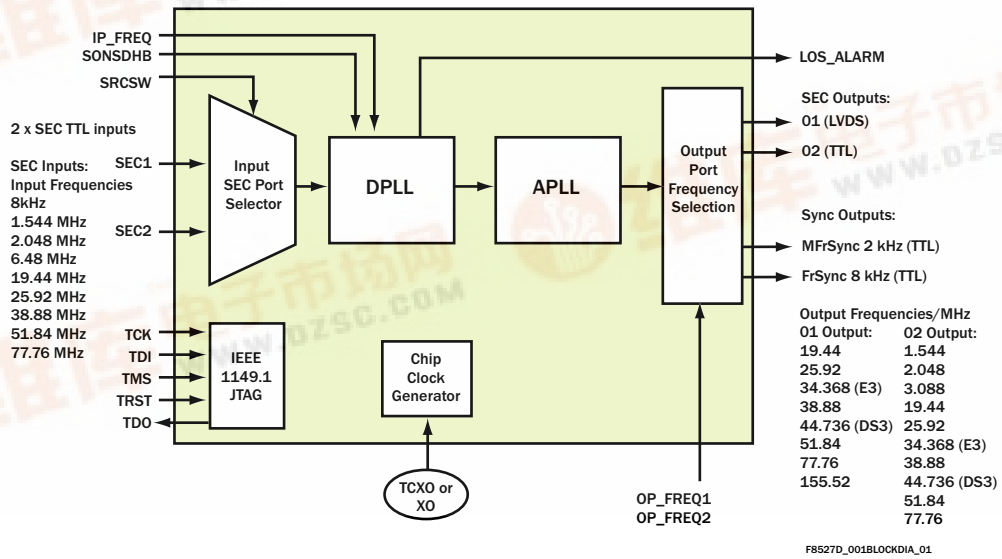
The ACS8527 generates two independent SEC clock outputs, one on a LVDS port and one on a TTL/CMOS port, at spot frequencies configured by hardware pins. The spot frequencies range from 1.544 MHz up to 155.52 MHz. The ACS8527 also provides an 8 kHz Frame Sync output and 2 kHz Multi-Frame Sync output.

Features

- Line card protection switch - partners Semtech SETS devices for Stratum 3E/3/4E/4 PDH, SONET or SDH applications
- High performance DPLL/APLL solution
- Output jitter compliant to STM-1
- Two independent SEC inputs ports (TTL)
- Four independent output ports:
  - Two clock ports: one LVDS, one TTL
  - Two Syncs (TTL): 8 kHz FrSync & 2 KHz MFrSync
- I/O frequencies configurable via hardware pins:
  - TTL I/O ports: spot frequencies 1.544 MHz to 77.76 MHz
  - LVDS output port: spot frequencies 19.44 MHz to 155.52 MHz
- Digital Holdover mode on input failure
- "Loss of activity" on selected input flagged on dedicated pin
- Source switch under external hardware control
- 70 Hz (acquisition) /35 Hz (locked) DPLL bandwidth
- Output clock phase continuity to GR-1244-CORE[13]
- Single 3.3 V operation, 5 V I/O compatible
- IEEE 1149.1 JTAG Boundary Scan is supported
- Operating temperature (ambient) of -40 to +85 °C
- Available in LQFP 64 package
- Lead (Pb)-free version available (ACS8527T). RoHS and WEE compliant

Block Diagram

Figure 1 Block Diagram of the ACS8527 MUXPLL



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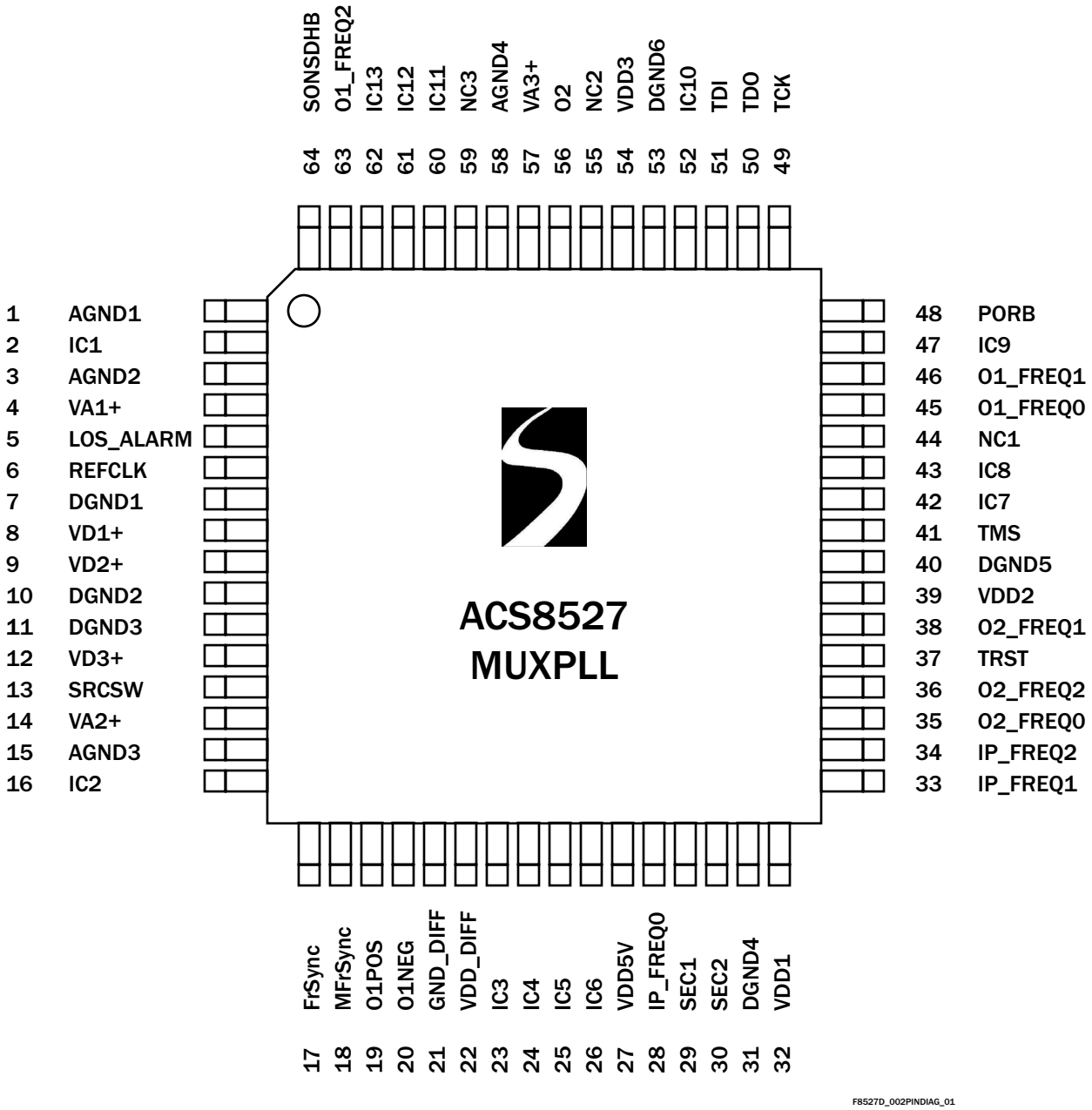
Pin Diagram

Figure 2 ACS8527 Pin Diagram



Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
8, 9, 12	VD1+, VD2+, VD3+	P	-	Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±10%.
22	VDD_DIFF	P	-	Supply Voltage: Digital supply for differential output pins 19 and 20, +3.3 Volts ± 10%.
27	VDD5V	P	-	Digital Supply for +5 Volts tolerance to input pins. Connect to +5 Volts (±10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
32, 39, 54	VDD1, VDD2, VDD3,	P	-	Supply Voltage: Digital supply to logic, +3.3 Volts ±10%.
4	VA1+	P	-	Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±10%.
14, 57	VA2+, VA3+	P	-	Supply Voltage: Analog supply to output PLLs APLL2 and APLL1, +3.3 Volts ± 10%.
15, 58	AGND3, AGND4			Supply Ground: Analog ground for output PLLs APLL2 and APLL1.
7, 10, 11	DGND1, DGND2, DGND3	P	-	Supply Ground: Digital ground for components in PLLs.
31, 40, 53	DGND4, DGND5, DGND6	P	-	Supply Ground: Digital ground for logic.
21	GND_DIFF	P	-	Supply Ground: Digital ground for differential output pins 19 and 20.
1, 3	AGND1, AGND2	P	-	Supply Ground: Analog grounds.

Note...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected

Pin Number	Symbol	I/O	Type	Description
2, 16, 23, 24, 25, 26, 42, 43, 47, 52, 60, 61, 62	IC1, IC2, IC3, IC4, IC5, IC6, IC7, IC8, IC9, IC10, IC11, IC12, IC13	-	-	Internally Connected: Leave to float.
44, 55, 59	NC1, NC2, NC3	-	-	Not Connected: Leave to float

Table 3 Other Pins

Pin Number	Symbol	I/O	Type	Description
5	LOS_ALARM	O	TTL/CMOS	Loss Of Signal Alarm: Flag to indicate loss of activity of currently selected reference source is raised on this pin.
6	REFCLK	I	TTL	Reference Clock: 12.800 MHz (refer to section headed Local Oscillator Clock).
13	SRCSW	I	TTL_D	Source Switching: Controls switchover between SEC1 and SEC2 inputs as the selected reference. SRCSW must be held *High* on power-up or reset, and for a further 251 ms after PORB has gone *High*. See "Initialization" on page 7.
17	FrSync	O	TTL/CMOS	Output Reference: 8 kHz Frame Sync output.
18	MFrSync	O	TTL/CMOS	Output Reference: 2 kHz Multi-Frame Sync output.
19, 20	O1POS, O1NEG	O	LVDS	Output Reference 1: Differential output. LVDS.
28	IP_FREQ0	I	TTL_D	Input Reference Frequency Select: Frequency select for input SEC1 and SEC2.
29	SEC1	I	TTL_D	Input Reference 1: Primary input.
30	SEC2	I	TTL_D	Input Reference 2: Secondary input.
33	IP_FREQ1	I	TTL_D	Input Reference Frequency Select: Frequency select for input SEC1 and SEC2.
34	IP_FREQ2	I	TTL_D	Input Reference Frequency Select: Frequency select for input SEC1 and SEC2.
35	O2_FREQ0	I	TTL_D	Output O2 Frequency Select: Frequency select for output O2.
36	O2_FREQ2	I	TTL_D	Output O2 Frequency Select: Frequency select for output O2.
37	TRST	I	TTL_D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for normal device operation (JTAG logic transparent). NC if not used.
38	O2_FREQ1	I	TTL_D	Output O2 Frequency Select: Frequency select for output O2.
41	TMS	I	TTL_D	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. NC if not used.
45	O1_FREQ0	I	TTL^U	Output O1 Frequency Select: Frequency select for output O1.
46	O1_FREQ1	I	TTL^U	Output O1 Frequency Select: Frequency select for output O1.
48	PORB	I	TTL^U	Power-On Reset: Master reset. If PORB is forced *Low*, all internal states are reset back to default values.
49	TCK	I	TTL_D	JTAG Clock: Boundary Scan clock input.
50	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK.
51	TDI	I	TTL_D	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. NC if not used.
56	O2	O	TTL/CMOS	Output Reference: Programmable, default 19.44 MHz.
63	O1_FREQ2	I	TTL^U	Output O1 Frequency Select: Frequency select for output O1.
64	SONSDHB	I	TTL_D	SONET or SDH frequency select: Sets the device for SONET or SDH frequencies on power-up/reset.

Introduction

The ACS8527 is a highly integrated, single-chip solution for protection switching of two SEC inputs from, for example, Master and Slave SETS clock cards sources, for Line Cards in a SONET or SDH Network Element. The ACS8527 has fast activity monitors on the SEC clock inputs.

The ACS8527 is a standalone part where all input and output frequencies are set by external control using the IP_FREQ, OP_FREQ and SONSDHB pins.

The SRCSW pin is used to select one of the two SEC inputs to lock to. The SRCSW pin must remain *High* for an initialization period of at least 251 ms following power-up or reset (251 ms after the PORB signal has gone *High*). SRCSW *Low* immediately after a power-up or reset is not supported.

The ACS8527 has two SEC inputs from which it can generate independent clocks on outputs 01 and 02 (11 possible output clock frequencies). In addition, there are two Sync outputs; 8 kHz Frame Synchronization (FrSync) signal and a 2 kHz Multi-Frame Synchronization (MFrSync) signal.

Initially the ACS8527 generates a stable, low-noise clock signal at a frequency to the same accuracy as the external oscillator. The device always attempts to lock to one of its inputs (according to the value on the SRCSW pin). Once locked to a reference the accuracy of the output clock is determined directly by the accuracy of the input reference. In the absence of any input references the device simply maintains its most recent frequency in a Digital Holdover mode. However, as soon as the DPLL (Digital Phase Locked Loop) detects an input presence, it will attempt to lock to it and will not “qualify” it first. As soon as the DPLL detects a failure on the input, the DPLL freezes its operating frequency and raises the LOS alarm on device pin LOS_ALARM.

The overall PLL (Phased Locked Loop) loop bandwidth, damping, pull-in range and frequency accuracy are all determined by fixed digital parameters that provide a consistent level of performance. An Analog PLL (APLL) takes the signal from the DPLL output and provides a lower jitter output. The APLL bandwidth is set four orders of magnitude higher than the DPLL bandwidth. This ensures that the overall system performance still maintains the advantage of consistent behavior provided by the digital approach. The DPLLs are clocked by the external oscillator module (TCXO or XO) so that prior to initial lock (with no input reference) or in Digital Holdover, the frequency stability is only determined by the stability of the external oscillator module. This gives the key advantage of confining all temperature critical components to one well defined and pre-calibrated oscillator module, whose performance can be chosen to match the application.

An Evaluation board is available for device introduction. This has its own documentation “ACS8527-EVB”.

General Description

The following description refers to the Block Diagram (Figure 1 on page 1).

Inputs

The ACS8527 SETS device has two TTL/CMOS compatible SEC input ports. They are 3 V and 5 V compatible (with clamping if required by connecting the VDD5V pin). Refer to the “Electrical Specifications” on page 10 for more information on electrical compatibility.

Input frequencies supported range from 8 kHz to 77.76 MHz. Common E1, DS1, OC-3 and sub-divisions are supported as spot frequencies that the DPLLs will directly lock to.

In addition to the SEC inputs, there are four configuration pins IP_FREQ [2:0] and SONSDHB used to configure the input to expect a particular input frequency (same value applies to both inputs), and a control pin SRCSW for switching between SEC1 and SEC2 as the selected input reference to which the device tries to lock.

Preconfiguring Inputs - Expected Input Frequency

The inputs SEC1 and SEC2 must be preconfigured to expect a particular input frequency. This can be selected from a range of spot frequencies by configuring the hardware pins IP_FREQ [2:0] and SONSDHB, which are read on reset.

The combined pin states of IP_FREQ [2:0] and SONSDHB represent a 4-bit word which addresses a particular frequency value as given in Table 4.

The frequency selected by the hardware configuration is always applied to both inputs on Power-up or Reset, so both will be preconfigured to expect the same frequency.

Table 4 Hardware Configuration for Selecting Expected Input Frequency on SEC1 and SEC2

IP_FREQ Pins			SONSDHB Pin	Input frequency
2	1	0		
0	0	0	X	8 kHz
0	0	1	0	2.048 MHz
			1	1.544 MHz
0	1	0	X	6.48 MHz
0	1	1	X	19.44 MHz
1	0	0	X	25.92 MHz
1	0	1	X	38.88 MHz
1	1	0	X	51.84 MHz
1	1	1	X	77.76 MHz

Preconfiguring Inputs - SONET/SDH

The SONSDHB pin is used to select SDH or SONET mode for the entire device and its setting affects parameters other than just the expected input frequency selection, e.g. output frequency. To set the device for use in a SONET network, set SONSDHB high. For SDH, set SONSDHB low.

Selection of Input SECs

Initialization

Switching between inputs SEC1 and SEC2 is triggered directly from a dedicated pin (SRCSW), though for the device to operate properly, the device must first be initialized by holding the pin *High* during reset and for at least a further 251 ms after PORB has gone *High* (250 ms allowance for the internal reset to be removed plus 1 ms allowance for APLLs to start-up and become stable). If SCRSW is held *Low* at any time during the 251 ms initialization period, this will result in incorrect device operation. A simple external circuit to set SCRSW high for the required period is shown in the “Simplified Application Schematic” on page 18.

SEC Selection - SRCSW pin

After the ACS8527 has been initialized (see previous “Initialization” section), then the value of SRCSW pin directly selects either SEC1 (SRCSW *High*) or SEC2 (SRCSW *Low*). The frequency tolerance of SEC1 and SEC2 is ± 80 ppm with respect to the local oscillator clock.

After initialization, the output clocks are stable and the device will operate as a simple switch, with the DPLL trying to lock on to the selected reference source.

Output Clock Phase Continuity on Source Switchover

A phase offset between SEC inputs will be seen as a phase shift on the output on source switchover equal to the input phase offset. (Note...The ACS8527 has no Phase Build-out function to accommodate this. If this function is required, it is available on the AS8525 LC/P device).

The rate of change of phase on the output, during the time between input switchover and the output settling to a steady state, is dependent on input frequency, and input phase change. The ACS8527 always complies with GR-1244-CORE[13] spec for Stratum 3 (max rate of phase change of 81ns/1.326 ms), for input frequencies at 6.48 MHz or higher.

For inputs at a lower frequency than 6.48 MHz (e.g. 8 kHz), then to ensure compliance with GR-1244-CORE[13], the input phase difference between the Master and Slave inputs to the line card PLL should be limited to less than 190 ns. A well designed system would have master and slave clock from the clock sync cards aligned to within a few nanoseconds. In which case a complete system using the Semtech SETS clock card parts (ACS8530, ACS8520 or ACS8510) and this line card part would be fully compliant to GR-1244-CORE[13] specifications under all conditions due to the lower frequency range and bandwidth set at the clock card end.

Phase Locked Loops (PLLs)

The PLL circuitry (See Figure 1) is represented by a DPLL and an output multiplying and filtering APLL. The device is more complex than the representation suggests, with several DPLLs and APLLs being used in different configurations to provide a range of frequencies at the outputs, with the internal configuration optimizing for jitter filtering and wander tracking. The output frequencies available are shown in Table 6.

The DPLL initially tries to lock to the input frequency of the selected input SEC. It uses a wide “acquisition” bandwidth setting until it has achieved frequency lock, then the DPLL switches to using a narrower “tracking” (locked) bandwidth setting as it locks to the phase of the input.

DPLL Acquisition Bandwidth

The ACS8527 DPLL has a preset acquisition bandwidth of 70 Hz.

DPLL Input Tracking (Locked) Bandwidth

The ACS8527 DPPL has a preset tracking bandwidth of 35 Hz. This bandwidth setting corresponds to the -3 dB jitter attenuation point on the ACS8527's jitter transfer characteristic.

DPLL Damping Factor

The DPLL damping factor is 10, giving a PLL jitter transfer peak gain of 0.06 dB.

Fast Activity Monitor

Anomalies on the selected clock have to be detected as they occur and the PLL must be temporarily isolated until the clock is once again pure. The phase locked loop itself contains a fast activity monitor such that within approximately two missing input clock cycles, the LOS alarm on pin LOS_ALARM is raised and the DPLL is frozen in Digital Holdover mode. With the DPLL in Digital Holdover mode it is isolated from further disturbances. If the input becomes active again then the DPLL will continue to lock to the input, with little disturbance.

Outputs

The ACS8527 delivers four output signals on the following ports: Two clocks, one each on outputs O1 and O2, and two Sync signals, one each on output ports FrSync and MFrSync. Outputs O1 and O2 are independent of each other and are individually selectable. Output O1 is an LVDS compatible differential port (pins O1POS and O1NEG). Output O2 (pin O2) and the Sync outputs are TTL/CMOS compatible. The two Sync outputs, FrSync (8 kHz) and MFrSync (2 kHz), are derived from the DPLL.

Output Frequency Selection

The frequencies available on the outputs can be selected from a range of spot frequencies by hardware selection, configuring the pins OP_FREQ1 [2:0], OP_FREQ2[2:0] and SONSDH, which are read on reset.

Tables 5 and 6 show the hardware settings for selecting from 11 output frequencies on outputs O1 and O2.

Table 5 Output 01 Frequency Selection by Hardware Configuration

01_FREQ			SONSDHB Pin	Output Frequency/ MHz	Jitter Level (typ)	
2	1	0			rms (ps)	p-p (ns)
0	0	0	X	0	-	-
0	0	1	0	34.368	120	1
			1	44.736	110	1
0	1	0	X	19.44	60	0.6
0	1	1	X	25.92	60	0.6
1	0	0	X	38.88	60	0.6
1	0	1	X	51.84	60	0.6
1	1	0	X	77.76	60	0.6
1	1	1	X	155.52	60	0.6

Table 6 Output 02 Frequency Selection by Hardware Configuration

02_FREQ			SONSDHB Pin	01_FREQ = "001"	Output Frequency/ MHz	Jitter Level (typ)	
2	1	0				rms (ps)	p-p (ns)
0	0	0	X	X	0	-	-
0	0	1	0	FALSE	2.048	400	2
			1		1.544	200	1.2
0	0	1	0	TRUE	2.048	900	0.45
			1		3.088	110	0.75
0	1	0	0	X	34.368	120	1
			1	X	44.736	110	1
0	1	1	X	X	19.44	60	0.6
1	0	0	X	X	25.92	60	0.6
1	0	1	X	X	38.88	60	0.6
1	1	0	X	X	51.84	60	0.6
1	1	1	X	X	77.76	60	0.6

Local Oscillator Clock

The Master system clock on the ACS8527 should be provided by an external clock oscillator of frequency 12.800 MHz. Wander on the local oscillator clock will not have a significant effect on the output clock whilst in Locked mode. Prior to initial lock or in Digital Holdover mode, wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator.

Please contact Semtech for information on crystal oscillator suppliers.

Power-On Reset

The Power-On Reset (PORB) pin resets the device if forced *Low*. The reset is asynchronous, the minimum *Low* pulse width is 5 ns. Reset must be asserted at power on, and may be re-asserted at any time to restore defaults. This is implemented simply using an external capacitor to GND along with the internal pull-up resistor. The ACS8527 holds itself in a reset state for 250 ms after the PORB pin has been pulled *High*. In normal operation PORB should be held *High*.

Status Reporting

In the event of loss of SEC input signal, LOS flag is raised on the LOS_ALARM pin. The LOS alarm is active *low*, and *high impedance* when inactive, i.e. when an LOS alarm exists, the output will be driven *low*; with no LOS alarm, the output will float. This is designed to be able to be connected to a processor together with other interrupt sources to trigger an interrupt. The output will require a pull-up resistor to pull the voltage up when the alarm is inactive.

JTAG

The JTAG connections on the ACS8527 allow a full boundary scan to be made. The JTAG implementation is fully compliant to IEEE 1149.1[4], with the following minor exceptions, and the user should refer to the standard for further information.

1. The output boundary scan cells do not capture data from the core, and so do not support INTEST. However this does not affect board testing.
2. In common with some other manufacturers, pin TRST is internally pulled *Low* to disable JTAG by default. The standard is to pull *High*. The polarity of TRST is as the standard: TRST *High* to enable JTAG boundary scan mode, TRST *Low* for normal operation.

The JTAG timing diagram is shown in Figure 3.

Over-voltage Protection

The ACS8527 may require Over-voltage Protection on input reference clock ports according to ITU recommendation K.41[10]. Semtech protection devices are recommended for this purpose (see Protection section on Semtech website: http://www.semtech.com.

ESD Protection

Suitable precautions should be taken to protect against electrostatic damage during handling and assembly. This device incorporates ESD protection structures that protect the device against ESD damage at ESD input levels up to at least +/2kV using the Human Body Model (HBD) MIL-STD-883D Method 3015.7, for all pins.

Latchup Protection

This device is protected against latchup for input current pulses of magnitude up to at least ±100 mA to JEDEC Standard No. 78 August 1997.

Figure 3 JTAG Timing

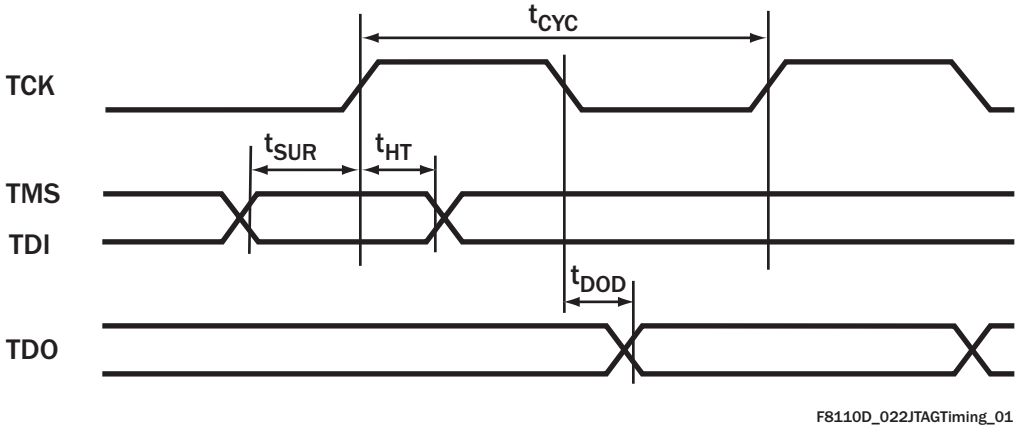


Table 7 JTAG Timing (for use with Figure 3)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Cycle Time	t_{CYC}	50	-	-	ns
TMS/TDI to TCK rising edge time	t_{SUR}	3	-	-	ns
TCK rising to TMS/TDI hold time	t_{HT}	23	-	-	ns
TCK falling to TDO valid	t_{DOD}	-	-	5	ns

Maximum Ratings

Important Note: The Absolute Maximum Ratings, Table 8, are stress ratings only, and functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 8 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage VDD1, VDD2, VDD3, VD1+,VD2+, VD3+, VA1+, VA2+, VA3+, VDD_DIFF	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins)	V_{IN}	-	5.5	V
Output Voltage (non-supply pins)	V_{OUT}	-	5.5	V
Ambient Operating Temperature Range	T_A	-40	+85	^oC
Storage Temperature	T_{STOR}	-50	+150	^oC

Operating Conditions

Table 9 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply (dc voltage) VDD1, VDD2, VDD3, VD1+,VD2+, VD3+, VA1+, VA2+, VA3+, VDD_DIFF	V_{DD}	3.0	3.3	3.6	V
Power Supply (dc voltage) VDD5V	V_{DD5V}	3.0	3.3/5.0	5.5	V
Ambient Temperature Range	T_A	-40	-	+85	^oC
Supply Current (Typical - one 19 MHz output)	I_{DD}	-	110	200	mA
Total Power Dissipation	P_{TOT}	-	360	720	mW

DC Characteristics

Table 10 DC Characteristics: TTL Input Port

Across all operating conditions, unless otherwise stated

PARAMETER	Symbol	Minimum	Typical	Maximum	Units
V_{IN} High	V_{IH}	2	-	-	V
V_{IN} Low	V_{IL}	-	-	0.8	V
Input Current	I_{IN}	-	-	10	µA

Table 11 DC Characteristics: TTL Input Port with Internal Pull-up

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} High	V_{IH}	2	-	-	V
V_{IN} Low	V_{IL}	-	-	0.8	V
Pull-up Resistor	PU	25	-	95	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 12 DC Characteristics: TTL Input Port with Internal Pull-down

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} High	V_{IH}	2	-	-	V
V_{IN} Low	V_{IL}	-	-	0.8	V
Pull-down Resistor (except TCK input)	PD	25	-	95	kΩ
Pull-down Resistor (TCK input only)	PD	12.5	-	47.5	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 13 DC Characteristics: TTL Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{OUT} Low (I_{OL} = 4 mA)	V_{OL}	0	-	0.4	V
V_{OUT} High (I_{OH} = 4 mA)	V_{OH}	2.4	-	-	V
Drive Current	I_D	-	-	4	mA

Table 14 DC Characteristics: LVDS Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVDS Output High Voltage (Note (i))	V_{OHLVDS}	-	-	1.585	V
LVDS Output Low Voltage (Note (i))	V_{OLLVDS}	0.885	-	-	V
LVDS Differential Output Voltage	V_{ODLVDS}	250	-	450	mV

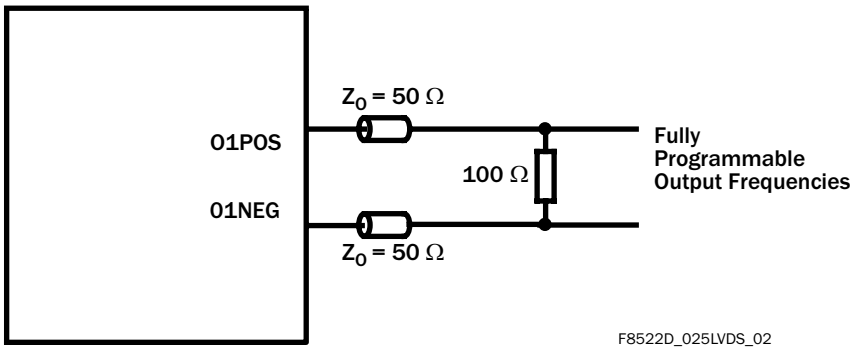
Table 14 DC Characteristics: LVDS Output Port (cont...)

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVDS Change in Magnitude of Differential Output Voltage for complementary States (Note (i))	$V_{DOSLVDS}$	-	-	25	mV
LVDS Output Offset Voltage Temperature = 25°C (Note (i))	V_{OSLVDS}	1.125	-	1.275	V

Notes: (i) With 100 Ω load between the differential outputs.

Figure 4 Recommended Line Termination for LVDS Output Port



Jitter Performance

Output jitter generation measured over 60 second interval, UI p-p max measured using C-MAC E2747 12.8 MHz TCXO on ICT Flexacom tester.

Table 15 Output Jitter Generation at 35 Hz Bandwidth and 8 kHz Input

Test Definition		Jitter Spec	ACS8527 Jitter
Specification	Filter	UI	UI (TYP)
G813[8] for 155 MHz o/p option 1	65 kHz - 1.3 MHz	0.1 p-p	0.073 p-p
G813[8] & G812[7] for 2.048 MHz option 1	20 Hz - 100 kHz	0.05 p-p	0.012 p-p
G813[8] for 155 MHz o/p option 2	12 kHz - 1.3 MHz	0.1 p-p	0.069 p-p
G812[7] for 1.544 MHz o/p	10 Hz - 40 kHz	0.05 p-p	0.011 p-p
G812[7] for 155 MHz electrical	500 Hz - 1.3 MHz	0.5 p-p	0.083 p-p
G812[7] for 155 MHz electrical	65 kHz - 1.3 MHz	0.075 p-p	0.073p-p
ETS-300-462-3[2] for 2.048 MHz SEC o/p	20 Hz - 100 kHz	0.5 p-p	0.012 p-p
ETS-300-462-3[2] for 2.048 MHz SEC o/p	49 Hz - 100 kHz	0.2 p-p	0.012 p-p
ETS-300-462-3[2] for 2.048 MHz SSU o/p	20 Hz - 100 kHz	0.05 p-p	0.012 p-p

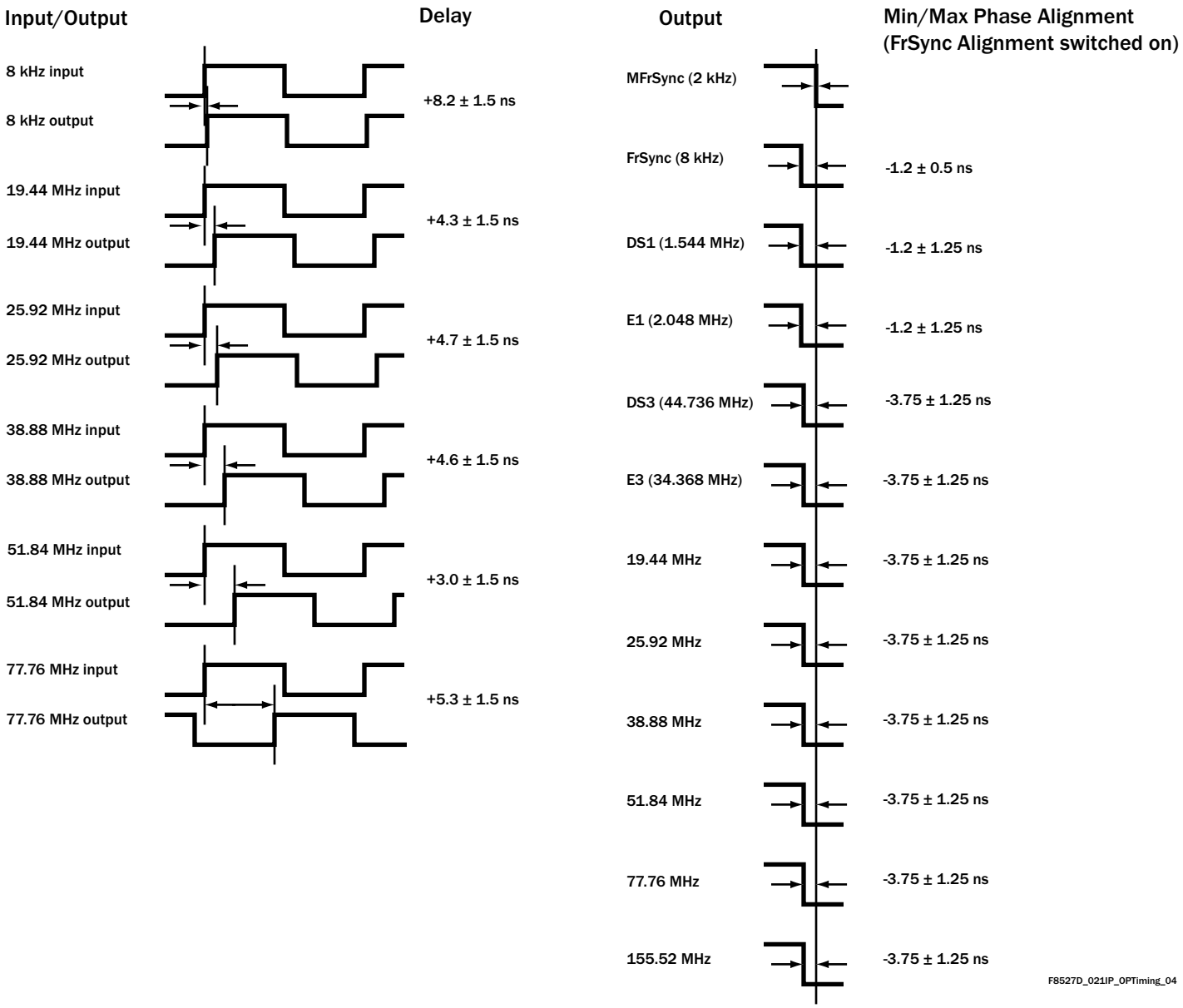
Table 15 Output Jitter Generation at 35 Hz Bandwidth and 8 kHz Input (cont...)

Test Definition		Jitter Spec	ACS8527 Jitter
Specification	**Filter**	**UI**	**UI (TYP)**
ETS-300-462-5[3] for 155 MHz o/p	500 Hz - 1.3 MHz	0.5 p-p	0.083 p-p
ETS-300-462-5[3] for 155 MHz o/p	65 kHz - 1.3 MHz	0.1 p-p	0.073 p-p
GR-253-CORE[11] net i/f, 51.84 MHz o/p	100 Hz - 0.4 MHz	1.5 p-p	0.038 p-p
GR-253-CORE[11] net i/f, 51.84 MHz o/p	20 kHz to 0.4 MHz	0.15 p-p	0.019 p-p
GR-253-CORE[11] net i/f, 155 MHz o/p	500 Hz - 1.3 MHz	1.5 p-p	0.083 p-p
GR-253-CORE[11] net i/f, 155 MHz o/p	65 kHz - 1.3 MHz	0.15 p-p	0.073 p-p
GR-253-CORE[11] cat II elect i/f, 155 MHz	12 kHz - 1.3 MHz	0.1 p-p	0.069 p-p
		0.01 rms	0.009 rms
GR-253-CORE[11] cat II elect i/f, 51.84 MHz	12 kHz - 400 kHz	0.1 p-p	0.008 p-p
		0.01 rms	0.004 rms
GR-253-CORE[11] DS1 i/f, 1.544 MHz	10 Hz - 40 kHz	0.1 p-p	0.0046 p-p
		0.01 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	10 Hz - 8 kHz	0.02 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	8 Hz - 40 kHz	0.025 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	10 Hz - 40 kHz	0.025 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	Broadband	0.05 rms	<0.001 rms
G-742[6] for 2.048 MHz	DC - 100 kHz	0.25 rms	0.012 rms
G-742[6] for 2.048 MHz	18 kHz - 100 kHz	0.05 p-p	0.012 p-p
G-736[5] for 2.048 MHz	20 Hz - 100 kHz	0.05 p-p	0.012 p-p
GR-499-CORE[12] & G824[9] for 1.544 MHz	10 Hz - 40kHz	5.0 p-p	0.001 p-p
GR-499-CORE[12] & G824[9] for 1.544 MHz	8 kHz - 40kHz	0.1 p-p	0.001 p-p
GR-1244-CORE[13] for 1.544 MHz	> 10 Hz	0.05 p-p	0.001 p-p

Note...This table is only for comparing the ACS8527 output jitter performance against values and quoted in various specifications for given conditions. It should not be used to infer compliance to any other aspects of these specifications.

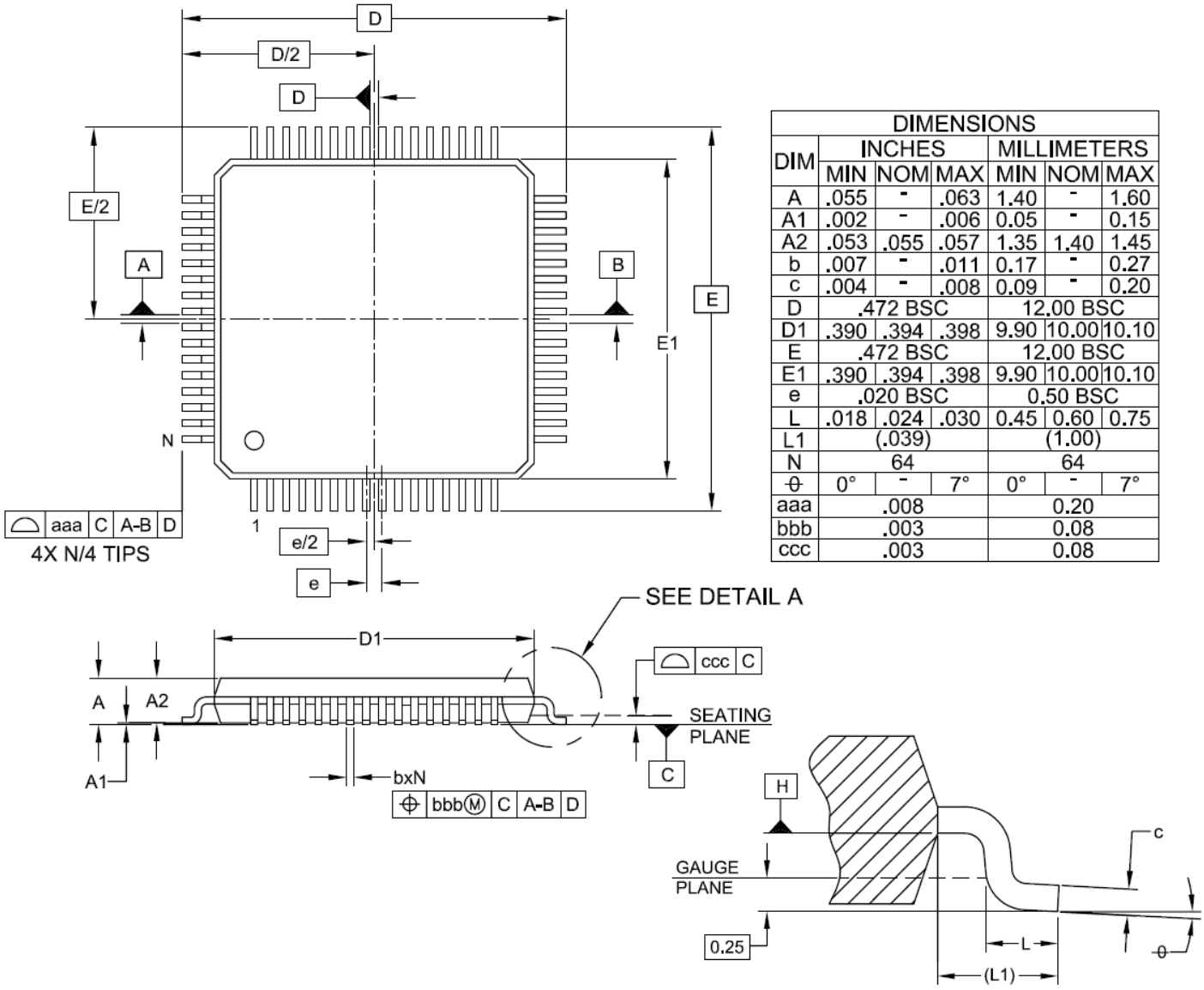
Input/Output Timing

Figure 5 Input/Output Timing (Typical Conditions)



Package Information

Figure 6 LQFP Package



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.055	-	.063	1.40	-	1.60
A1	.002	-	.006	0.05	-	0.15
A2	.053	.055	.057	1.35	1.40	1.45
b	.007	-	.011	0.17	-	0.27
c	.004	-	.008	0.09	-	0.20
D	.472 BSC			12.00 BSC		
D1	.390	.394	.398	9.90	10.00	10.10
E	.472 BSC			12.00 BSC		
E1	.390	.394	.398	9.90	10.00	10.10
e	.020 BSC			0.50 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.00)		
N	64			64		
θ	0°	-	7°	0°	-	7°
aaa	.008			0.20		
bbb	.003			0.08		
ccc	.003			0.08		

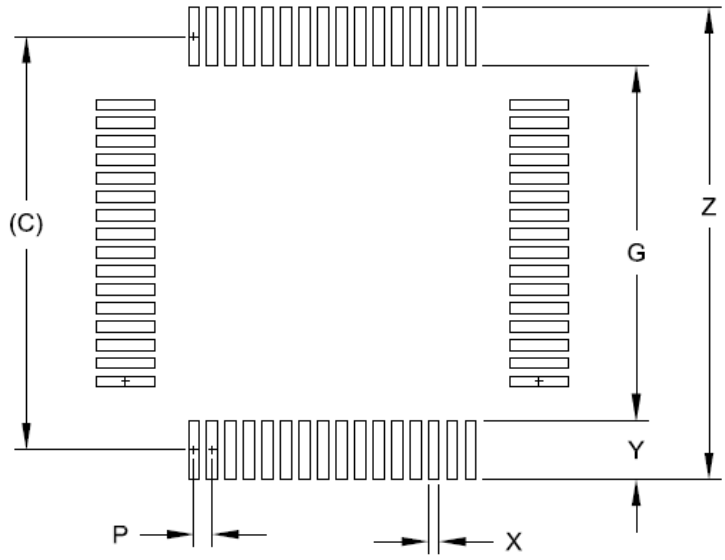
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D1" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-026, VARIATION BCD.

Thermal Conditions

The device is rated for full temperature range when this package is used with a 4 layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

Figure 7 Typical 64-Pin LQFP Package Landing Pattern



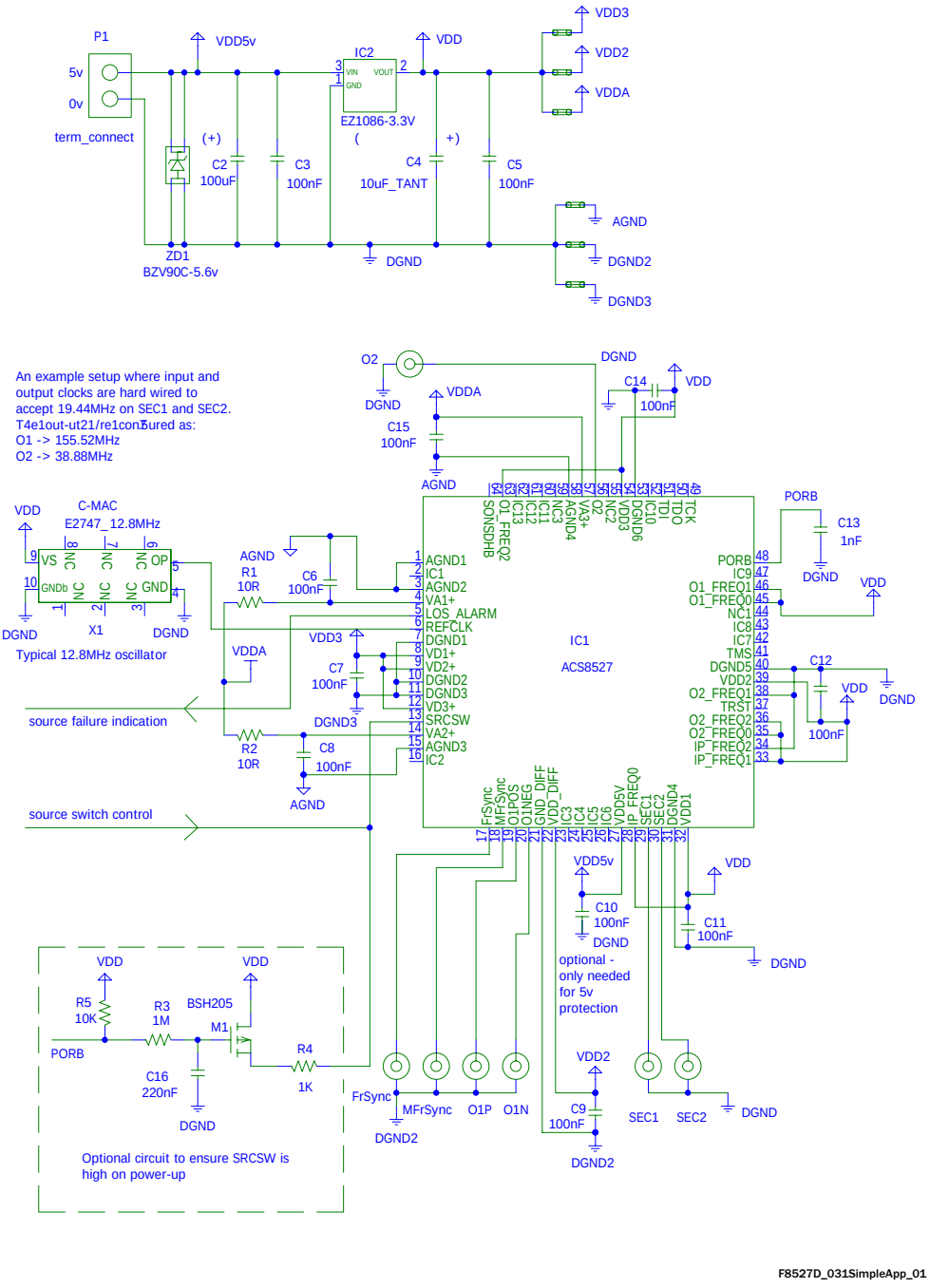
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.441)	(11.20)
G	.378	9.60
P	.020	0.50
X	.012	0.30
Y	.063	1.60
Z	.504	12.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.
3. REFERENCE IPC-SM-782A, RLP NO. 572A.

Application Information

Figure 8 Simplified Application Schematic



Abbreviations

APLL	Analogue Phase Locked Loop
DPLL	Digital Phase Locked Loop
DS1	1544 kbit/s interface rate
E1	2048 kbit/s interface rate
I/O	Input - Output
LOS	Loss Of Signal
LQFP	Low profile Quad Flat Pack
LVDS	Low Voltage Differential Signal
PDH	Plesiochronous Digital Hierarchy
PLL	Phase Locked Loop
POR	Power-On Reset
ppm	parts per million
p-p	peak-to-peak
rms	root-mean-square
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing source
SONET	Synchronous Optical Network
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
TCXO	Temperature Compensated Crystal Oscillator
UI	Unit Interval
WEEE	Waste Electrical and Electronic Equipment (directive)
XO	Crystal Oscillator

References

[1] AT & T 62411 (12/1990)
ACCUNET® T1.5 Service description and Interface Specification

[2] ETSI ETS 300 462-3, (01/1997)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3: The control of jitter and wander within synchronization networks

[3] ETSI ETS 300 462-5 (09/1996)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment

[4] IEEE 1149.1 (1990)
Standard Test Access Port and Boundary-Scan Architecture

[5] ITU-T G.736 (03/1993)
Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s

[6] ITU-T G.742 (1988)
Second order digital multiplex equipment operating at 8448 kbit/s, and using positive justification

[7] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

[8] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC)

[9] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

[10] ITU-T K.41 (05/1998)
Resistability of internal interfaces of telecommunication centres to surge overvoltages

[11] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

[12] Telcordia GR-499-CORE, Issue 2 (12/1998)
Transport Systems Generic Requirements (TSGR) Common requirements

[13] Telcordia GR-1244-CORE, Issue 2 (12/2000)
Clocks for the Synchronized Network: Common Generic Criteria

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Notes

Revision Status/History

The Revision Status of the datasheet, as shown in the center of the datasheet header bar, may be DRAFT, PRELIMINARY, or FINAL, and refers to the status of the Device (not the datasheet) within the design cycle. DRAFT status is used when the design is being realized but is not yet physically available, and the datasheet content reflects the intention of the design. The datasheet is raised to PRELIMINARY status when initial prototype devices are physically available, and the datasheet content more accurately represents the realization of the design. The datasheet is only raised to FINAL status after the device has been fully characterized, and the datasheet content updated with measured, rather than simulated parameter values.

This is a FINAL release (Revision 4.01) of the ACS8527 datasheet. Changes made for this document revision are given in Table 16, together with a summary of previous revisions. For specific changes between earlier revisions, refer (where available) to those earlier revisions. Always use the current version of the datasheet.

Table 16 Revision History

Revision	Reference	Description of changes
2.00/ December 2002	All pages	First full release.
3.00/April 2003	All pages	Major revision. First Release at FINAL status.
4.00/September 2003	All pages	Major revision. All pages reformatted. General update of cross-references.
	Table 3, Table 5, Table 6, Table 11, Table 12 and Figure 5.	Tables and Figures updated.
	“Fast Activity Monitor” on page 8, “Status Reporting” on page 9, “Revision Status/History” on page 21.	Sections updated.
	“ESD Protection” on page 10, “Latchup Protection” on page 10.	New Sections inserted.
4.01/June 2006	Front and back pages and “Abbreviations” on page 19.	Interim update to reflect availability of lead(Pb)-free packaged part and change to Semtech US address.
	“Trademark Acknowledgements” on page 20 and “Revision Status/History” on page 21.	Minor non-technical changes.
	Back page	Taiwan address changed
	“Over-voltage Protection” on page 10	Hyperlink to Semtech website added.
	Figure 6, Figure 7.	Updated Package diagram and footprint diagram. Former Tables 16 and 17 removed.

Ordering Information

Table 17 Parts List

Part Number	Description
ACS8527	MUXPLL Line Card Protection Switch for PDH, SONET or SDH Systems
ACS8527T	Lead (Pb)-free package version of ACS8527; RoHS and WEEE compliant.

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Right to change- Semtech Corporation reserves the right to make changes, without notice, to this product. Customers are advised to obtain the latest version of the relevant information before placing orders.

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