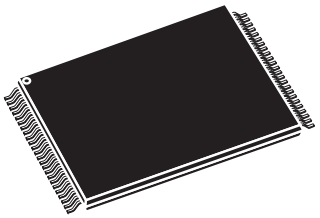
NAND04G-B2D, NAND08G-BxC

4 Gbit, 8 Gbit, 2112 byte/1056 word page multiplane architecture, 1.8 V or 3 V, NAND Flash memories

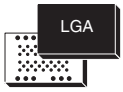
Preliminary Data

Features

- High density NAND Flash Memory
  - Up to 8 Gbit memory array
  - Cost-effective solution for mass storage applications
- NAND interface
  - x8 or 16x bus width
  - Multiplexed address/data
- Supply voltage: 1.8 V or 3.0 V device
- Page size
  - x8 device: (2048 + 64 spare) bytes
  - x16 device: (1024 + 32 spare) words
- Block size
  - x8 device: (128K + 4 K spare) bytes
  - x16 device: (64K + 2 K spare) words
- Multiplane architecture
  - Array split into two independent planes
  - Program/erase operations can be performed on both planes at the same time
- Page read/program
  - Random access: 25 µs (max)
  - Sequential access: 25 ns (min)
  - Page program time: 200 µs (typ)
  - Multiplane page program time (2 pages): 200 µs (typ)
- Copy back program with automatic error detection code (EDC)
- Cache read mode
- Fast block erase
  - Block erase time: 1.5 ms (typ)
  - Multiblock erase time (2 blocks): 1.5 ms (typ)
- Status Register
- Electronic signature
- Chip Enable 'don't care'
- Serial number option



TSOP48 12 x 20 mm (N)



LGA52 12 x 17 mm (ZL)

- Data protection:
  - Hardware program/erase disabled during power transitions
  - Non-volatile protection option
- ONFI 1.0 compliant command set
- Data integrity
  - 100 000 program/erase cycles (with ECC (error correction code))
  - 10 years data retention
- ECOPACK® packages

Table 1. Device Summary

Reference	Part number
NAND04G-B2D	NAND04GR3B2D
	NAND04GW3B2D
	NAND04GR4B2D(1)
	NAND04GW4B2D(1)
NAND08G-BxC	NAND08GR3B2C,
	NAND08GW3B2C
	NAND08GR4B2C(1)
	NAND08GW4B2C(1)
	NAND08GR3B4C
	NAND08GW3B4C

1. x16 organization only available for MCP products.

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1 Description

The NAND04G-B2D and NAND08G-BxC are part of the NAND Flash 2112 byte/1056 word page family of non-volatile Flash memories. They use NAND cell technology have a density of 4 Gbits and 8 Gbits, respectively.

The NAND04G-B2D memory array is split into 2 planes of 2048 blocks each. This multiplane architecture makes it possible to program 2 pages at a time (one in each plane), or to erase 2 blocks at a time (one in each plane). This feature reduces the average program and erase times by 50%.

The NAND08G-BxC is a stacked device that combines two NAND04G-B2D dice, both of which feature a multiplane architecture.

In the NAND08G-B2C devices, only one of the memory components can be enabled at a time, therefore, operations can only be performed on one of the memory components at any one time.

In the NAND08G-B4C devices, each NAND04G-B2D die can be accessed independently using two sets of signals.

The devices operate from a 1.8 V or 3 V voltage supply. Depending on whether the device has a x8 or x16 bus width, the page size is 2112 bytes (2048 + 64 spare) or or 1056 words (1024 + 32 spare), respectively.

The address lines are multiplexed with the data input/output signals on a multiplexed x8 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100 000 cycles with ECC (error correction code) on. To extend the lifetime of NAND Flash devices, the implementation of an ECC is strongly recommended.

A Write Protect pin is available to provide hardware protection against program and erase operations.

The devices feature an open-drain ready/busy output that identifies if the P/E/R (program/erase/read) Controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to connect to a single pull-up resistor.

A Copy Back Program command is available to optimize the management of defective blocks. When a page program operation fails, the data can be programmed in another page without having to resend the data to be programmed. An embedded error detection code is automatically executed after each copy back operation: 1 error bit can be detected for every 528 bits. With this feature it is no longer necessary, nor recommended, to use an external 2-bit ECC to detect copy back operation errors.

The devices have a cache read feature that improves the read throughput for large files. During cache reading, the device loads the data in a Cache Register while the previous data is transferred to the I/O buffers to be read.

The devices have the Chip Enable ‘don’t care’ feature, which allows code to be directly downloaded by a microcontroller. This is possible because Chip Enable transitions during the latency time do not stop the read operation.

Both the NAND04G-B2D and NAND08G-BxC support the ONFI 1.0 specification.

Two further features are available as options:

- Extra non-volatile protection.
- An individual serial number that acts as an unique identifier.

More information is available, upon completion of an NDA (non-disclosure agreement), and therefore, the details are not described in this datasheet. For more information on these two options, contact your nearest Numonyx Sales office.

The devices are available in the TSOP48 (12 x 20 mm) and LGA52 (12 x 17 mm) packages. To meet environmental requirements, Numonyx offers the NAND04G-B2D and NAND08G-BxC in ECOPACK® packages.

For information on how to order these options, refer to *Table 34: Ordering information scheme*. Devices are shipped from the factory with block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

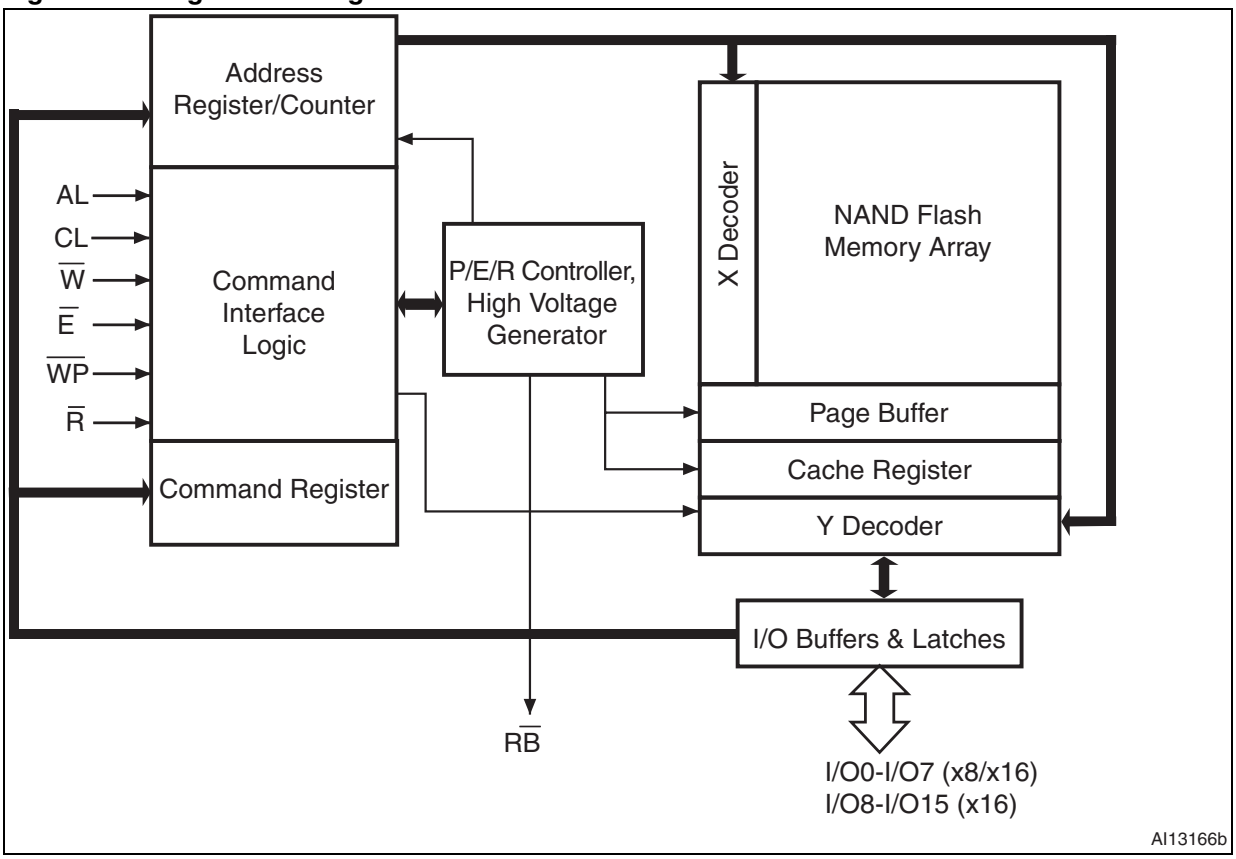
Table 2: Product description lists the part numbers and other information for all the devices able in the family.

Table 2. Product description

Part Number	Density	Bus width	Page size	Block size	Memory array	Operating voltage	Timings				Package
							Sequential access time (min)	Random access time (max)	Page Program (typ)	Block Erase (typ)	
NAND04GR3B2D	4 Gb	x8	2048+64 bytes	128 K+ 4 K bytes	64 pages x 4096 blocks	1.7 to 1.95 V	45 ns	25 µs	200 µs	1.5ms	LGA52
NAND04GW3B2D						2.7 to 3.6 V	25 ns				TSOP48 LGA52
NAND04GR4B2D		x16	1024+ 32 words	64 K + 2 K words		1.7 to 1.95 V	45 ns				(1)
NAND04GW4B2D						2.7 to 3.6 V	25 ns				
NAND08GR3B2C	8 Gb	x8	2048+64 bytes	128 K + 4 K bytes	64 pages x 8192 blocks	1.7 to 1.95 V	45 ns	25 µs	200 µs	1.5ms	LGA52(2)
NAND08GW3B2C						2.7 to 3.6 V	25 ns				TSOP48 LGA52(2)
NAND08GR4B2C		x16	1024+ 32 words	64 K + 2 K words		1.7 to 1.95 V	45 ns				(1)(2)
NAND08GW4B2C						2.7 to 3.6 V	25 ns				
NAND08GR3B4C		x8	2048+64 bytes	128 K + 4 K bytes		1.7 to 1.95 V	45 ns				LGA52(2)
NAND08GW3B4C		x8				2.7 to 3.6 V	25 ns				

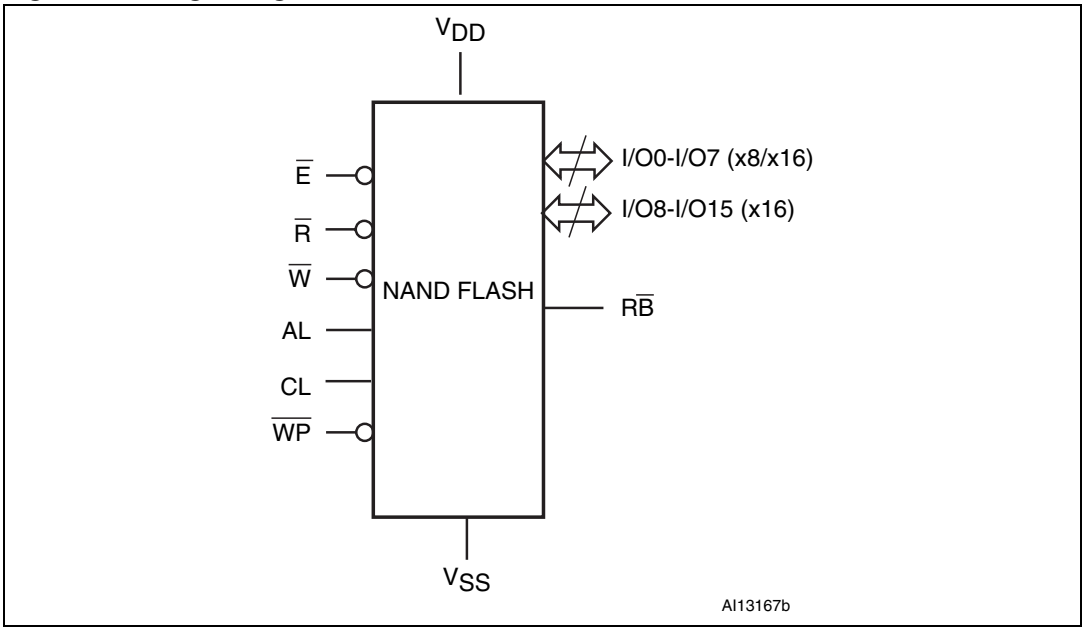
1. x16 organization is only available for MCP products.
2. The NAND08G-BxC is composed of two 4-Gbit dice.

Figure 1. Logic block diagram



1. The NAND08G-B4C devices have two separate sets of signals for each 4 Gb die.

Figure 2. Logic diagram



1. The NAND08G-B4C devices have two separate sets of signals for each 4 Gb die.

Table 3. Signal names(1)

Signal	Function	Direction
I/O0-7	Data input/outputs, address inputs, or command inputs (x8/x16 devices)	Input/output
I/O8-15	Data input/outputs (x16 devices)	Input/output
AL	Address Latch Enable	Input
CL	Command Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$R\overline{B}$	Ready/Busy (open-drain output)	Output
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
V_{DD}	Supply Voltage	Power supply
V_{SS}	Ground	Ground
NC	Not connected internally	N/A
DU	Do not use	N/A

1. The NAND08G-B4C devices have two separate sets of signals for each 4 Gb die.

Figure 3. TSOP48 connections for NAND04G-B2D and NAND08G-BxC

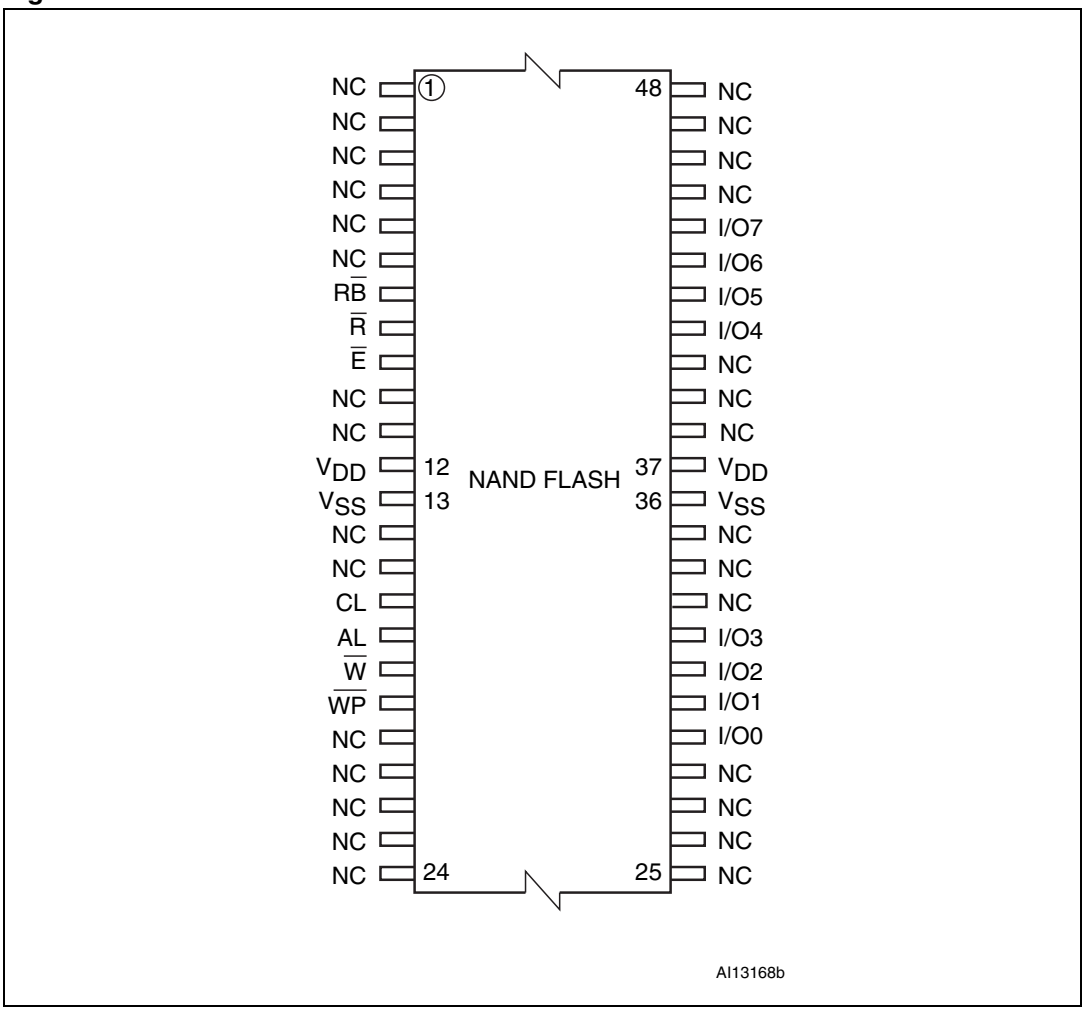


Figure 4. LGA52 connections for NAND04G-B2D and NAND08G-B2C devices

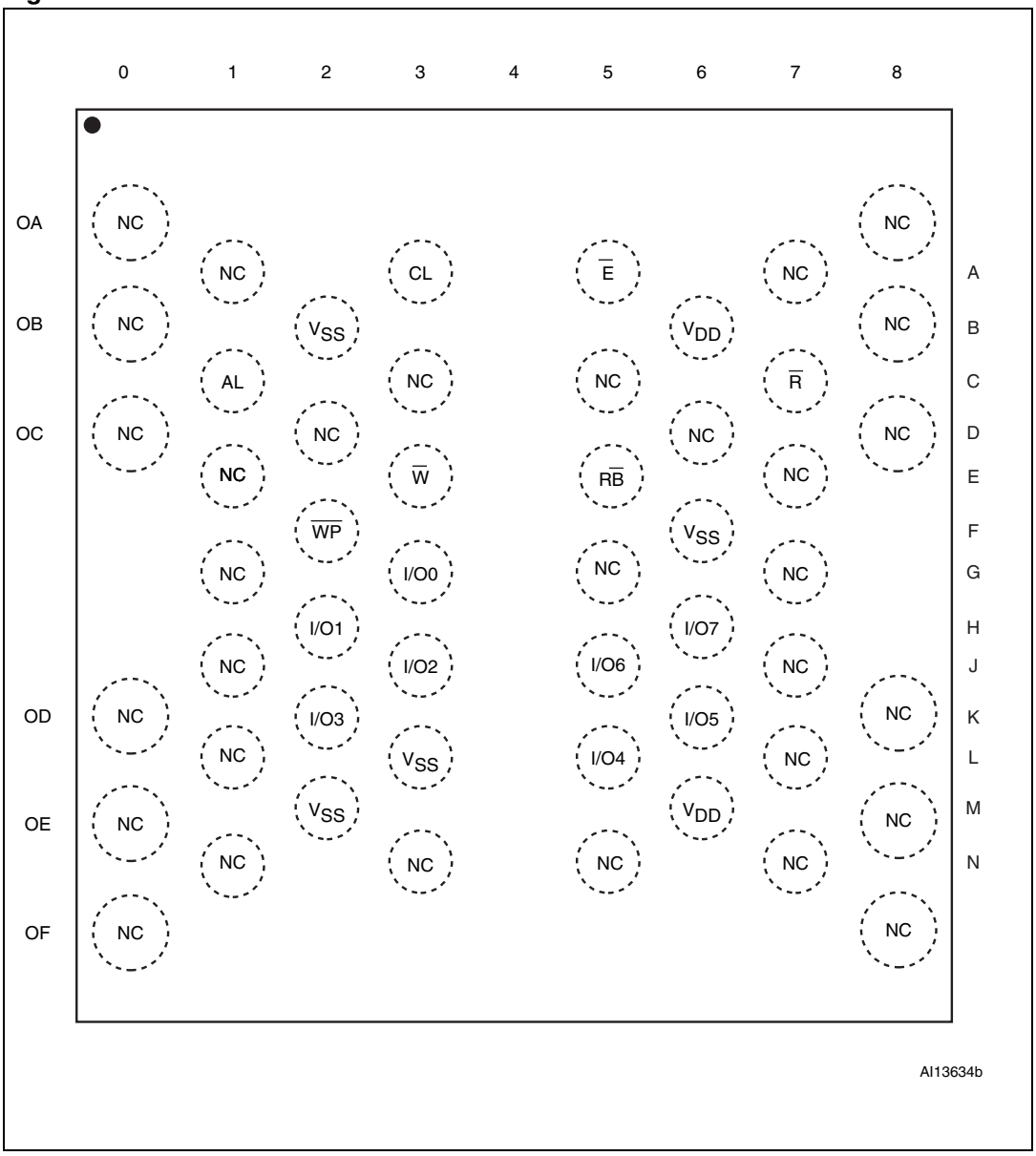
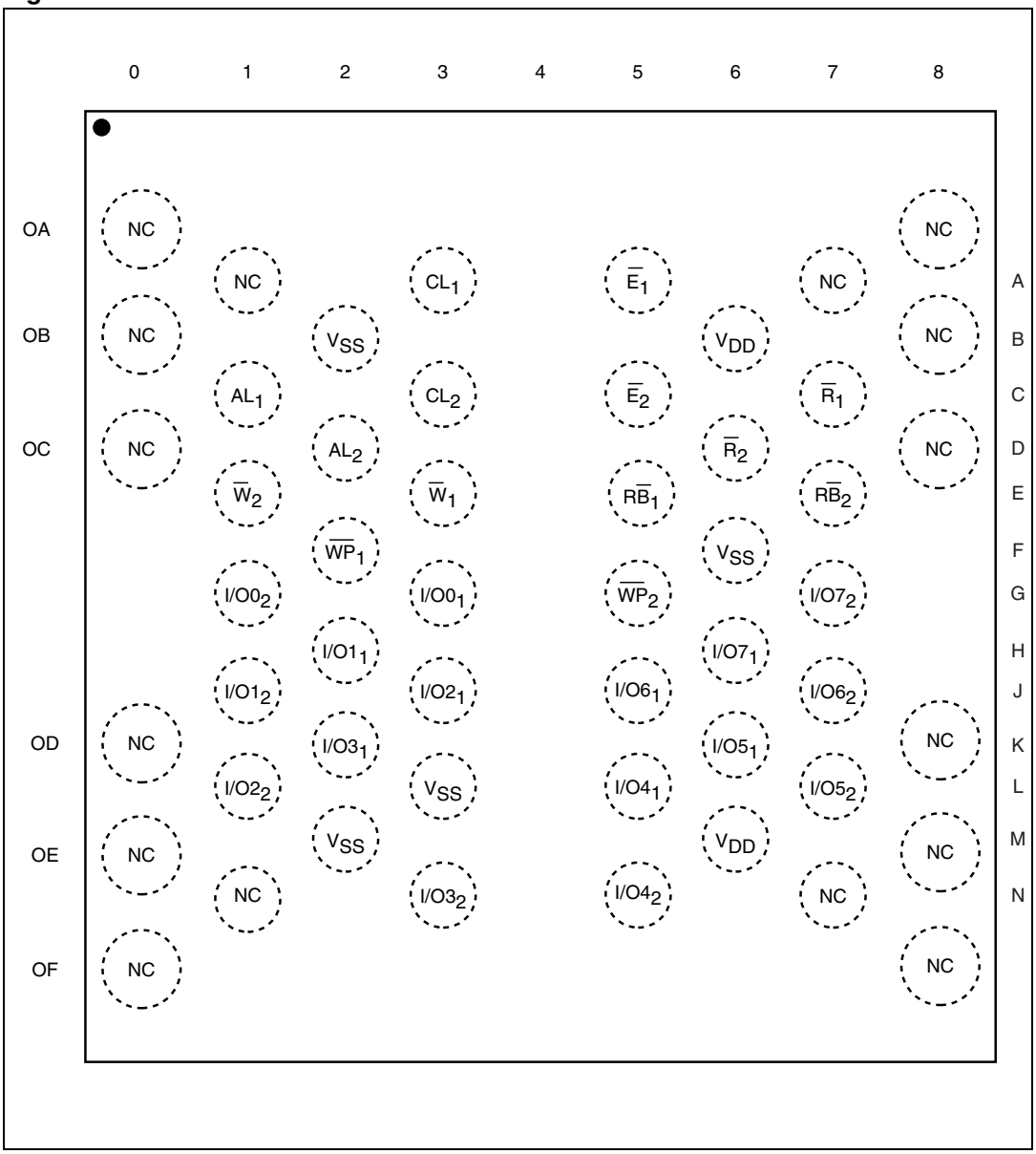


Figure 5. LGA52 connections for the NAND08G-B4C devices



1. The NAND08G-B4C devices have two separate sets of signals for each 4 Gb die.

2 Memory array organization

The memory array of the devices is made up of NAND structures where 32 cells are connected in series. It is organized into blocks where each block contains 64 pages. The array is split into two areas, the main area, and the spare area. The main area of the array is used to store data, and the spare area typically stores error correction codes, software flags, or bad block identification.

In x8 devices, the pages are split into a 2048-byte main area and a spare area of 64 bytes. In x16 devices, the pages are split into a 1024-word main area and a spare area of 32 words. Refer to *Figure 6: Memory array organization*.

Bad blocks

In the x8 devices, the NAND Flash 2112 byte/1056 word page devices may contain bad blocks, which are blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block information is written prior to shipping (refer to *Section 9.1: Bad block management* for more details).

Table 4 shows the minimum number of valid blocks. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on. Block 0 is guaranteed to be valid up to 1000 write/erase cycles with 1 bit ECC.

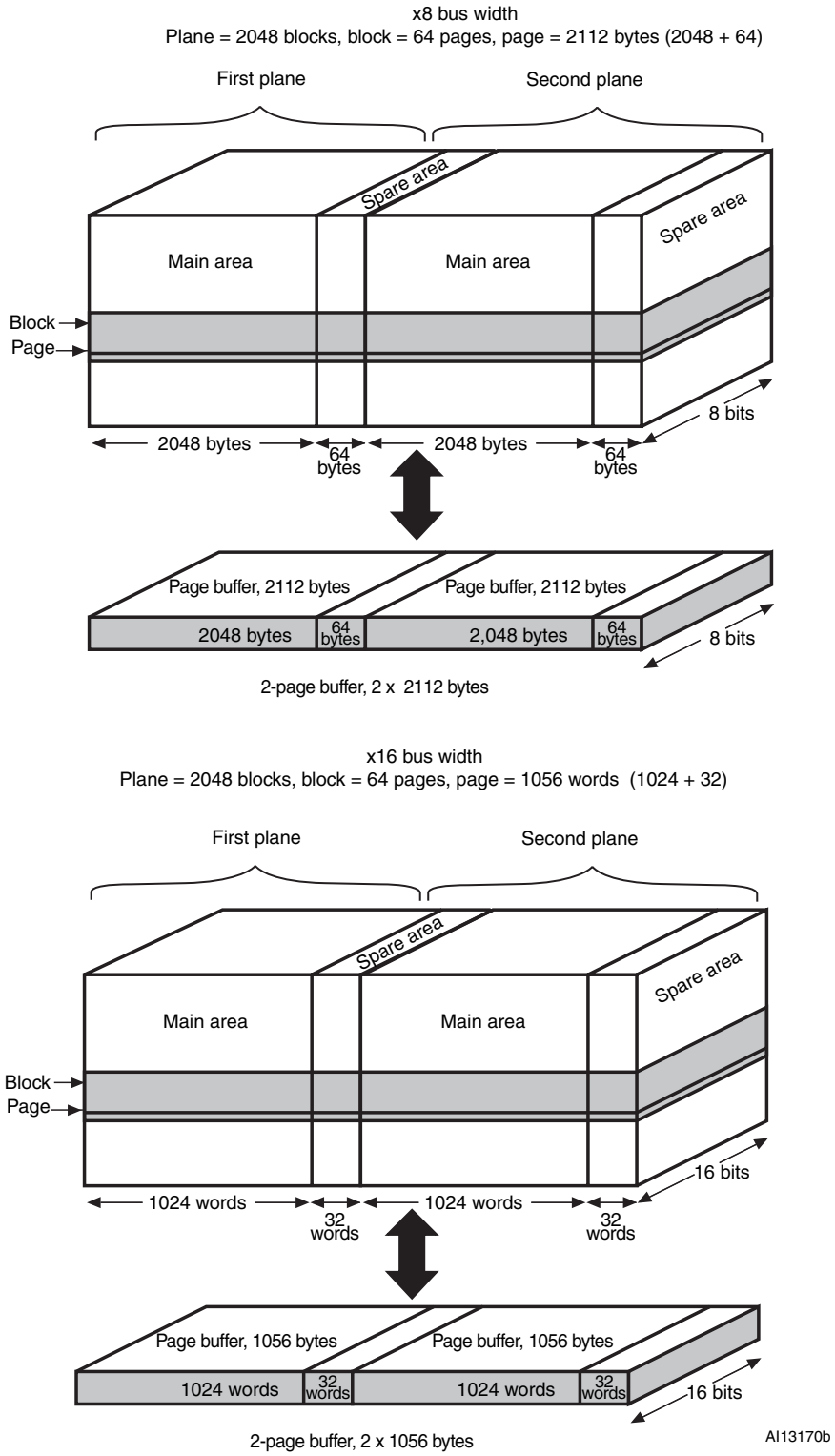
These blocks need to be managed using bad blocks management, block replacement, or error correction codes (refer to *Section 9: Software algorithms*).

Table 4. Valid Blocks

Density of Device	Min	Max
4 Gbits	4016	4096
8 Gbits(1)	8032	8192

1. The NAND08G-BxC devices are composed of two 4-Gbit dice. The minimum number of valid blocks is 4016 for each die.

Figure 6. Memory array organization



3 Signal descriptions

See *Figure 2: Logic diagram* and *Table 3: Signal names* for a brief overview of the signals connected to this device. The NAND08G-B4C devices have two separate sets of signals for each 4 Gb die.

3.1 Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 input the selected address, output the data during a read operation, or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Inputs/Outputs (I/O8-I/O15)

Input/Outputs 8 to 15 are only available in x16 devices. They output the data during a read operation or input data during a write operation. Command and address inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

3.3 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the Command Interface. When AL is high, the inputs are latched on the rising edge of Write Enable.

3.4 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the Command Interface. When CL is high, the inputs are latched on the rising edge of Write Enable.

3.5 Chip Enable ($\overline{E}$)

The Chip Enable input, $\overline{E}$, activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is low, V_{IL}, the device is selected. If Chip Enable goes high, V_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.6 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the Command Interface, input address and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 µs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

3.8 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.9 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that identifies if the P/E/R Controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes, Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the ready/busy pins from several memories to be connected to a single pull-up resistor. A Low then indicates that one or more of the memories is busy.

During power-up and power-down a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. During this period the $R\overline{B}$ signal is Low, V_{OL}.

Refer to *Section 12.1: Ready/Busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.10 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} (see *Table 29*) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

3.11 V_{SS} ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory, as described in this section. See *Table 5: Bus operations* for a summary of these operations.

Typically, glitches of less than 5 ns on Chip Enable, Write Enable, and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command input

Command input bus operations give commands to the memory.

Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low, and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 25* and *Table 30* for details of the timings requirements.

4.2 Address input

Address input bus operations input the memory addresses. Five bus cycles are required to input the addresses (refer to *Table 6: Address insertion (x8 devices)* and *Table 7: Address insertion (x16 devices)*).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low, and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input addresses.

See *Figure 26* and *Table 30* for details of the timings requirements.

4.3 Data input

Data input bus operations input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low, and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 27* and *Table 30* and *Table 31* for details of the timings requirements.

4.4 Data output

Data output bus operations read the data in the memory array, the Status Register, the electronic signature, and the unique identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

If the Read Enable pulse frequency is lower then 33 MHz (t_{RLRL} higher than 30 ns), the output data is latched on the rising edge of Read Enable signal (see *Figure 28*).

For higher frequencies (t_{RLRL} lower than 30 ns), the EDO (extended data out) mode must be used. In this mode, data output bus operations are valid on the input/output bus for a time of t_{RLQX} after the falling edge of Read Enable signal (see *Figure 29*).

See *Table 31* for details on the timings requirements.

4.5 Write protect

Write protect bus operations protect the memory against program or erase operations. When the Write Protect signal is Low the device does not accept program or erase operations, and, therefore, the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection, even during power-up.

4.6 Standby

When Chip Enable is High the memory enters Standby mode, the device is deselected, outputs are disabled, and power consumption is reduced.

Table 5. Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7	I/O8 - I/O15(1)
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data input	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output	Data output
Write protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X	X

1. Only for x16 devices.
2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 6. Address insertion (x8 devices)

Bus Cycle(1)	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A11	A10	A9	A8
3rd	A19	A18	A17	A16	A15	A14	A13	A12
4th	A27	A26	A25	A24	A23	A22	A21	A20
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A30(2)	A29	A28

1. Any additional address input cycles are ignored.
2. A30 is only valid for the NAND08G-BxC devices.

Table 7. Address insertion (x16 devices)

Bus Cycle(1)	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A10	A9	A8
3rd	A18	A17	A16	A15	A14	A13	A12	A11
4th	A26	A25	A24	A23	A22	A21	A20	A19
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A29(2)	A28	A27

1. Any additional address input cycles are ignored.
2. A29 is only valid for the NAND08G-BxC devices.

Table 8. Address definition (x8 devices)

Address	Definition
A0 - A11	Column address
A12 - A17	Page address
A18 - A29	Block address(NAND04G-B2D)
A18 - A30	Block address (NAND08G-BxC)
A18 = 0	First plane
A18 = 1	Second plane

Table 9. Address definition (x16 devices)

Address	Definition
A0 - A10	Column address
A11 - A16	Page address
A17 - A28	Block address (NAND04G-B2D)
A17 - A29	Block address (NAND08G-BxC)
A18 = 0	First plane
A18 = 1	Second plane

5 Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the command Latch Enable signal is high. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for program and erase operations are imposed to maximize data security.

Table 10 summarizes the commands.

Table 10. Commands

Command[1]	Bus write operations				Commands accepted during busy
	1st cycle	2nd cycle	3rd cycle	4th cycle	
Read	00h	30h	–	–	
Random Data Output	05h	E0h	–	–	
Cache Read (sequential)	**31h**	**–**	**–**	**–**	
Enhanced Cache Read (random)	**00h**	**31h**	**–**	**–**	
Exit Cache Read	**3Fh**	**–**	**–**	**–**	**Yes[2]**
Page Program (sequential input default)	80h	10h	–	–	
Random Data Input	85h	–	–	–	
Multiplane Page Program[3]	80h	11h	81h	10h	
Multiplane Page Program	**80h**	**11h**	**80h**	**10h**	
Copy Back Read	00h	35h	–	–	
Copy Back Program	85h	10h	–	–	
Multiplane Copy Back Program[3]	85h	11h	81h	10h	
Multiplane Copy Back Program	**85h**	**11h**	**85h**	**10h**	
Block Erase	60h	D0h	–	–	
Multiplane Block Erase[3]	60h	60h	D0h	–	
Multiplane Block Erase	**60h**	**D1h**	**60h**	**D0h**	
Reset	FFh	–	–	–	Yes
Read Electronic Signature	90h	–	–	–	
Read Status Register	70h	–	–	–	Yes
Read Status Enhanced	**78h**	**–**	**–**	**–**	**Yes**
Read Parameter Page	**ECh**	**–**	**–**	**–**	
Read EDC Status Register	7Bh	–	–	–	

1. Commands in bold are referring to ONFI 1.0 specifications.
2. Only during cache read busy.
3. Command maintained for backward compatibility.

6 Device operations

This section provides details of the device operations.

6.1 Read memory array

At power-up the device defaults to read mode. To enter read mode from another mode, the Read command must be issued (see *Table 10: Commands*).

6.1.1 Random read

Each time the Read command is issued, the first read is random read.

6.1.2 Page read

After the first random read access, the page data (2112 bytes or 1056 words) are transferred to the page buffer in a time of t_{WHBH} (see *Table 31*). Once the transfer is complete, the Ready/Busy signal goes High. The data can then be read sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

The device can output random data in a page, instead of consecutive sequential data, by issuing a Random Data Output command. The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command. The Random Data Output command can be issued as many times as required within a page.

The Random Data Output command is not accepted during cache read operations.

Figure 7. Read operations

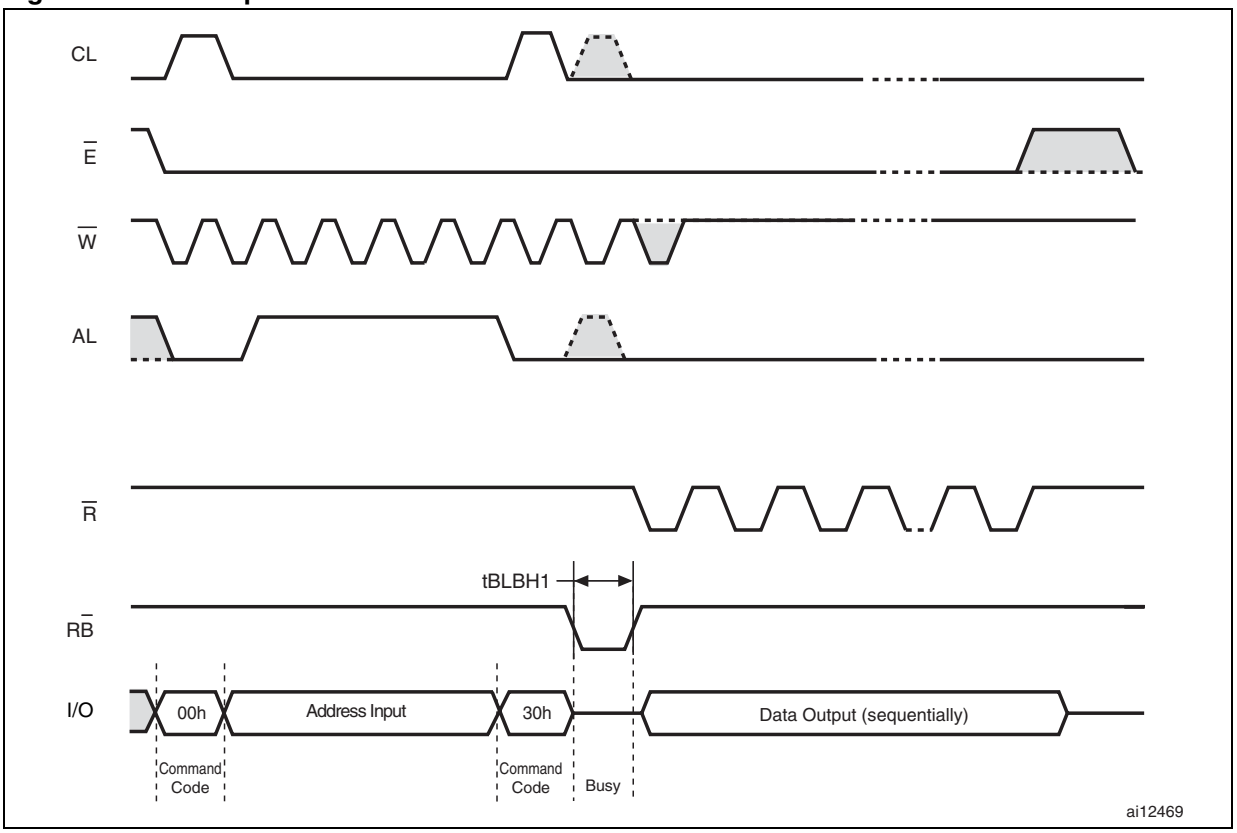
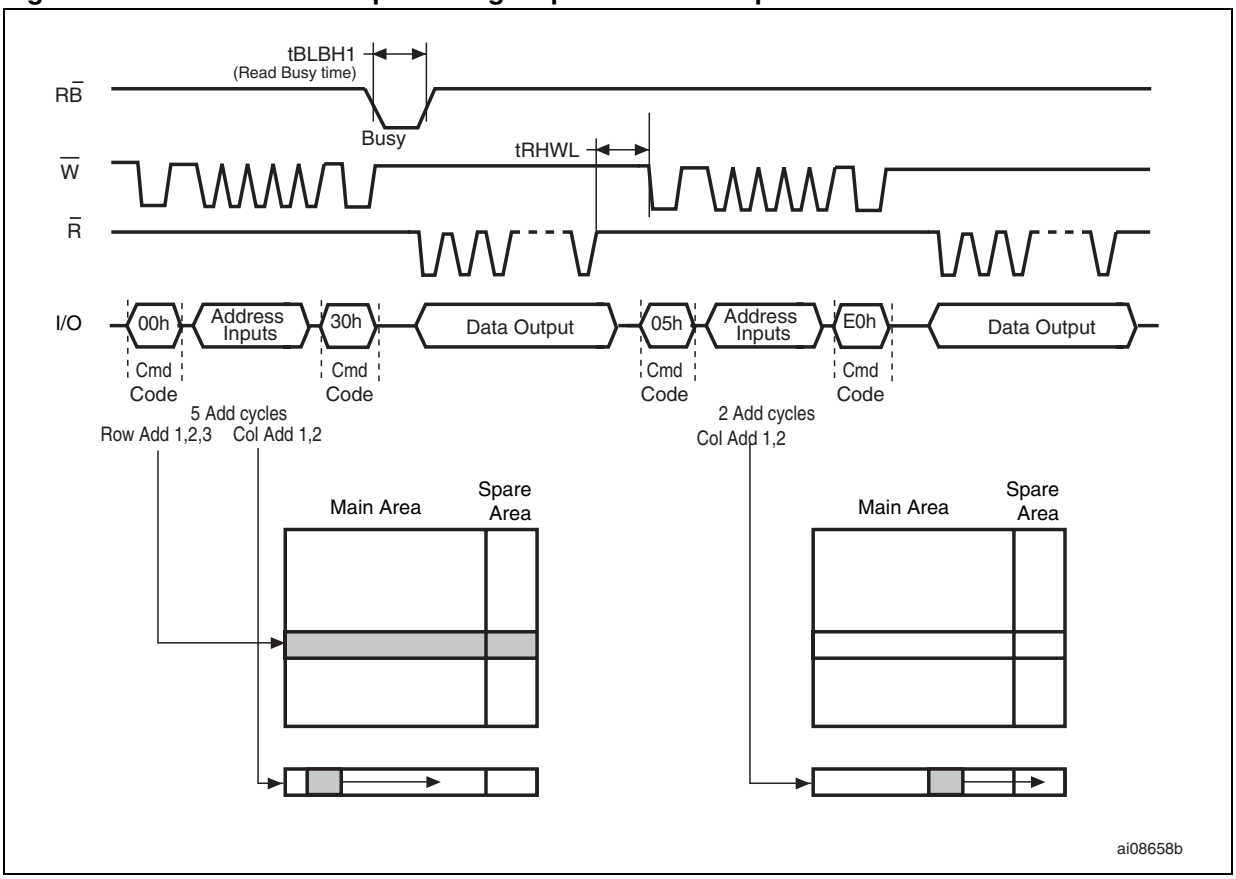


Figure 8. Random data output during sequential data output



6.2 Cache read

The cache read operation improves the read throughput by reading data using the Cache Register. As soon as the user starts to read one page, the device automatically loads the next page into the Cache Register.

A Read Page command, as defined in *Section 6.1.1: Random read*, is issued prior to the first Read Cache command in a read cache sequence. Once the data output of the Page Read command terminates, the Cache Read command can be issued as follows:

1. Issue a Sequential Cache Read command to copy the next page in sequential order to the Cache Register.
2. Issue a Random Cache Read command to copy the page addressed in this command to the Cache Register.

The two commands can be used interchangeably, in any order. When there are no more pages are to be read, the final page is copied into the Cache Register by issuing the Exit Cache Read command. A Read Cache Command must not be issued after the last page of the device is read.

See *Figure 9: Cache read (sequential) operation* and *Figure 10: Cache read (random) operation* for examples of the two sequences.

After the Sequential Cache Read or Random Cache Read command has been issued, the Ready/Busy signal goes Low and the Status Register bits are set to SR5 =' 0' and SR6 ='0' for a period of Cache Read busy time, t_{RCBSY}, while the device copies the next page into the Cache Register.

After the cache read busy time has passed, the Ready/Busy signal goes High and the Status Register bits are set to SR5 = '0' and SR6 = '1', signifying that the Cache Register is ready to download new data. Data of the previously read page can be output from the page buffer by toggling the Read Enable signal. Data output always begins at column address 00h, but the Random Data Output command is also supported.

Figure 9. Cache read (sequential) operation

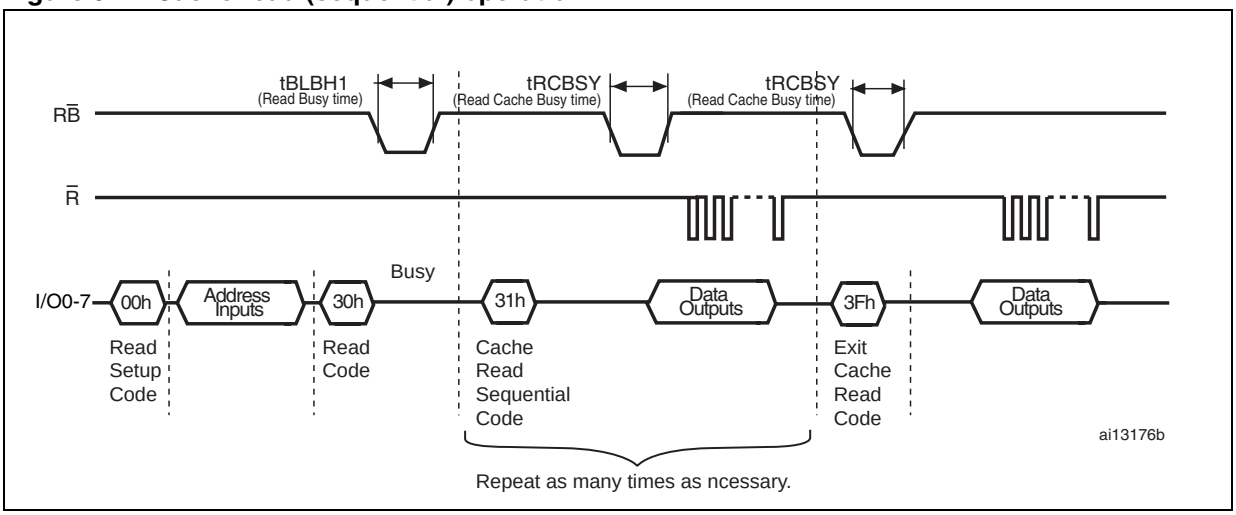
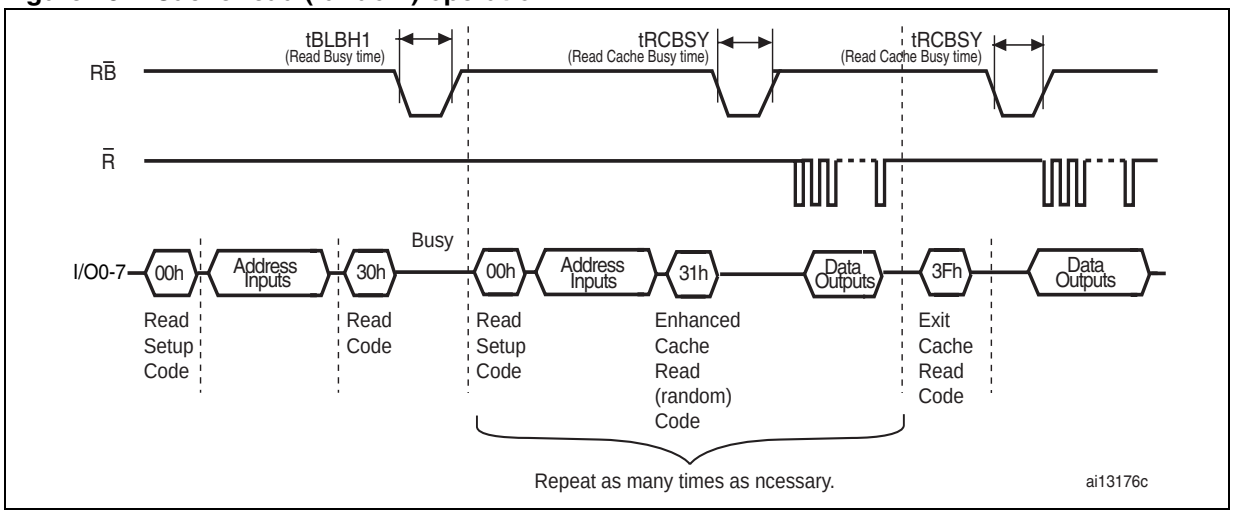


Figure 10. Cache read (random) operation



6.3 Page program

The page program operation is the standard operation to program data to the memory array. Generally, the page is programmed sequentially, however, the device does support random input within a page.

It is recommended to address pages sequentially within a given block.

The memory array is programmed by page, however, partial page programming is allowed where any number of bytes (1 to 2112) or words (1 to 1056) can be programmed.

The maximum number of consecutive, partial-page program operations allowed in the same page is four. After exceeding four operations a Block Erase command must be issued before any further program operations can take place in that page.

6.3.1 Sequential input

To input data sequentially the addresses must be sequential and remain in one block.

For sequential input each page program operation consists of the following five steps :

1. One bus cycle is required to set up the Page Program (sequential input) command (see *Table 10: Commands*).
2. Five bus cycles are then required to input the program address (refer to *Table 6: Address insertion (x8 devices)* and *Table 7: Address insertion (x16 devices)*).
3. The data is then loaded into the Data Registers.
4. One bus cycle is required to issue the Page Program Confirm command to start the P/E/R Controller. The P/E/R only starts if the data has been loaded in step *3.*
5. the P/E/R Controller then programs the data into the array.

See *Figure 11: Page program operation* for more information.

6.3.2 Random data input in page

During a sequential input operation, the next sequential address to be programmed can be replaced by a random address by issuing a Random Data Input command. The following two steps are required to issue the command:

1. One bus cycle is required to set up the Random Data Input command (see *Table 10: Commands*).
2. Two bus cycles are then required to input the new column address (refer to *Table 6: Address insertion (x8 devices)*).

Random data input can be repeated as often as required in any given page.

Once the program operation has started, the Status Register can be read using the Read Status Register command. During program operations the Status Register only flags errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored.

Once the program operation has completed, the P/E/R Controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High.

The device remains in Read Status Register mode until another valid command is written to the command interface.

Figure 11. Page program operation

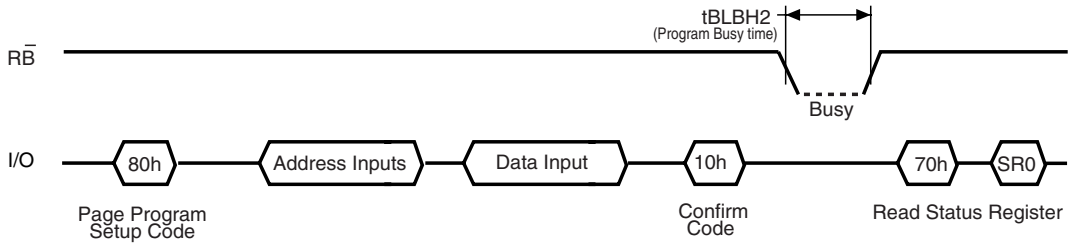
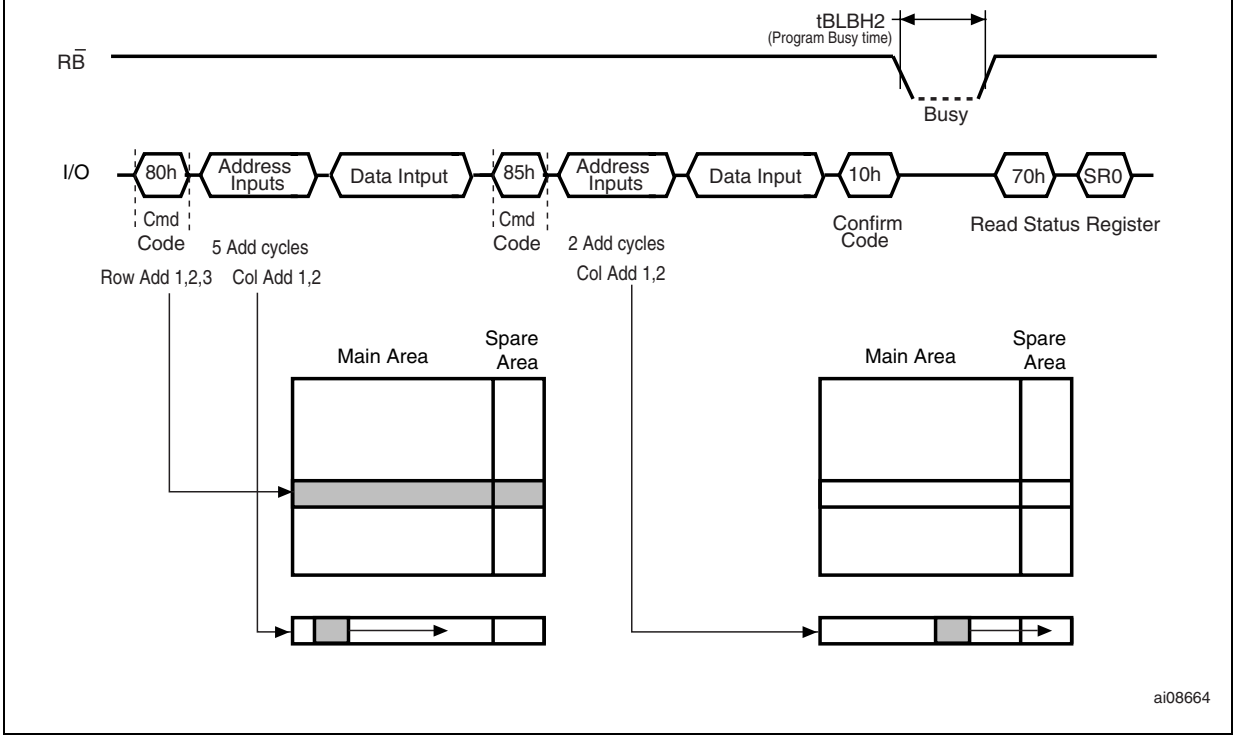


Figure 12. Random data input during sequential data input



6.4 Multiplane page program

The devices support multiplane page program, which enables the programming of two pages in parallel, one in each plane.

A multiplane page program operation requires the following two steps:

1. The first step serially loads up to two pages of data (4224 bytes) into the data buffer. It requires:
   - One clock cycle to set up the Page Program command (see *Section 6.3.1: Sequential input*).
   - 5 bus write cycles to input the first page address and data. The address of the first page must be within the first plane (A18 = 0).
   - One bus write cycle to issue the Page Program Confirm code. After this, the device is busy for a time of t_{IPBSY}.
   - When the device returns to the ready state (Ready/Busy High), a multiplane page program setup code must be issued, followed by the 2nd page address (5 write cycles) and data. The address of the 2nd page must be within the second plane (A18 = 1).
2. The 2nd step programs in parallel the two pages of data loaded into the data buffer into the appropriate memory pages. It is started by issuing a the Program Confirm command.

As for standard page program operation, the device supports random data input during both data loading phases.

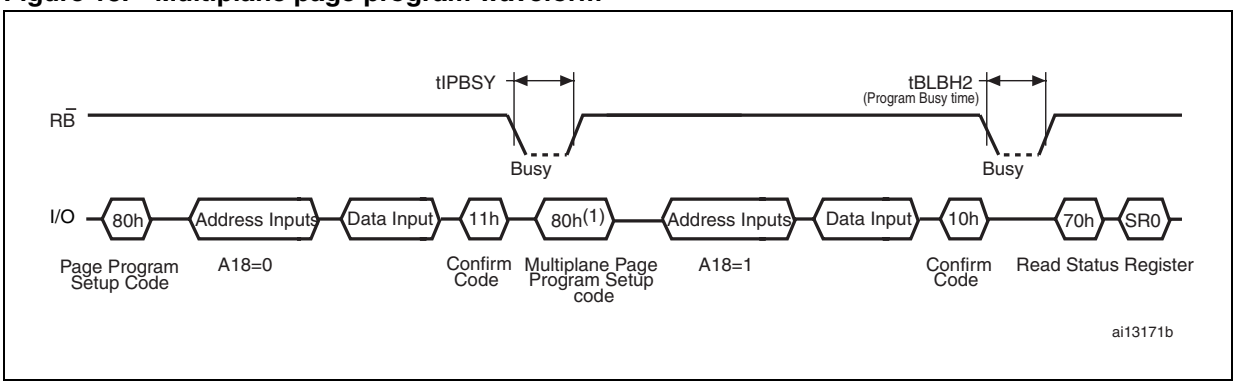
Once the multiplane page program operation has started, that is during a delay of t_{IPBSY}, the Status Register can be read using the Read Status Register command.

Once the multiplane page program operation has completed, the P/E/R Controller bit SR6 is set to '1' and the Ready/Busy signal goes High.

If the multiplane page program fails, an error is signaled on bit SR0 of the Status Register. To know which page of the two planes failed, the Read Status Enhanced command must be issued twice, once for each plane (see *Section 6.12*).

Figure 13 provides a description of multiplane page program waveforms.

Figure 13. Multiplane page program waveform



1. The 81h setup code is also accepted for backward compatibility.

6.5 Copy back program

The copy back program operation copies the data stored in one page and reprograms it in another page.

The copy back program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

The NAND04G-B2D and NAND08G-BxC devices feature automatic EDC during a copy back operation. Consequently, external ECC is no longer required. The errors detected during copy back operations can be read by performing a read EDC Status Register operation (see *Section 6.13: Read EDC Status Register*). See also *Section 6.9* for details of EDC operations.

The copy back program operation requires the following four steps:

1. The first step reads the source page. The operation copies all 2112 bytes from the page into the data buffer. It requires:
   - One bus write cycle to set up the command
   - 5 bus write cycles to input the source page address
   - One bus write cycle to issue the confirm command code
2. When the device returns to the ready state (Ready/Busy High), optional data readout is allowed by pulsing $\overline{R}$; the next bus write cycle of the command is given with the 5 bus cycles to input the target page address. See *Table 11* for the addresses that must be the same for the source and target page.
3. Issue the confirm command to start the P/E/R Controller.

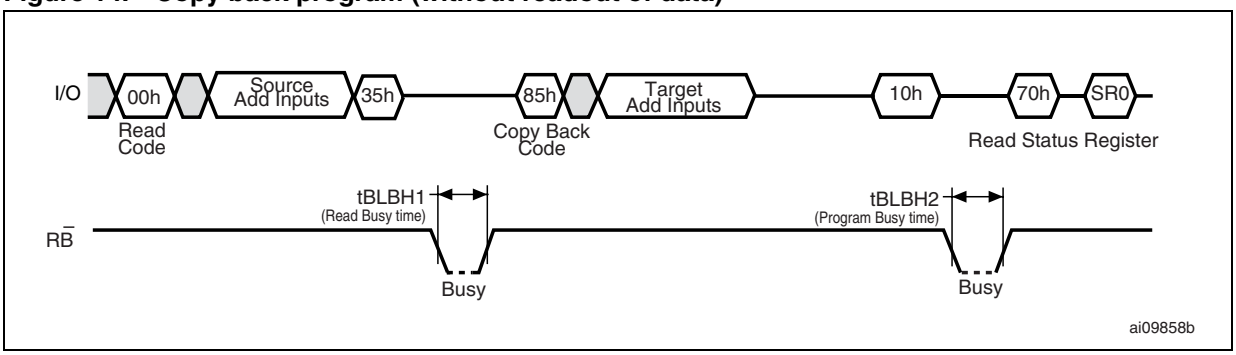
To see the data input cycle for modifying the source page and an example of the copy back program operation, refer to *Figure 14: Copy back program (without readout of data)*.

Figure 16: Page copy back program with random data input shows a data input cycle to modify a portion or a multiple distant portion of the source page.

Table 11. Copy back program addresses

Density	Source and target page addresses
4 Gbits	Same A18
8 Gbits	Same A18 and A30

Figure 14. Copy back program (without readout of data)



1. Copy back program is only permitted between odd address pages or even address pages.

Figure 15. Copy back program (with readout of data)

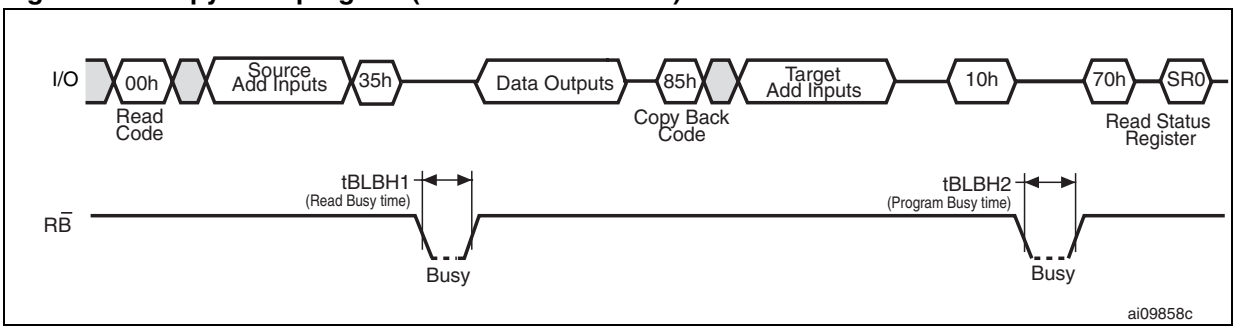
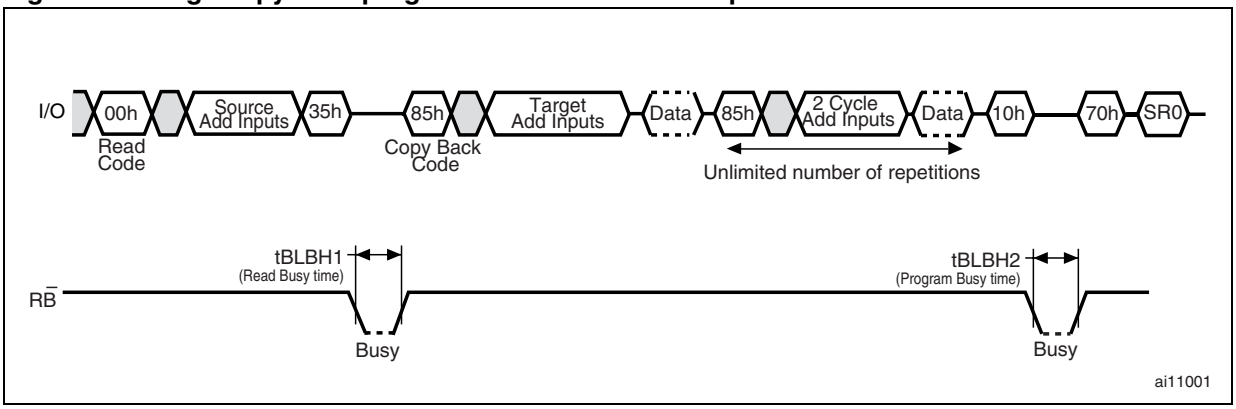


Figure 16. Page copy back program with random data input



6.6 Multiplane copy back program

In addition to multiplane page program, the NAND04G-B2D and NAND08G-BxC devices support multiplane copy back program.

A Multiplane Copy Back Program command requires exactly the same steps as a Multiplane Page Program command, and must satisfy the same time constraints (see *Section 6.4: Multiplane page program*).

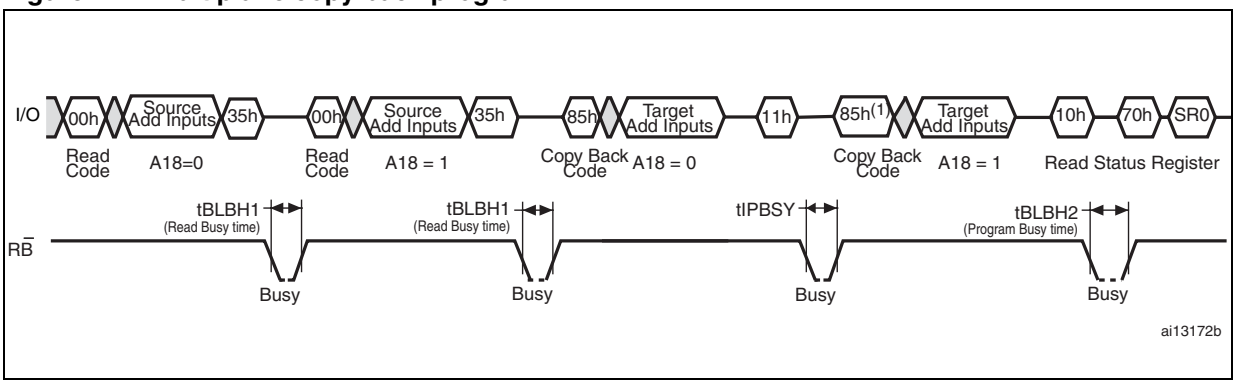
Prior to executing the multiplane copy back program operation, two single-page read operations must be executed to copy back the first page from the first plane and the second page from the second plane.

The EDC check is also performed during the multiplane copy back program. Errors during multiplane copy back operations can be detected by performing a Read EDC Status Register operation (see *Section 6.13: Read EDC Status Register*).

If the multiplane copy back program fails, an error is signaled on bit SR0 of the Status Register. To know which page of the two planes failed, the Read Status Enhanced command must be executed twice, once for each plane (see *Section 6.12*).

Figure 17 provides a description of multiplane copy back program waveform.

Figure 17. Multiplane copy back program



1. The 81h setup code is also accepted for backward compatibility.

6.7 Block erase

Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to ‘1’. All previous data in the block is lost.

An erase operation consists of the following three steps (refer to *Figure 18: Block erase*):

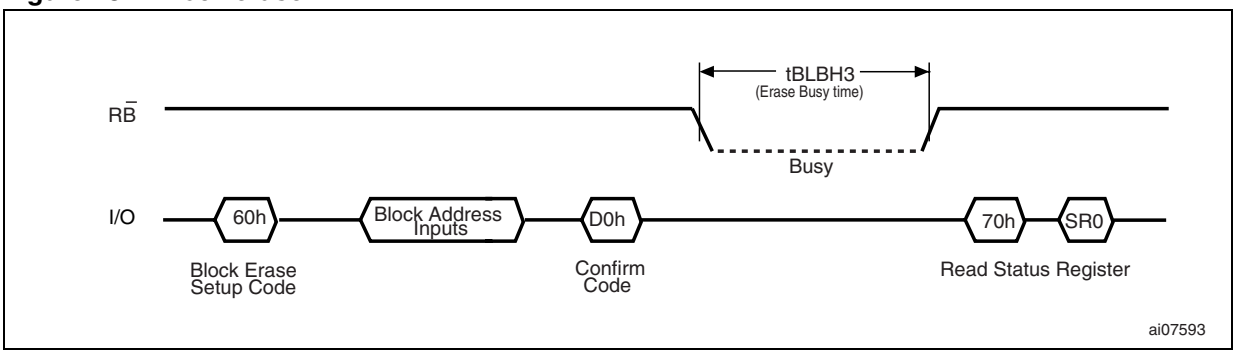
1. One bus cycle is required to set up the Block Erase command. Only addresses A18-A29 are used; all other address inputs are ignored.
2. Three bus cycles are then required to load the address of the block to be erased. Refer to *Table 8: Address definition (x8 devices)* for the block addresses of each device.
3. One bus cycle is required to issue the Block Erase Confirm command to start the P/E/R Controller.

The operation is initiated on the rising edge of Write Enable, $\overline{W}$, after the Confirm command is issued. The P/E/R Controller handles block erase and implements the verify process.

During the block erase operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored.

Once the program operation has completed, the P/E/R Controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High. If the operation completed successfully, the Write Status bit SR0 is ‘0’, otherwise it is set to ‘1’.

Figure 18. Block erase



6.8 Multiplane block erase

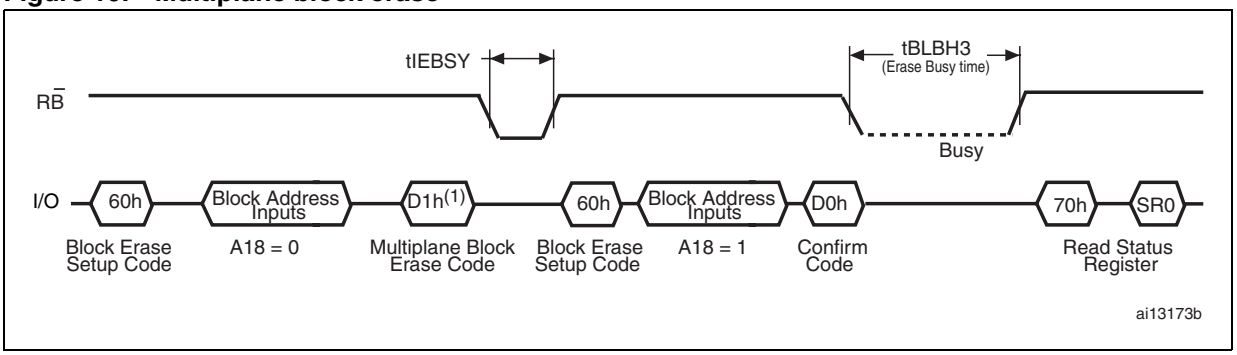
The multiplane block erase operation allows the erasure of two blocks in parallel, one in each plane.

This operation consists of the following three steps (refer to *Figure 19: Multiplane block erase*):

1. 8 bus cycles are required to set up the Block Erase command and load the addresses of the blocks to be erased. The setup command followed by the address of the block to be erased must be issued for each block. t_{IEBSY} busy time is required between the insertion of first and the second block addresses. As for multiplane page program operations, the address of the first and second page must be within the first plane (A18 = 0) and second plane (A8 = 1), respectively.
2. One bus cycle is then required to issue the Multiplane Block Erase Confirm command and start the P/E/R Controller.

If the multiplane block erase fails, an error is signaled on bit SR0 of the Status Register. To know which page of the two planes failed, the Read Status Enhanced command must be issued twice, once for each plane (see *Section 6.12*).

Figure 19. Multiplane block erase



1. The D1h Confirm code is required by the ONFI 1.0 command set. To maintain backward compatibility, the D1h Confirm code can optionally be ignored, and then the tIEBSY Busy Time does not occur.

6.9 Error detection code (EDC)

The EDC (error detection code) is performed automatically during all program operations. It starts immediately after the device becomes busy.

The EDC detects 1 single bit error per EDC unit. Each EDC unit has a density of 528 bytes (or 264 words), split into 512 bytes of main area and 16 bytes of spare area (or 256 + 8 words). Refer to *Table 12* and *Figure 20* for EDC unit addresses definition.

To properly use the EDC, the following conditions apply:

- Page program operations must be performed on a whole page, or on whole EDC unit(s).
- The modification of the content of an EDC unit using a random data input before the copy back program, must be performed on the whole EDC unit. It can only be done once per EDC unit. Any partial modification of the EDC unit results in the corruption of the on-chip EDCs.

EDC results can be retrieved only during copy back program and multiplane copy back using the Read EDC Status Register command (see *Section 6.13*).

Figure 20. Page organization

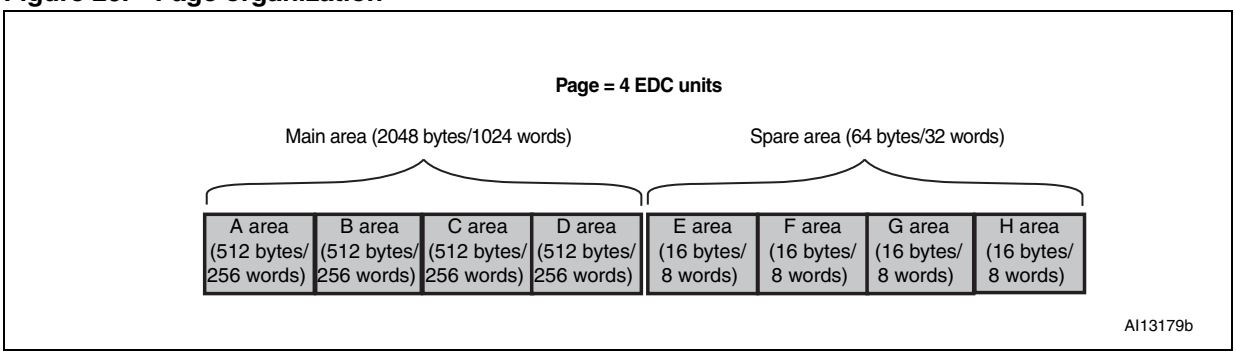


Table 12. Address definition for EDC units (x8 devices)

EDC unit	Main area		Spare area	
	Area name	Column address	Area name	Column address
1st 528-byte EDC unit	A	0 to 511	E	2048 to 2063
2nd 528-byte EDC unit	B	512 to 1023	F	2064 to 2079
3rd 528-byte EDC unit	C	1024 to1535	G	2080 to 2095
4th 528-byte EDC unit	D	1536 to 2047	H	2096 to 2111

Table 13. Address definition for EDC units (x16 devices)

EDC unit	Main area		Spare area	
	Area name	Column address	Area name	Column address
1st 264-word EDC unit	A	0 to 255	E	1024 to 1031
2nd 264-word EDC unit	B	256 to 511	F	1032 to 1039
3rd 264-word EDC unit	C	512 to 767	G	1040 to 1047
4th 264-word EDC unit	D	768 to 1023	H	1048 to 1055

6.10 Reset

The Reset command is used to reset the command interface and Status Register. If the Reset command is issued during any operation, the operation is aborted. If the aborted operation is a program or erase, the contents of the memory locations being modified are no longer valid as the data is partially programmed or erased.

If the device has already been reset, then the new Reset command is not accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued. Refer to *Table 31* for the values.

6.11 Read Status Register

The devices contain a Status Register that provides information on the current or previous program or erase operation. The various bits in the Status Register convey information and errors on the operation.

The Status Register is read by issuing the Read Status Register command. The Status Register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the Status Register.

After the Read Status Register command has been issued, the device remains in Read Status Register mode until another command is issued. Therefore, if a Read Status Register command is issued during a Random Read cycle, a new Read command must be issued to continue with a page read operation.

The Status Register bits are summarized in *Table 14: Status Register bits*. Refer to *Table 14* in conjunction with the following sections.

6.11.1 Write protection bit (SR7)

The write protection bit identifies if the device is protected or not. If the write protection bit is set to ‘1’, the device is not protected and program or erase operations are allowed. If the write protection bit is set to ‘0’ the device is protected and program or erase operations are not allowed.

6.11.2 P/E/R Controller and cache ready/busy bit (SR6)

Status Register bit SR6 has two different functions depending on the current operation.

During cache operations, SR6 acts as a cache ready/busy bit, which indicates whether the Cache Register is ready to accept new data. When SR6 is set to '0', the Cache Register is busy, and when SR6 is set to '1', the Cache Register is ready to accept new data.

During all other operations, SR6 acts as a P/E/R Controller bit, which indicates whether the P/E/R Controller is active or inactive. When the P/E/R Controller bit is set to ‘0’, the P/E/R Controller is active (device is busy); when the bit is set to ‘1’, the P/E/R Controller is inactive (device is ready).

6.11.3 P/E/R Controller bit (SR5)

The Program/Erase/Read Controller bit indicates whether the P/E/R Controller is active or inactive during cache operations. When the P/E/R Controller bit is set to ‘0’, the P/E/R Controller is active (device is busy); when the bit is set to ‘1’, the P/E/R Controller is inactive (device is ready).

Note: This bit is only valid for cache operations.

6.11.4 Error bit (SR0)

The error bit identifies if any errors have been detected by the P/E/R Controller. The error bit is set to ’1’ when a program or erase operation has failed to write the correct data to the memory. If the error bit is set to ‘0’ the operation has completed successfully.

6.11.5 SR4, SR3, SR2 and SR1 are reserved

Table 14. Status Register bits

Bit	Name	Logic level	Definition
SR7	Write protection	'1'	Not protected
		'0'	Protected
SR6	Program/Erase/Read Controller	'1'	P/E/R Controller inactive, device ready
		'0'	P/E/R Controller active, device busy
SR5	Program/Erase/Read Controller(1)	'1'	P/E/R Controller inactive, device ready
		'0'	P/E/R Controller active, device busy
SR4, SR3, SR2, SR1	Reserved	‘don’t care’	
SR0	Generic error	‘1’	Error – operation failed
		‘0’	No error – operation successful

1. Only valid for cache operations.

6.12 Read status enhanced

In NAND Flash devices with multiplane architecture, it is possible to independently read the Status Register of a single plane using the Read Status Enhanced command. If the Error bit of the Status Register, SR0, reports an error during or after a multiplane operation, the Read Status Enhanced command is used to know which of the two planes contains the page that failed the operation. Three address cycles are required to address the selected block and page (A18-0).

The output of the Read Status Enhanced command has the same coding as the Read Status command. See *Table 14* for a full description and *Figure 31* for the read status enhanced waveform.

6.13 Read EDC Status Register

The devices contain an EDC Status Register, which provides information on the errors that occurred during the read cycles of the copy back and multiplane copy back operations. In the case of multiplane copy back program, it is not possible to distinguish which of the two read operations caused the error.

The EDCS Status Register is read by issuing the Read EDC Status Register command.

After issuing the Read EDC Status Register command, a read cycle outputs the content of the EDC Status Register to the I/O pins on the falling edge of Chip Enable or Read Enable signals, whichever occurs last. The operation is similar to Read Status Register command.

Table 15: EDC Status Register bits summarizes the EDC Status Register bits. See *Figure 30* for a description of Read EDC Status Register waveforms.

Table 15. EDC Status Register bits

Bit	Name	Logic level	Definition
0	Pass/fail	'1'	Copy back or multiplane copy back operation failed
		'0'	Copy back or multiplane copy back operation succeeded
1	EDC status	'1'	Error
		'0'	No error
2	EDC validity	'1'	Valid
		'0'	Invalid
3	Reserved	'don't care'	-
4	Reserved	'don't care'	-
5	Ready/busy(1)	'1'	Ready
		'0'	Busy
6	Ready/busy(1)	'1'	Ready
		'0'	Busy
7	Write protect	'1'	Not protected
		'0'	Protected

1. See *Table 14: Status Register bits* for a description of SR5 and SR6 bits.

6.14 Read electronic signature

The devices contain a manufacturer code and device code. The following three steps are required to read these codes:

1. One bus write cycle to issue the Read Electronic Signature command (90h)
2. One bus write cycle to input the address (00h)
3. Five bus read cycles to sequentially output the data (as shown in *Table 16: Electronic signature*).

Table 16. Electronic signature

Root part number	Byte 1	Byte 2	Byte 3 (see *Table 17*)	Byte 4 (see *Table 18*)	Byte 5 (see *Table 19*)
NAND04GR3B2D NAND08GR3B4C(1)	20h	ACh	10h	15h	54h
NAND04GW3B2D NAND08GW3B4C(1)	20h	DCh	10h	95h	54h
NAND04GR4B2D	0020h	BCh	10h	55h	54h
NAND04GW4B2D	0020h	CCh	10h	D5h	54h
NAND08GR3B2C	20h	A3h	51h	15h	58h
NAND08GW3B2C	20h	D3h	51h	95h	58h
NAND08GR4B2C	0020h	B3h	51h	55h	58h
NAND08GW4B2C	0020h	C3h	51h	D5h	58h

1. For NAND08G-B4C devices, each 4 Gb die returns its own electronic signature.

Table 17. Electronic signature byte 3

I/O	Definition	Value	Description
I/O1-I/O0	Internal chip number	0 0 0 1 1 0 1 1	1 2 4 8
I/O3-I/O2	Cell type	0 0 0 1 1 0 1 1	2-level cell 4-level cell 8-level cell 16-level cell
I/O5-I/O4	Number of simultaneously programmed pages	0 0 0 1 1 0 1 1	1 2 4 8
I/O6	Interleaved programming between multiple devices	0 1	Not supported Supported
I/O7	Cache program	0 1	Not supported Supported

Table 18. Electronic signature byte 4

I/O	Definition	Value	Description
I/O1-I/O0	Page size (without spare area)	0 0 0 1 1 0 1 1	1 Kbytes 2 Kbytes 4 Kbytes 8 Kbytes
I/O2	Spare area size (byte/512 byte)	0 1	8 16
I/O7, I/O3	Minimum sequential access time	0 0 1 0 0 1 1 1	30/50 ns 25 ns Reserved Reserved
I/O5-I/O4	Block size (without spare area)	0 0 0 1 1 0 1 1	64 Kbytes 128 Kbytes 256 Kbytes 512 Kbytes
I/O6	Organization	0 1	x8 x16

Table 19. Electronic signature byte 5

I/O	Definition	Value	Description
I/O1 - I/O0	Reserved	0 0	
I/O3 - I/O2	Plane number	0 0 0 1 1 0 1 1	1 plane 2 planes 4 planes 8 planes
I/O6 - I/O4	Plane size (without spare area)	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	64 Mbits 128 Mbits 256 Mbits 512 Mbits 1 Gb 2 Gb 4 Gb 8 Gb
I/O7	Reserved	0	

6.15 Read ONFI signature

To recognize NAND Flash devices that are compatible with the ONFI 1.0 command set, the Read Electronic Signature can be issued, followed by an address of 20h. The next four bytes output is the ONFI signature, which is the ASCII encoding of the “ONFI” word. Reading beyond four bytes produces indeterminate values.

Figure 33 provides a description of the read ONFI signature waveform and *Table 20* provides the definition of the output bytes.

Table 20. Read ONFI signature

Byte	Value	ASCII character
1st byte	4Fh	O
2nd byte	4Eh	N
3rd byte	46h	F
4th byte	49h	I
5th byte	Undefined	Undefined

6.16 Read parameter page

The Read Parameter Page command retrieves the data structure that describes the NAND Flash organization, features, timings and other behavioral parameters. This data structure enables the host processor to automatically recognize the NAND Flash configuration of a device. The whole data structure is repeated at least five times.

See *Figure 40* for a description of the read parameter page waveform.

The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.

The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

Read status enhanced is not be used during execution of the Read Parameter Page command.

Table 21 defines the parameter page data structure; for parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.

Values are reported in the parameter page in bytes when referring to items related to the size of data access (as in an x8 data access device). For example, the chip returns how many data bytes are in a page. For a device that supports x16 data access, the host is required to convert byte values to word values for its use. Unused fields are set to 0h.

For more detailed information about parameter page data bits, refer to ONFI Specification 1.0, section 5.4.1.

Table 21. Parameter page data structure

	Byte	O/M[1]	Description	
Revision information and features block	0-3	M	Parameter page signature – Byte 0: 4Fh, "O" – Byte 1: 4Eh, "N" – Byte 2: 46h, "F" – Byte 3: 49h, "I"	
	4-5	M	**Revision number**	
			Bit 2 to bit 15	Reserved (0)
			Bit 1	1 = supports ONFI version 1.0
			Bit 0	Reserved (0)
	6-7	M	**Features supported**	
			Bit 5 to bit 15	Reserved (0)
			Bit 4	1 = supports odd to even page copyback
			Bit 3	1 = supports interleaved operations
			Bit 2	1 = supports non-sequential page programming
			Bit 1	1 = supports multiple LUN operations
			Bit 0	1 = supports 16-bit data bus width
	8-9	M	**Optional commands supported**	
			Bit 6 to bit 15	Reserved (0)
			Bit 5	1 = supports Read Unique ID
			Bit 4	1 = supports Copyback
			Bit 3	1 = supports Read Status Enhanced
			Bit 2	1 = supports Get Features and Set Features
			Bit 1	1 = supports Read Cache commands
			Bit 0	1 = supports Page Cache Program command
	10-31			Reserved (0)
Manufacturer information block	32-43	M	Device manufacturer (12 ASCII characters)	
	44-63	M	Device model (20 ASCII characters)	
	64	M	JEDEC manufacturer ID	
	65-66	O	Date code	
	67-79		Reserved (0)	
	80-83	M		Number of data bytes per page
	84-85	M		Number of spare bytes per page
	86-89	M		Number of data bytes per partial page
	90-91	M		Number of spare bytes per partial page
	92-95	M		Number of pages per block

Table 21. Parameter page data structure (continued)

	Byte	O/M(1)	Description	
Memory organization block	96-99	M		Number of blocks per logical unit (LUN)
	100	M		Number of logical units (LUNs)
	101	M	**Number of address cycles**	
			Bit 4 to bit 7	Column address cycles
			Bit 0 to bit 3	Row address cycles
	102	M		Number of bits per cell
	103-104	M		Bad blocks maximum per LUN
	105-106	M		Block endurance
	107	M		Guaranteed valid blocks at beginning of target
	108-109	M		Block endurance for guaranteed valid blocks
	110	M		Number of programs per page
	111	M	**Partial programming attributes**	
			Bit 5 to bit 7	Reserved
			4	1 = partial page layout is partial page data followed by partial page spare
			Bit 1 to bit 3	Reserved
			0	1 = partial page programming has constraints
	112	M		Number of bits ECC correctability
	113	M	**Number of interleaved address bits**	
			Bit 4 to bit 7	Reserved (0)
			Bit 0 to bit 3	Number of interleaved address bits
	114	O	**Interleaved operation attributes**	
			Bit 4 to bit 7	Reserved (0)
			Bit 3	Address restrictions for program cache
			Bit 2	1 = program cache supported
			Bit 1	1 = no block address restrictions
			Bit 0	Overlapped/concurrent interleaving support
	115-127			Reserved (0)
	128	M		I/O pin capacitance

Table 21. Parameter page data structure (continued)

	Byte	O/M(1)	Description	
Electrical parameters block	129-130	M	**Timing mode support**	
			Bit 6 to bit 15	Reserved (0)
			Bit 5	1 = supports timing mode 5
			Bit 4	1 = supports timing mode 4
			Bit 3	1 = supports timing mode 3
			Bit 2	1 = supports timing mode 2
			Bit 1	1 = supports timing mode 1
			Bit 0	1 = supports timing mode 0, shall be 1
	131-132	O	**Program cache timing mode support**	
			Bit 6 to bit 15	Reserved (0)
			Bit 5	1 = supports timing mode 5
			Bit 4	1 = supports timing mode 4
			Bit 3	1 = supports timing mode 3
			Bit 2	1 = supports timing mode 2
			Bit 1	1 = supports timing mode 1
			Bit 0	1 = supports timing mode 0
	133-134	M		t_{PROG} maximum page program time (µs)
	135-136	M		t_{BERS} maximum block erase time (µs)
	137-138	M		t_R maximum page read time (µs)
	139-163	M		Reserved (0)
Vendor block	164-165	M		Vendor specific revision number
	166-253	M		Vendor specific
	254-255	M		Integrity CRC
Red. param. pages	256-511	M		Value of bytes 0-255
	512-767	M		Value of bytes 0-255
	768+	O		Additional redundant parameter pages

1. O = optional, M = mandatory

7 Concurrent operations and extended read status

The NAND08G-BxC devices are composed of two 4-Gbit dice stacked together. This configuration allows the devices to support concurrent operations, which means that while performing an operation in one die (erase, read, program, etc.), another operation is possible in the other die.

The standard Read Status Register operation returns the status of the NAND08G-BxC device. To provide information on each 4-Gbit die, the NAND08G-BxC devices feature an Extended Read Status Register command that independently checks the status of each NAND04G-B2D.

The following steps are required to perform concurrent operations:

1. Select one of the two dice by setting the most significant address bit A30 to ‘0’ or ‘1’.
2. Execute one operation on this die.
3. Launch a concurrent operation on the other die.
4. Check the status of these operations by performing an Extended Read Status Register operation.

All combinations of operations are possible except read while read. This is due to the fact that the input/output bus is common to both dice.

Refer to *Table 22* for the description of the Extended Read Status Register command sequence, and to *Table 14*. for the definition of the Status Register bits.

Table 22. Extended Read Status Register commands

Command	Address range	1 bus write cycle
Read 1st die status	Address ≤0x3FFFFFFF	F2h
Read 2nd die status	0x3FFFFFFF < Address ≤0x7FFFFF	F3h

8 Data protection

The devices feature a Write Protect, $\overline{WP}$, pin, which can be used to protect the device against program and erase operations. It is recommended to keep $\overline{WP}$ at V_{IL} during power-up and power-down.

9 Software algorithms

This section provides information on the software algorithms that Numonyx recommends implementing to manage the bad blocks and extend the lifetime of the NAND device.

NAND Flash memories are programmed and erased by Fowler-Nordheim tunnelling using high voltage. Exposing the device to high voltage for extended periods damages the oxide layer.

To extend the number of program and erase cycles and increase the data retention, the:

- Number of program and erase cycles is limited (see *Table 24: Program erase times and program erase endurance cycles* for the values)
- Implementation of a garbage collection, a wear-leveling algorithm and an error correction code is recommended.

To help integrate a NAND memory into an application, Numonyx provides a file system OS native reference software, which supports the basic commands of file management.

Contact the nearest Numonyx sales office for more details.

9.1 Bad block management

Devices with bad blocks have the same quality level and the same AC and DC characteristics as devices that have all valid blocks. A bad block does not affect the performance of valid blocks because it is isolated from the bit and common source lines by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The bad block information is written prior to shipping. Any block, where the 1st and 6th bytes or the 1st word in the spare area of the 1st page, does not contain FFh, is a bad block.

The bad block information must be read before any erase is attempted as the bad block Information may be erased. For the system to be able to recognize the bad blocks based on the original information, the creation of a bad block table following the flowchart shown in *Figure 21: Bad block management flowchart* is recommended.

9.2 NAND Flash memory failure modes

Over the lifetime of the device bad blocks may develop. To implement a highly reliable system, the possible failure modes must be considered.

- Program/erase failure

  In this case, the block has to be replaced by copying the data to a valid block. These additional bad blocks can be identified because attempts to program or erase them gives errors in the Status Register. As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by reprogramming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block. See *Section 6.5: Copy back program* for more details.

- Read failure

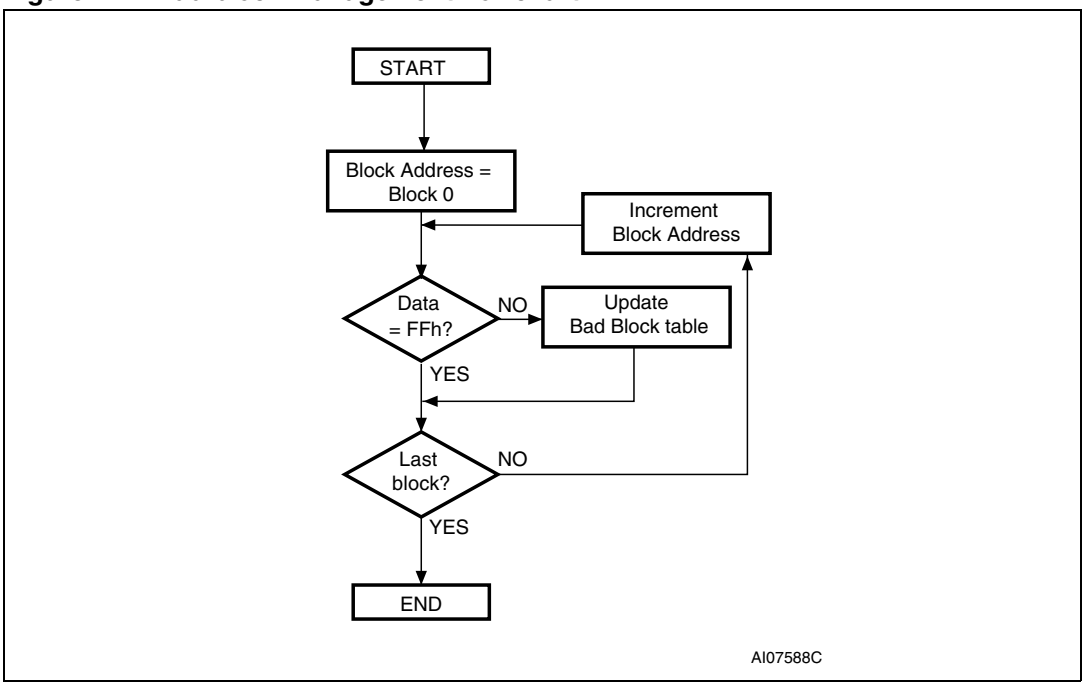
  In this case, ECC correction must be implemented. To efficiently use the memory space, the recovery of a single-bit error in read by ECC, without replacing the whole block, is recommended.

Refer to *Table 23: Block failure* for the recommended procedure to follow if an error occurs during an operation.

Table 23. Block failure

Operation	Procedure
Erase	Block replacement
Program	Block replacement or ECC
Read	ECC

Figure 21. Bad block management flowchart

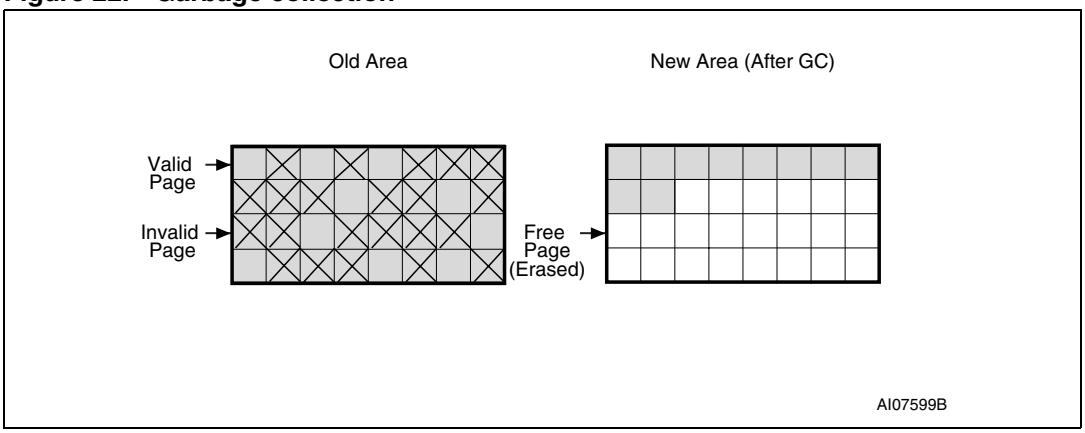


9.3 Garbage collection

When a data page needs to be modified, it is faster to write to the first available page, resulting in the previous page being marked as invalid. After several updates it is necessary to remove invalid pages to free memory space.

To free this memory space and allow further program operations, the implementation of a garbage collection algorithm is recommended. In garbage collection software, the valid pages are copied into a free area and the block containing the invalid pages is erased as show in *Figure 22*.

Figure 22. Garbage collection



9.4 Wear-leveling algorithm

For write-intensive applications, the implementation of a wear-leveling algorithm is recommended to monitor and spread the number of write cycles per block.

In memories that do not use a wear-leveling algorithm, not all blocks get used at the same rate. The wear-leveling algorithm ensures that equal use is made of all the available write cycles for each block. There are two wear-leveling levels:

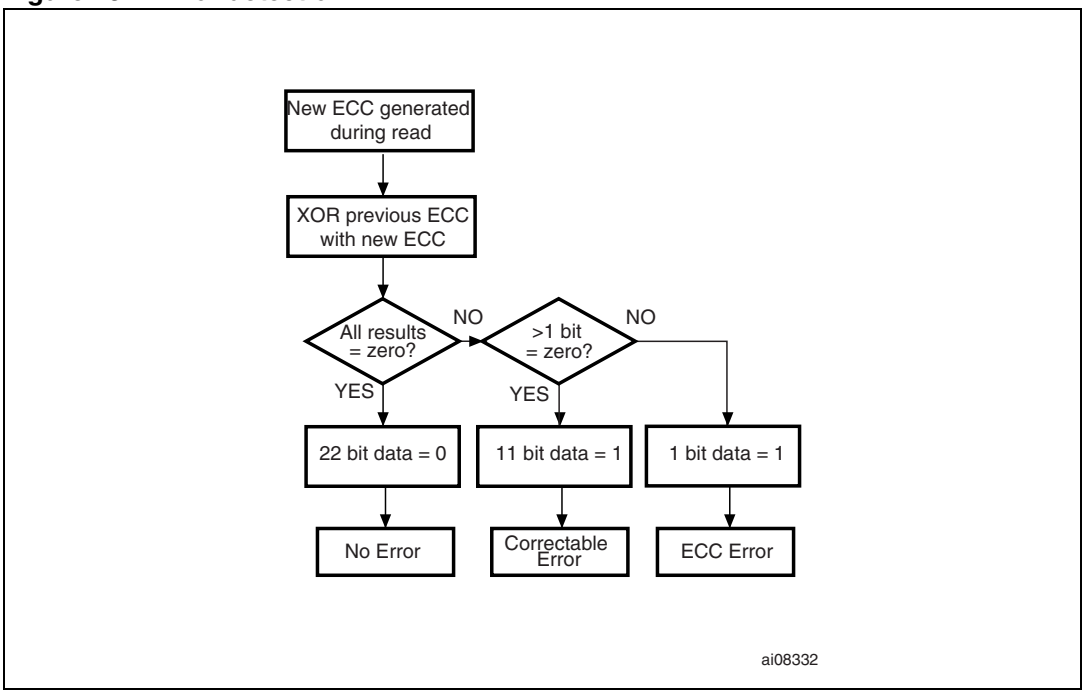
- First level wear-leveling, where new data is programmed to the free blocks that have had the fewest write cycles.
- Second level wear-leveling, where long-lived data is copied to another block so that the original block can be used for more frequently-changed data.

The second level wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

9.5 Error correction code

An ECC can be implemented in the NAND Flash memories to identify and correct errors in the data. For every 2048 bits in the device, the implementation of 22 bits of ECC (16 bits for line parity plus 6 bits for column parity) is recommended.

Figure 23. Error detection



10 Program and erase times and endurance cycles

The program and erase times and the number of program/erase cycles per block are shown in *Table 24*.

Table 24. Program erase times and program erase endurance cycles

Parameters	NAND Flash			Unit
	Min	Typ	Max	
Page Program/Multiplane Program time		200	700	µs
Block Erase/Multiplane Erase time		1.5	2	ms
Multiplane Program time (1.8 V)		250	800	µs
Multiplane Erase (1.8 V)		2	2.5	ms
Multiplane Program Busy time (t_{IPBSY})		0.5	1	µs
Multiplane Erase Busy time (t_{IEBSY})		0.5	1	µs
Cache Read Busy time (t_{RCBSY})		3	t_R	µs
Program/erase cycles per block (with ECC)	100 000			Cycles
Data retention	10			Years

11 Maximum ratings

Stressing the device above the ratings listed in *Table 25: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer to the Numonyx SURE Program and other relevant quality documents for more information.

Table 25. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature under bias	– 50	125	°C
T_{STG}	Storage temperature	– 65	150	°C
V_{IO}(1)	Input or output voltage	– 0.6	4.6	V
V_{DD}	Supply voltage	– 0.6	4.6	V

1. Minimum voltage may undershoot to –2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2 V for less than 20 ns during transitions on I/O pins.

12 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the devices. The parameters in the following DC and AC characteristics tables are derived from tests performed under the measurement conditions summarized in *Table 26*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 26. Operating and AC measurement conditions

Parameter		NAND Flash		Units
		Min	Max	
Supply voltage (V_{DD})		2.7	3.6	V
Ambient temperature (T_A)	Grade 1	0	70	°C
	Grade 6	–40	85	°C
Load capacitance (C_L) (1 TTL GATE and C_L)	1.8 V device	30		pF
	3.0 V device	50		pF
Input pulses voltages		0	V_{DD}	V
Input and output timing ref. voltages		$V_{DD}/2$		V
Output circuit resistor R_{ref}		8.35		kΩ
Input rise and fall times		5		ns

Table 27. Capacitance(1)

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V		10	pF
$C_{I/O}$	Input/output capacitance(2)	V_{IL} = 0V		10	pF

1. T_A = 25°C, f = 1MHz. C_{IN} and $C_{I/O}$ are not 100% tested.
2. Input/output capacitances double in stacked devices.

Figure 24. Equivalent testing circuit for AC characteristics measurement

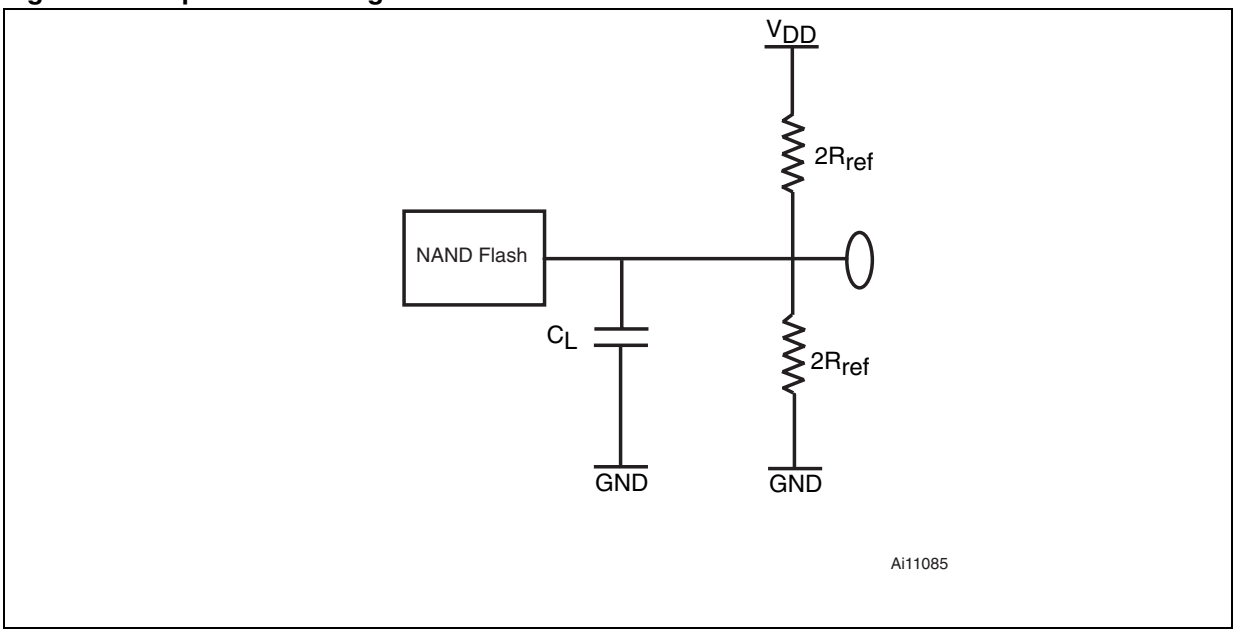


Table 28. DC characteristics (1.8 V devices)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential read	t_{RLRL} minimum $\overline{E}=V_{IL}$, I_{OUT} = 0 mA	-	10	20	mA
I_{DD2}		Program	-	-	10	20	mA
I_{DD3}		Erase	-	-	10	20	mA
I_{DD5}	Standby current (CMOS(1))		$\overline{E}=V_{DD}$-0.2, $\overline{WP}=0/V_{DD}$	-	10	50	µA
I_{LI}	Input leakage current(1)		V_{IN}= 0 to V_{DD}max	-	-	±10	µA
I_{LO}	Output leakage current(1)		V_{OUT}= 0 to V_{DD}max	-	-	±10	µA
V_{IH}	Input high voltage		-	0.8 * V_{DD}	-	V_{DD} + 0.3	V
V_{IL}	Input low voltage		-	-0.3	-	0.2 * V_{DD}	V
V_{OH}	Output high voltage level		I_{OH} = -100 µA	V_{DD} - 0.1	-	-	V
V_{OL}	Output low voltage level		I_{OL} = 100 µA	-	-	0.1	V
I_{OL} ($R\overline{B}$)	Output low current ($R\overline{B}$)		V_{OL} = 0.1 V	3	-	4	mA
V_{LKO}	V_{DD} supply voltage (erase and program lockout)		-	-	-	1.2	V

1. Leakage current and standby current double in stacked devices.

Table 29. DC characteristics (3 V devices)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential read	t_{RLRL} minimum $\overline{E}$ = V_{IL}, I_{OUT} = 0 mA	-	15	30	mA
I_{DD2}		Program	-	-	15	30	mA
I_{DD3}		Erase	-	-	15	30	mA
I_{DD4}	Standby current (TTL)(1)		E = V_{IH}, $\overline{WP}$ = 0/V_{DD}			1	mA
I_{DD5}	Standby current (CMOS)(1)		$\overline{E}$ = V_{DD}-0.2, $\overline{WP}$ = 0/V_{DD}	-	10	50	µA
I_{LI}	Input leakage current(1)		V_{IN}= 0 to V_{DD}max	-	-	±10	µA
I_{LO}	Output leakage current(1)		V_{OUT}= 0 to V_{DD}max	-	-	±10	µA
V_{IH}	Input High voltage		-	0.8 V_{DD}	-	V_{DD}+0.3	V
V_{IL}	Input Low voltage		-	-0.3	-	0.2 V_{DD}	V
V_{OH}	Output High voltage Level		I_{OH} = -400 µA	2.4	-	-	V
V_{OL}	Output Low voltage Level		I_{OL} = 2.1 mA	-	-	0.4	V
I_{OL} ($R\overline{B}$)	Output Low current ($R\overline{B}$)		V_{OL} = 0.4 V	8	-	10	mA
V_{LKO}	V_{DD} supply voltage (erase and program lockout)		-	-	-	1.8	V

1. leakage current and standby current double in stacked devices.

Table 30. AC characteristics for command, address, data input

Symbol	Alt. Symbol	Parameter			1.8 V	3 V	Unit
t_{ALLWH}	t_{ALS}	Address Latch Low to Write Enable high	AL setup time	Min	25	12	ns
t_{ALHWH}		Address Latch High to Write Enable high					
t_{CLHWH}	t_{CLS}	Command Latch High to Write Enable high	CL setup time	Min	25	12	ns
t_{CLLWH}		Command Latch Low to Write Enable high					
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data setup time	Min	20	12	ns
t_{ELWH}	t_{CS}	Chip Enable Low to Write Enable high	$\overline{E}$ setup time	Min	35	20	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL hold time	Min	10	5	ns
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	10	5	ns
t_{WHCLL}		Write Enable High to Command Latch Low					
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data hold time	Min	10	5	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ hold time	Min	10	5	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ high hold time	Min	15	10	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ pulse width	Min	25	12	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write cycle time	Min	45	25	ns

Table 31. AC characteristics for operations(1)

Symbol	Alt. symbol	Parameter			1.8 V	3 V	Unit
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read electronic signature	Min	10	10	ns
t_{ALLRL2}			Read cycle	Min	10	10	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20	20	ns
t_{BLBH1}		Ready/Busy Low to Ready/Busy High	Read Busy time	Max	25	25	µs
t_{BLBH2}	t_{PROG}		Program Busy time	Max	700	700	µs
t_{BLBH3}	t_{BERS}		Erase Busy time	Max	2	2	ms
t_{BLBH4}	t_{RST}		Reset Busy time, during ready	Max	5	5	µs
			Reset Busy time, during read	Max	5	5	µs
			Reset Busy time, during program	Max	10	10	µs
			Reset Busy time, during erase	Max	500	500	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	10	10	ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0	0	ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	30	30	ns
t_{EHALX}	t_{CSD}	Chip Enable High to Address Latch ‘don’t care’		Min	10	10	ns
t_{EHCLX}		Chip Enable High to Command Latch ‘don’t care’					
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-z		Max	100	100	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	45	25	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High Hold time	Min	15	10	ns
t_{EHQX}	t_{COH}	Chip Enable high to Output Hold		Min	15	15	ns
t_{RHQX}	t_{RHOH}	Read Enable High to Output Hold		Min	15	15	ns
t_{RLQX}	t_{RLOH}	Read Enable Low to Output Hold (EDO mode)		Min	5	5	ns
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable pulse width	Min	25	12	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read cycle time	Min	45	25	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable access time	Max	30	20	ns
			Read ES access time(2)				
t_{WHBH}	t_{R}	Write Enable High to Ready/Busy High	Read Busy time	Max	25	25	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100	100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	60	60	ns
t_{RHWL}	t_{RHW}	Read Enable High to Write Enable Low		Min	100	100	ns

Table 31. AC characteristics for operations(1) (continued)

t_{WHWH}	t_{ADL}(3)	Last address latched to data loading time during program operations	Min	100	70	ns
t_{VHWH} t_{VLWH}	t_{WW}(4)	Write protection time	Min	100	100	ns

1. The time to Ready depends on the value of the pull-up resistor tied to the Ready/Busy pin. See *Figure 41*, *Figure 42* and *Figure 43*.
2. ES = Electronic Signature.
3. t_{ADL} is the time from $\overline{W}$ rising edge during the final address cycle to $\overline{W}$ rising edge during the first data cycle.
4. During a Program/Erase Enable Operation, t_{WW} is the delay from $\overline{WP}$ high to $\overline{W}$ High.
During a Program/Erase Disable Operation, t_{WW} is the delay from $\overline{WP}$ Low to $\overline{W}$ High.

Figure 25. Command latch AC waveforms

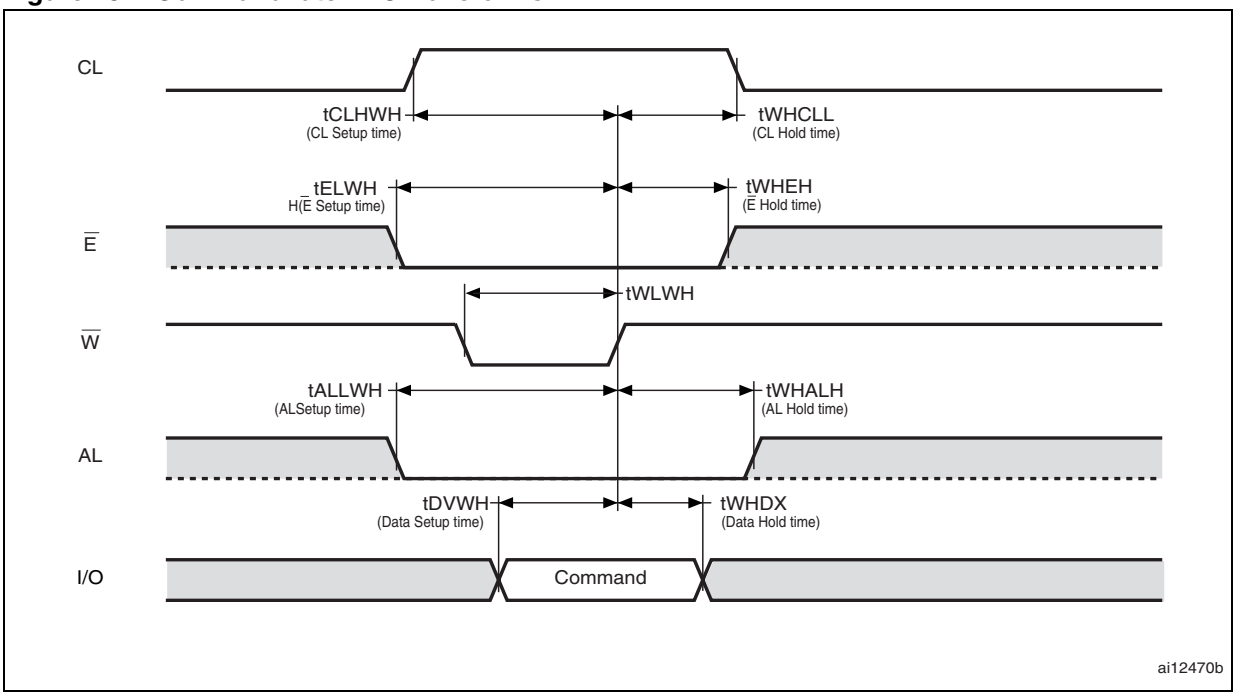


Figure 26. Address latch AC waveforms

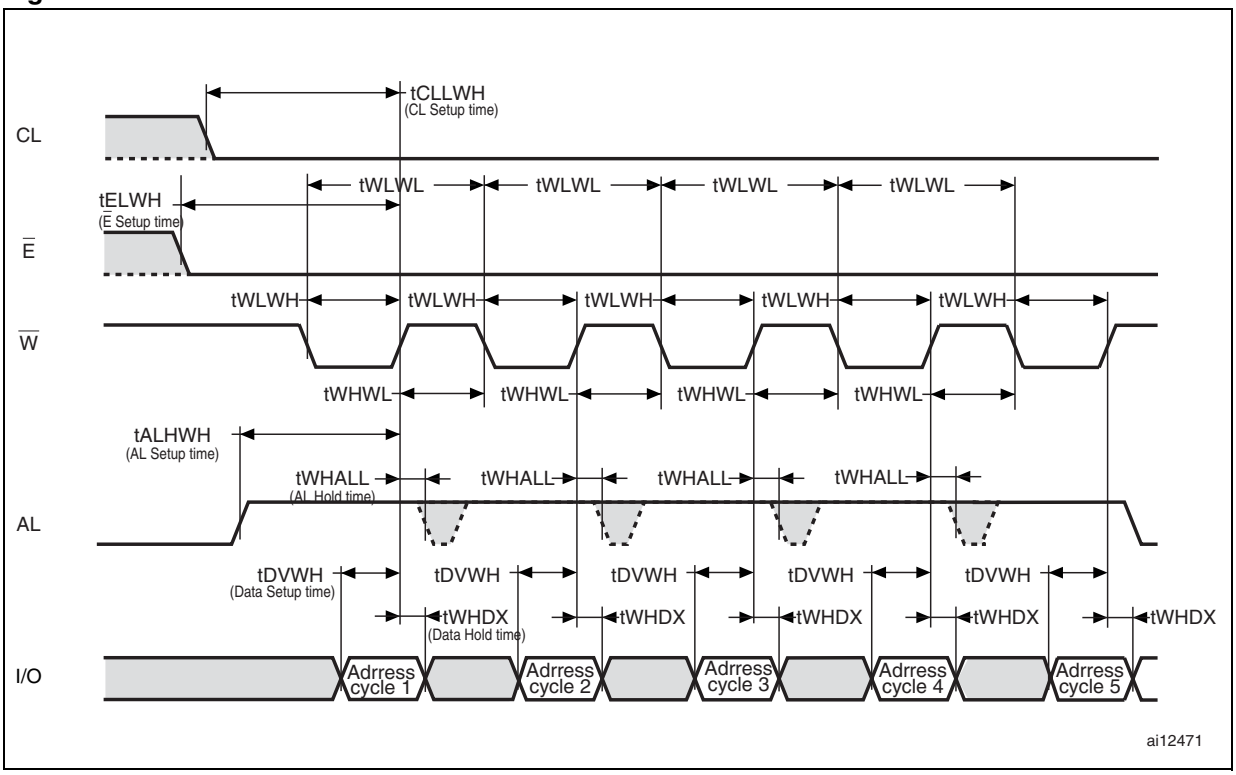
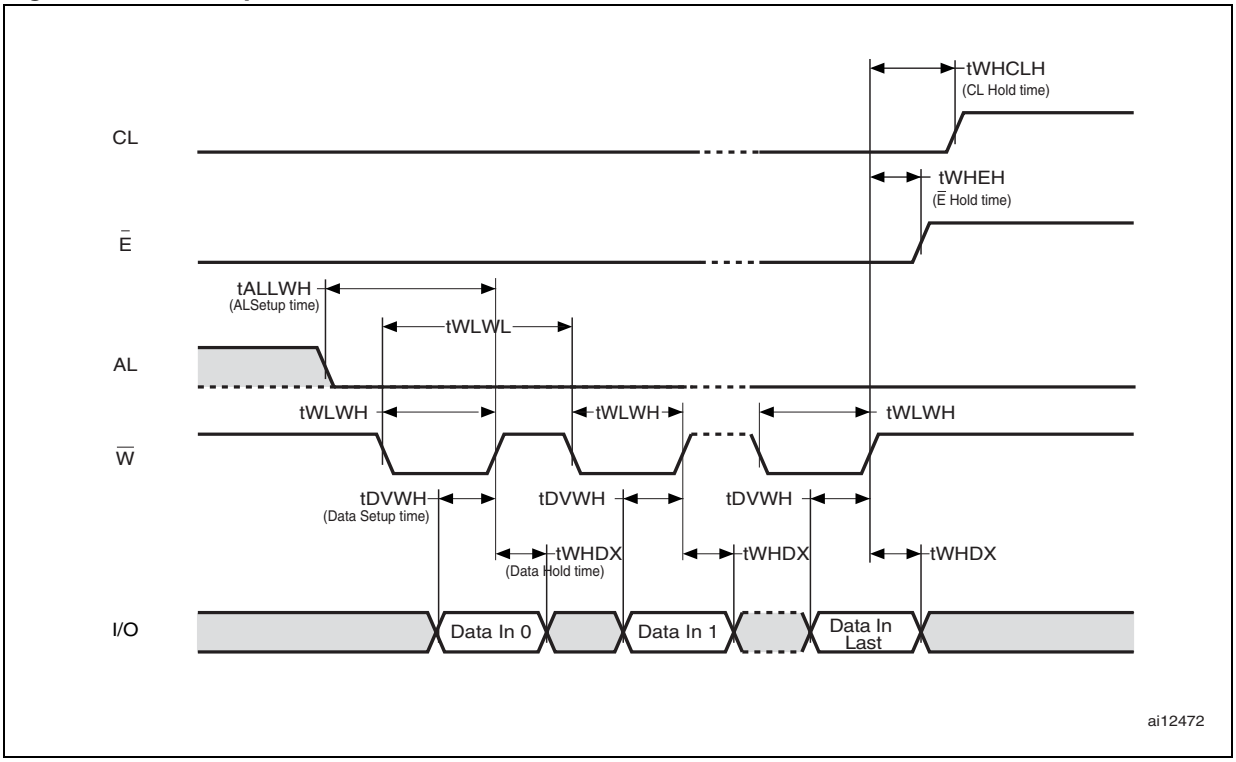
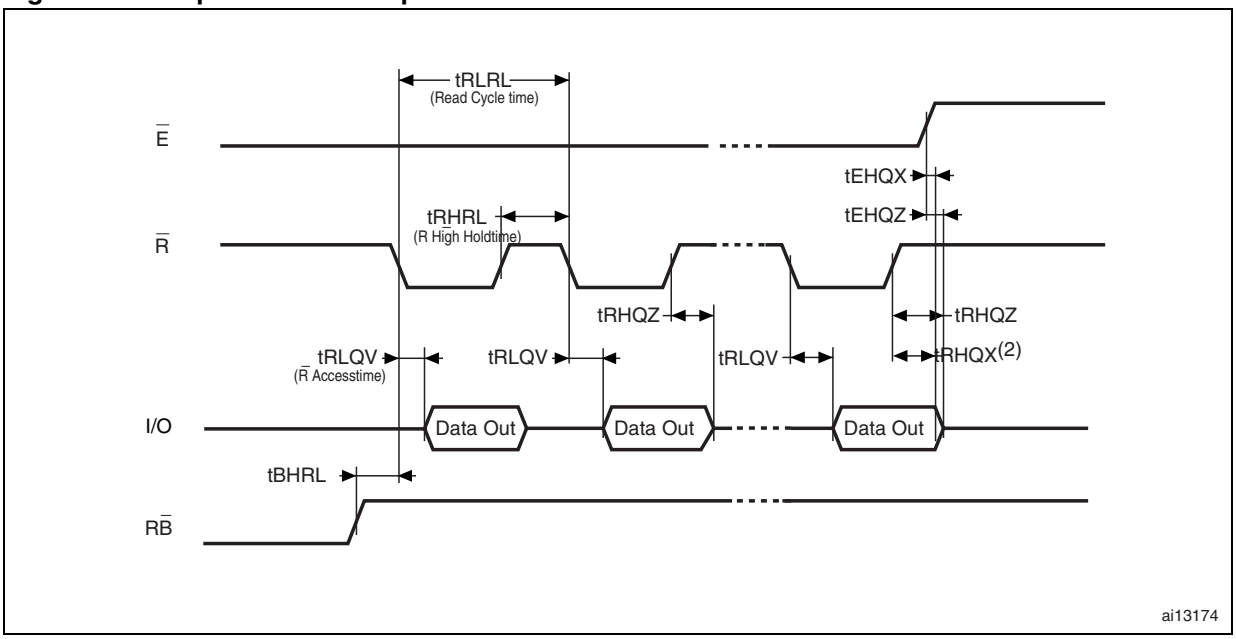


Figure 27. Data input latch AC waveforms



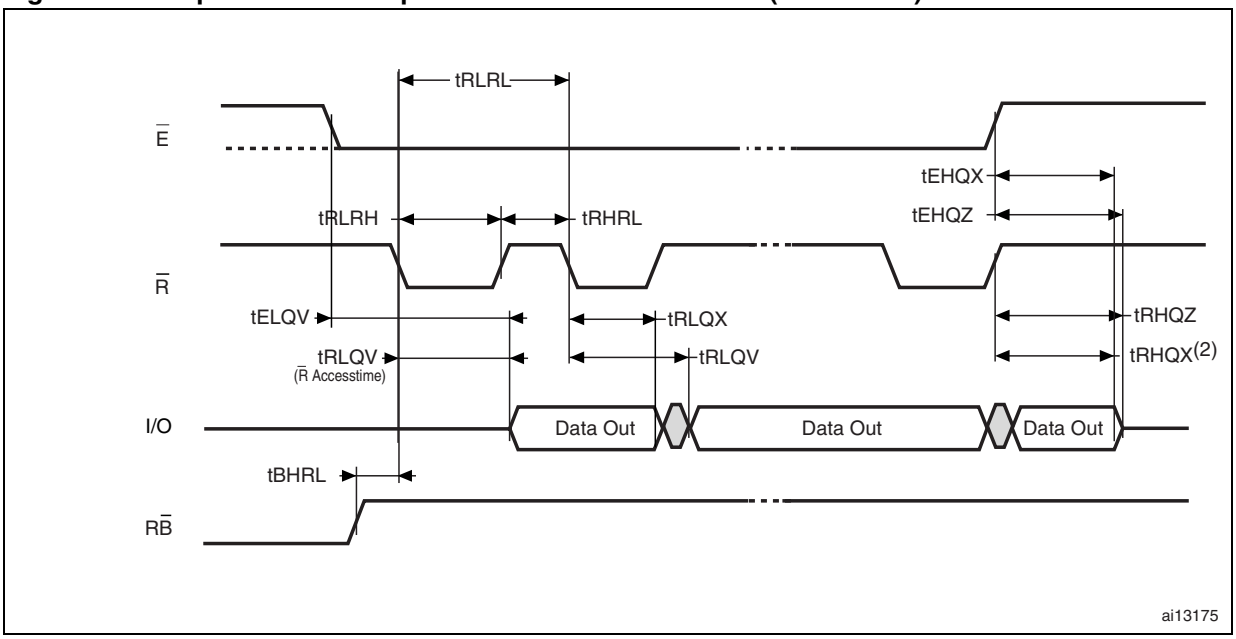
1. The last data input is the 2112th.

Figure 28. Sequential data output after read AC waveforms



1. CL = Low, AL = Low, $\overline{W}$ = High.
2. t_{RHQX} is applicable for frequencies lower than 33MHz (i.e. t_{RLRL} higher than 30ns).

Figure 29. Sequential data output after read AC waveforms (EDO mode)



1. In EDO mode, CL and AL are Low, V_{IL}, and $\overline{W}$ is High, V_{IH}.
2. t_{RLQX} is applicable for frequencies high than 33 MHz (i.e. t_{RLRL} lower than 30 ns).

Figure 30. Read Status Register or read EDC Status Register AC waveform

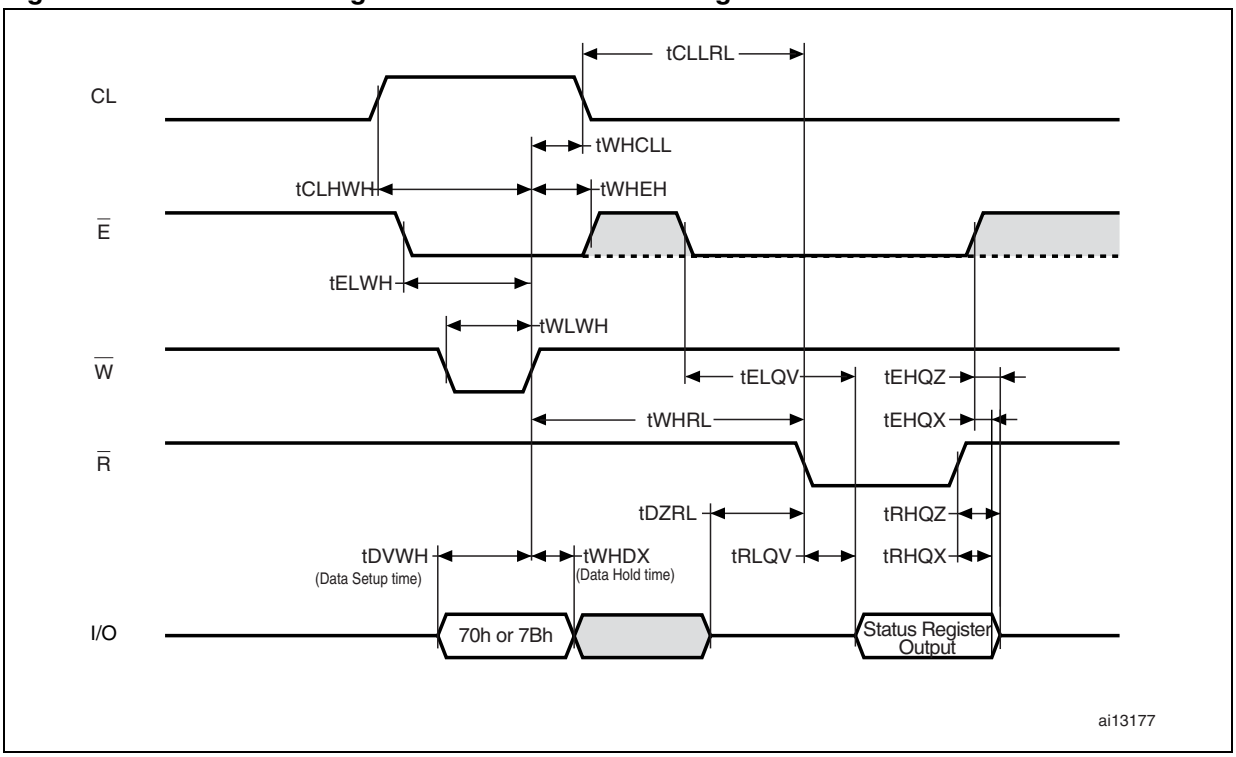


Figure 31. Read status enhanced waveform

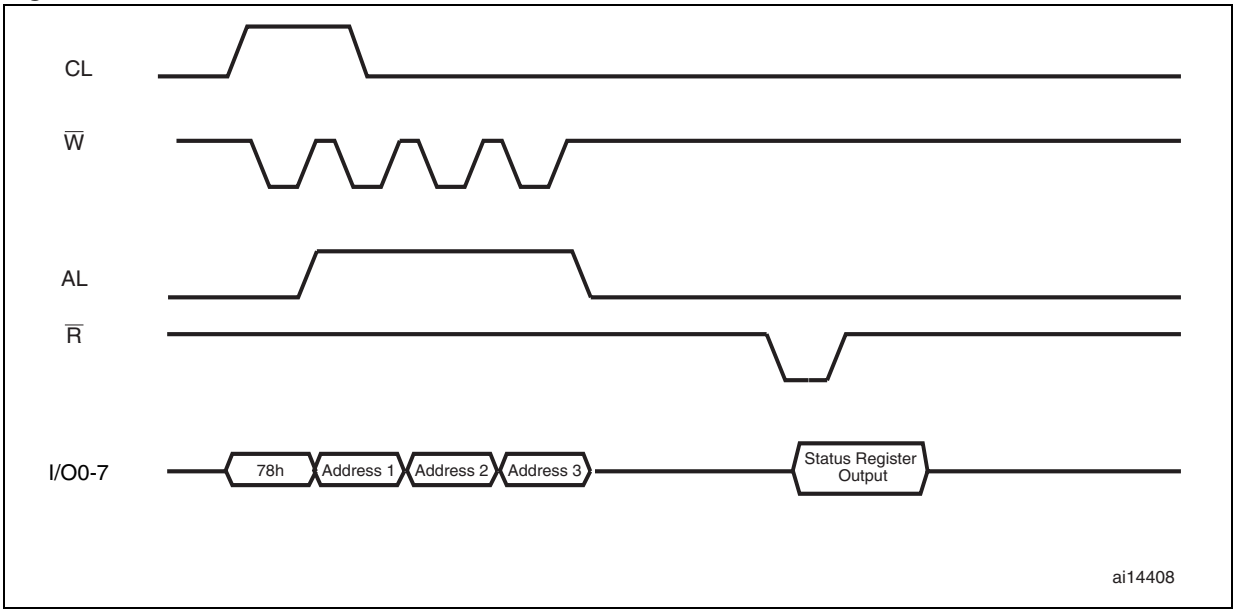
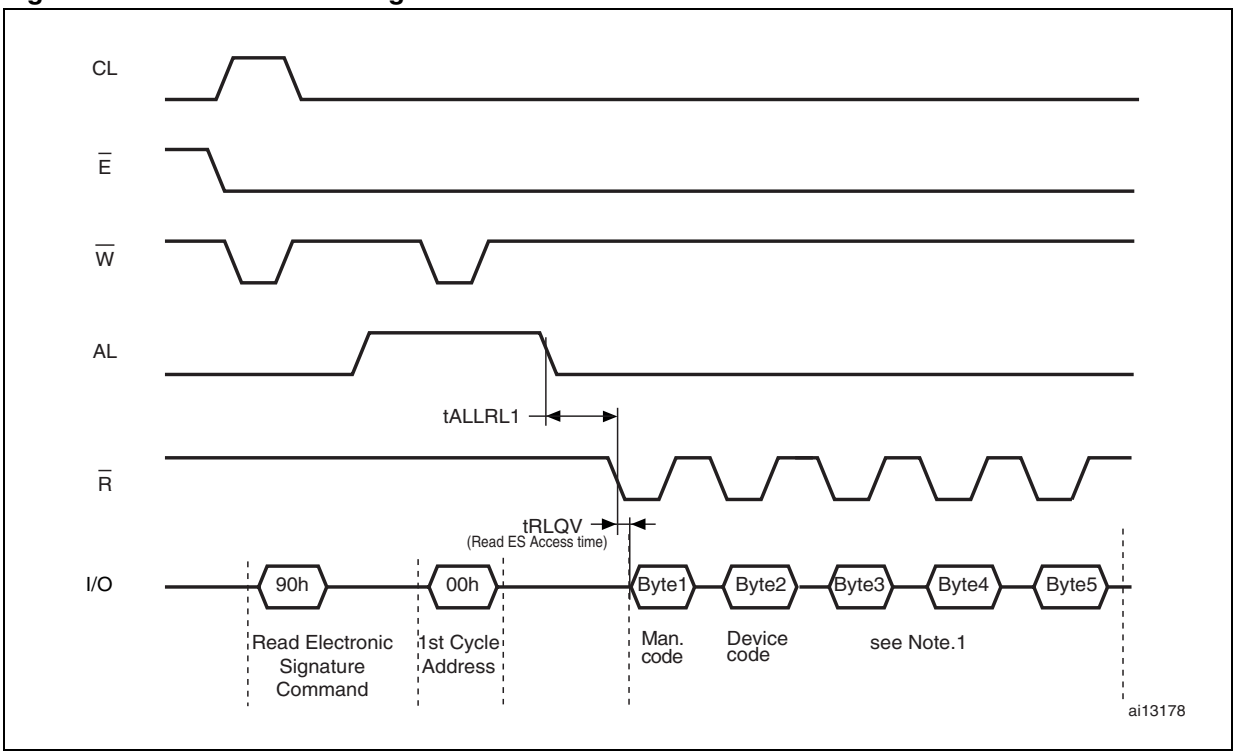


Figure 32. Read Electronic Signature AC waveform



1. Refer to *Table 16* for the values of the manufacturer and device codes, and to *Table 17*, *Table 18*, and *Table 19* for the information contained in byte 3, byte 4, and byte 5.

Figure 33. Read ONFI signature waveform

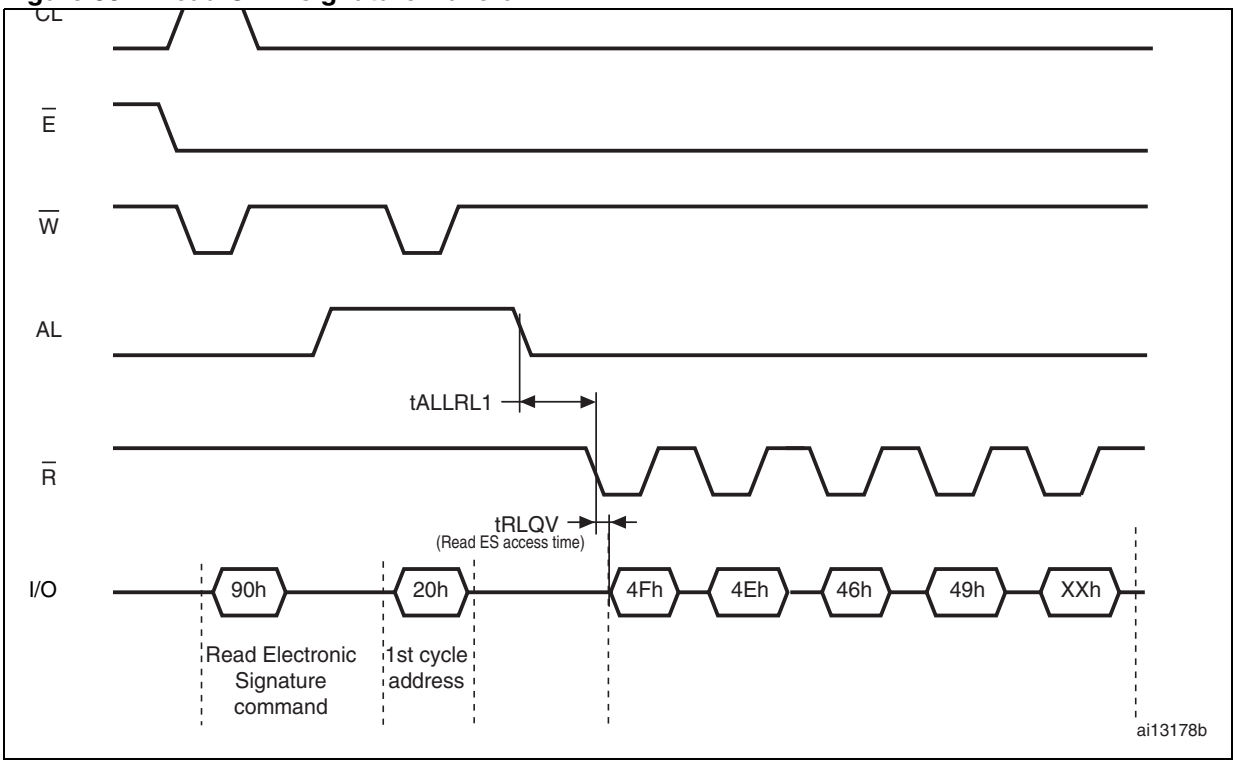


Figure 34. Page read operation AC waveform

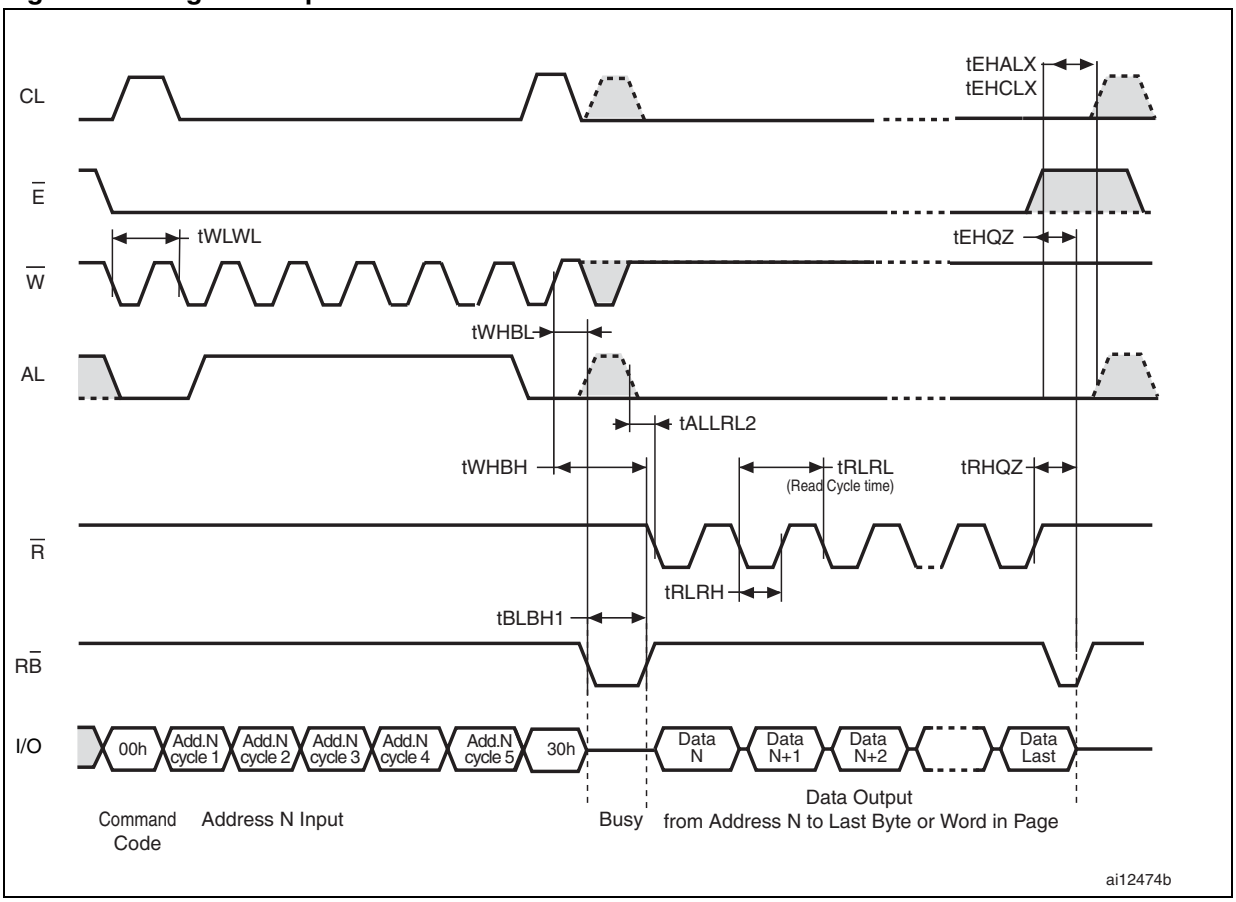


Figure 35. Page program AC waveform

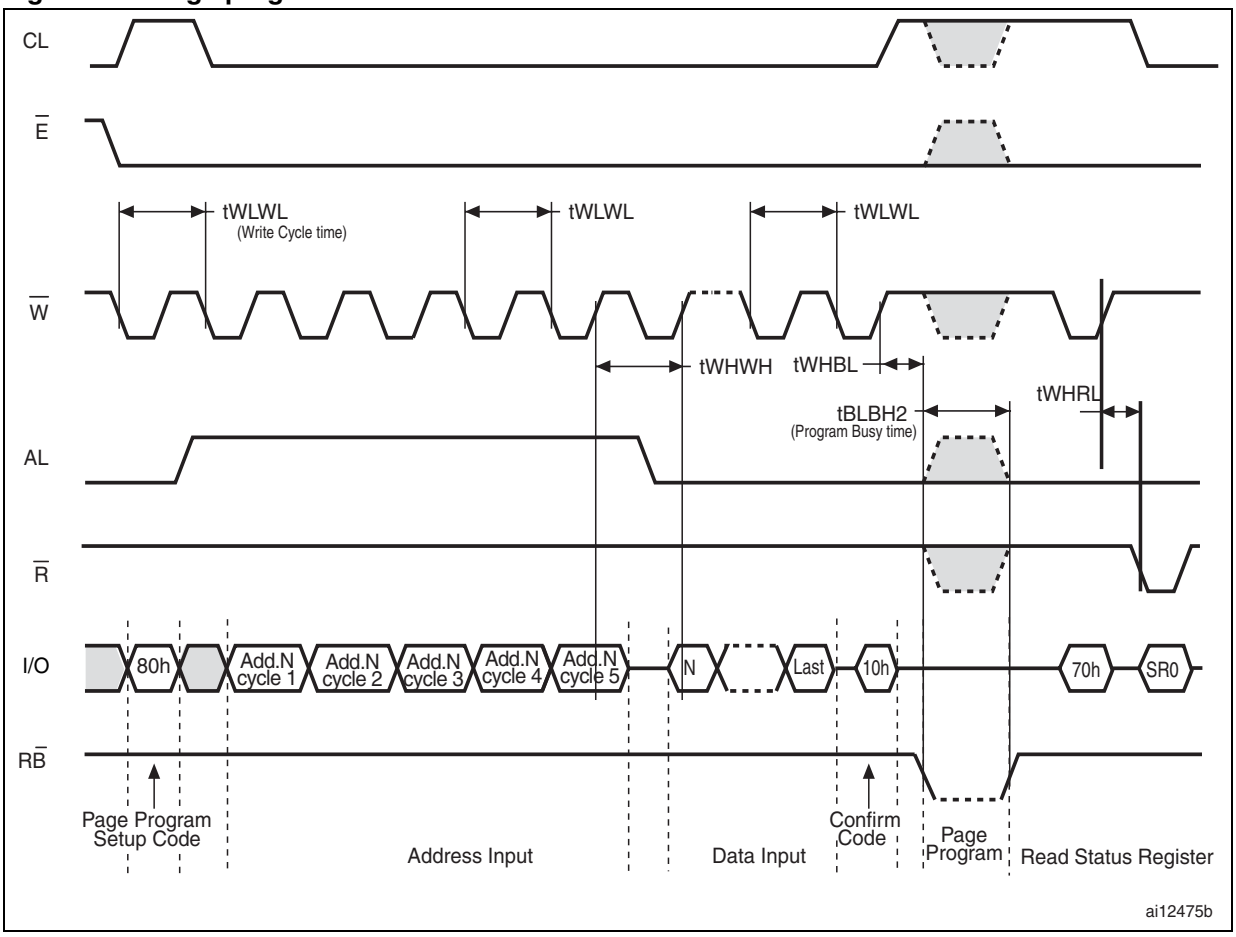


Figure 36. Block erase AC waveform

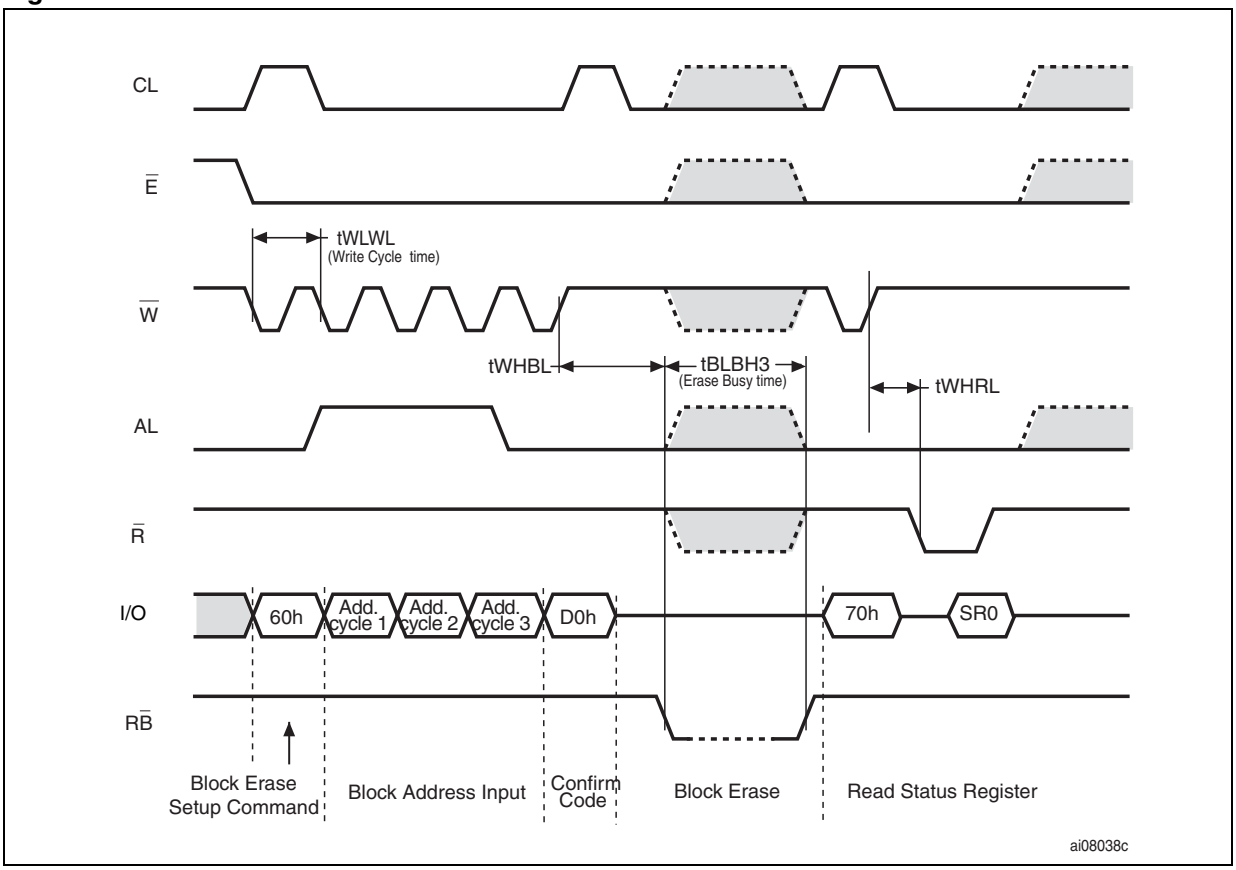


Figure 37. Reset AC waveform

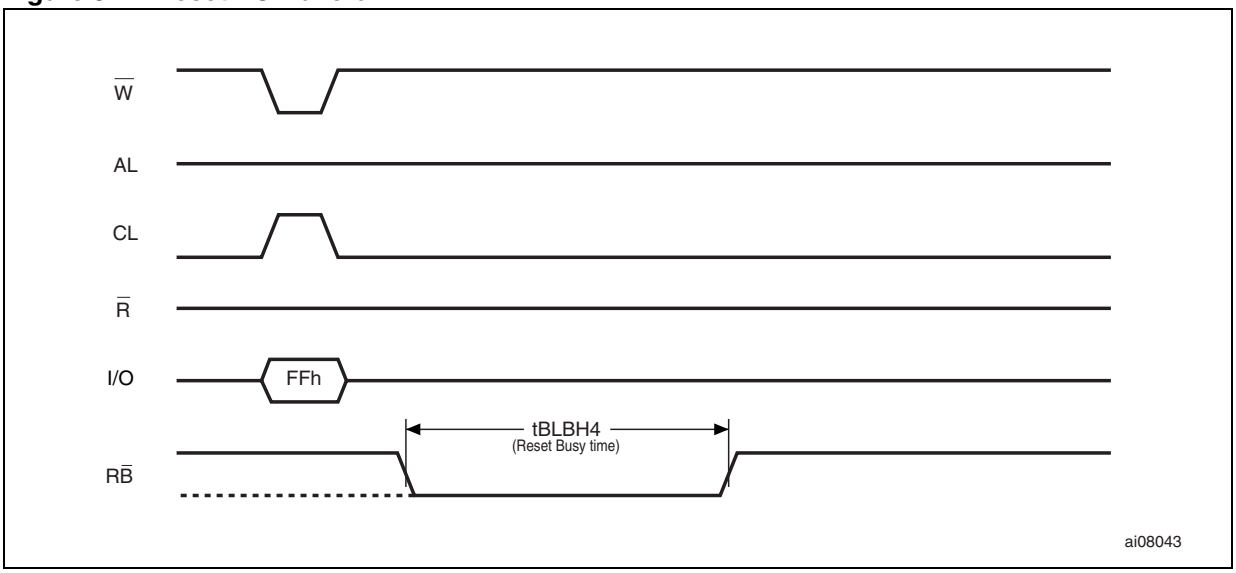


Figure 38. Program/erase enable waveform

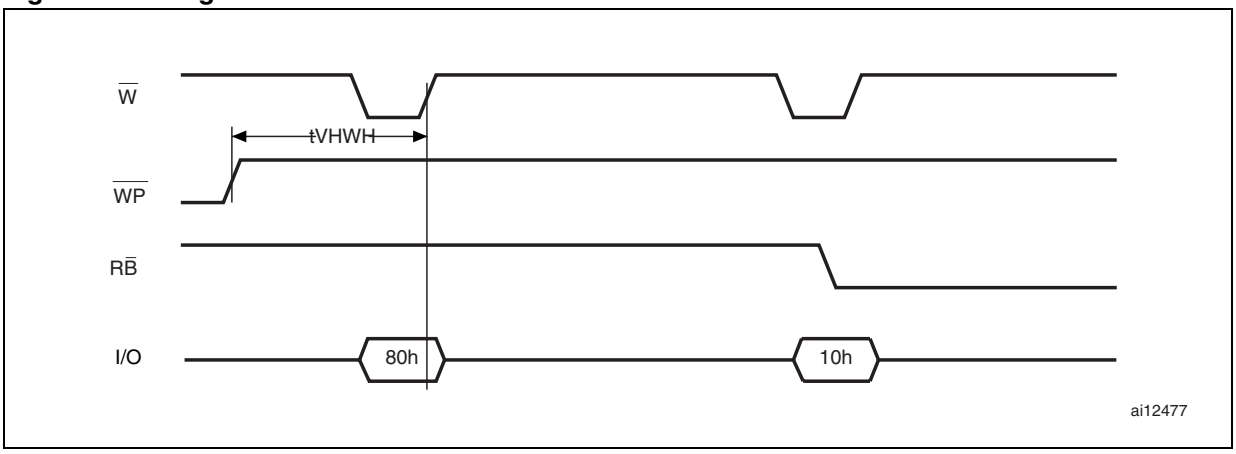


Figure 39. Program/erase disable waveform

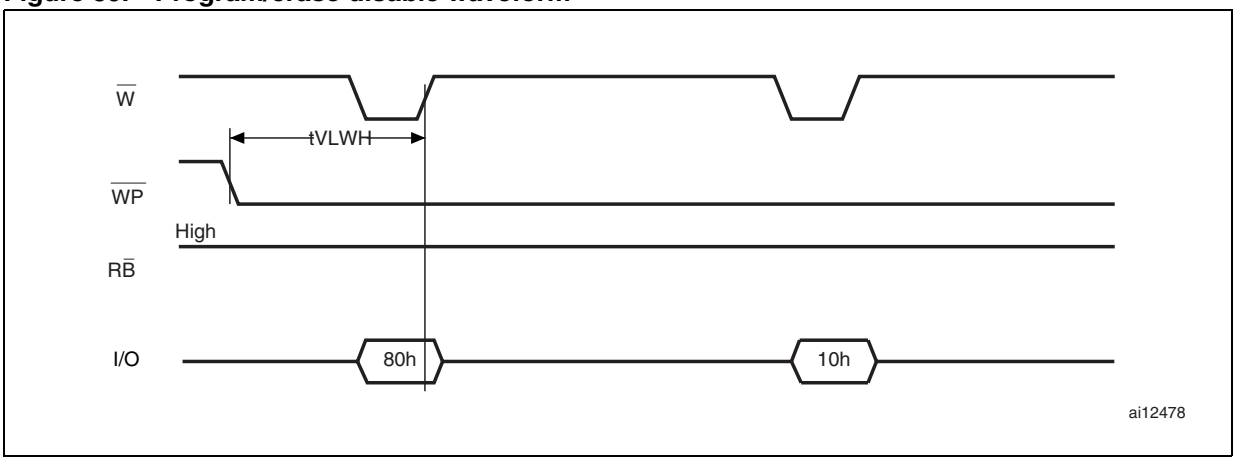
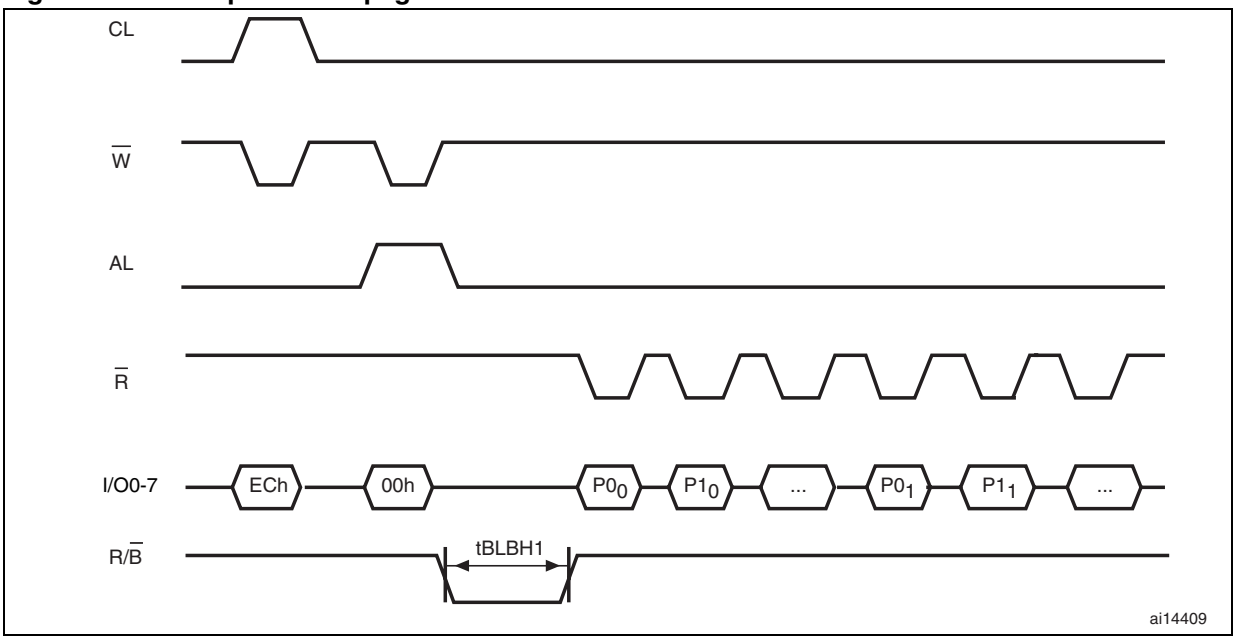


Figure 40. Read parameter page waveform



12.1 Ready/Busy signal electrical characteristics

Figure 42, *Figure 41* and *Figure 43* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

This is an example for 3 V devices:

$$R_P min = \frac{3{,}2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 41. Ready/Busy AC waveform

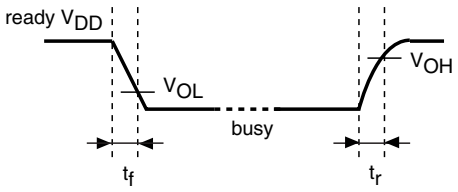


Figure 42. Ready/Busy load circuit

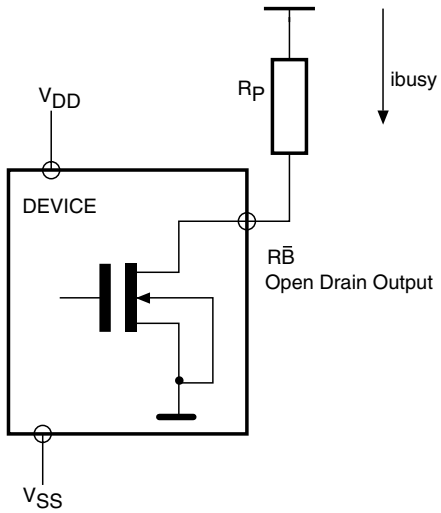
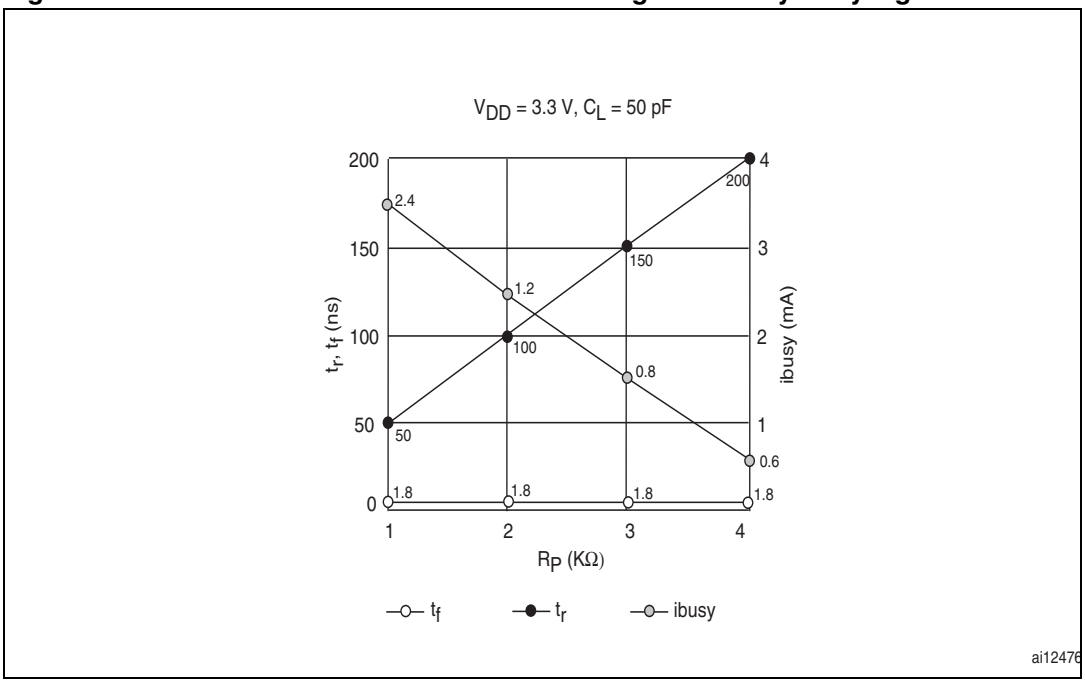


Figure 43. Resistor value versus waveform timings for Ready/Busy signal



1. T = 25°C.

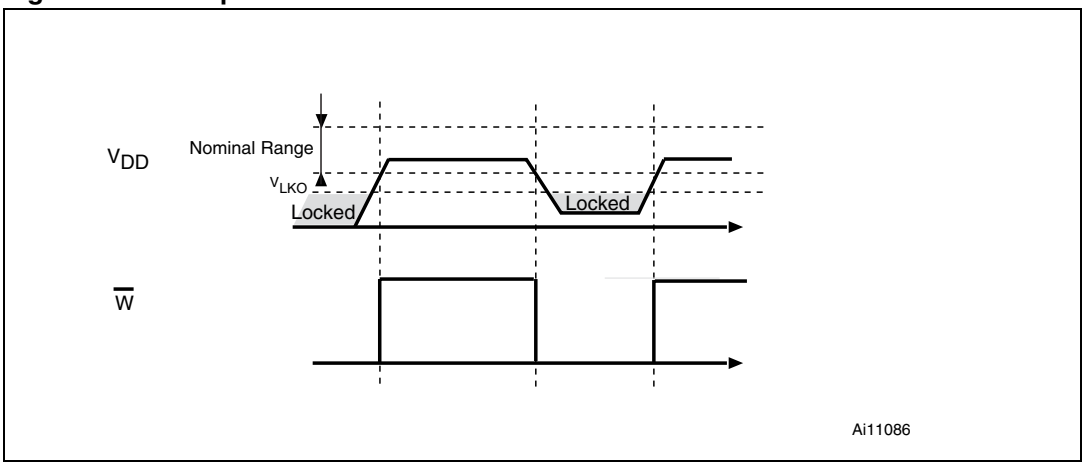
12.2 Data protection

The Numonyx NAND devices aredesigned to guarantee data protection during power transitions.

A V_{DD} detection circuit disables all NAND operations, if V_{DD} is below the V_{LKO} threshold.

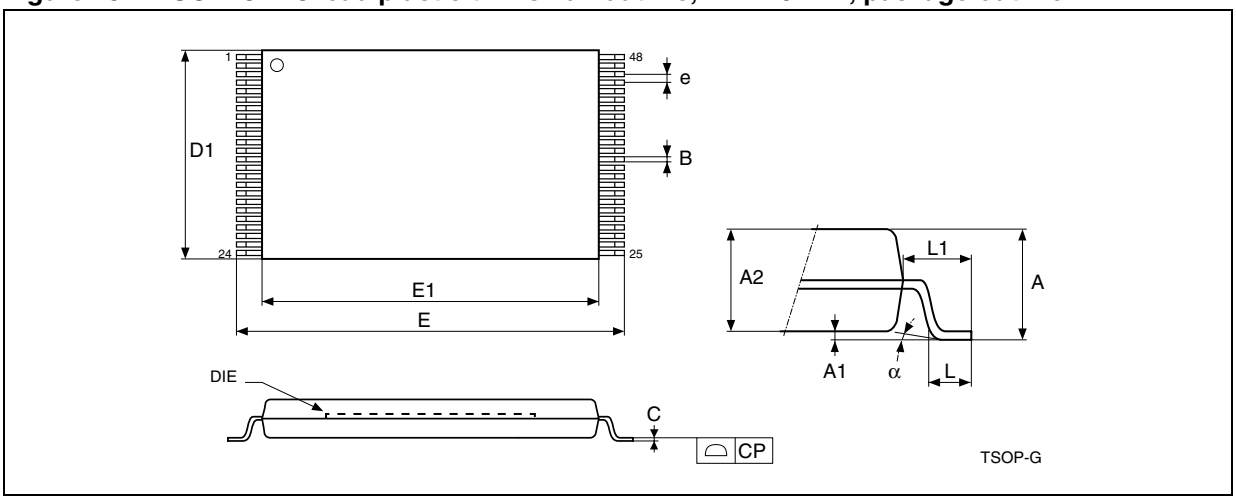
In the V_{DD} range from V_{LKO} to the lower limit of nominal range, the $\overline{WP}$ pin should be kept low (V_{IL}) to guarantee hardware protection during power transitions as shown in the below figure.

Figure 44. Data protection



13 Package mechanical

Figure 45. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package outline



1. Drawing is not to scale.

Table 32. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.080			0.0031
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800			0.0315		
a	3°	0°	5°	3°	0°	5°

Figure 46. LGA52 12 x 17 mm, 1 mm pitch, package outline

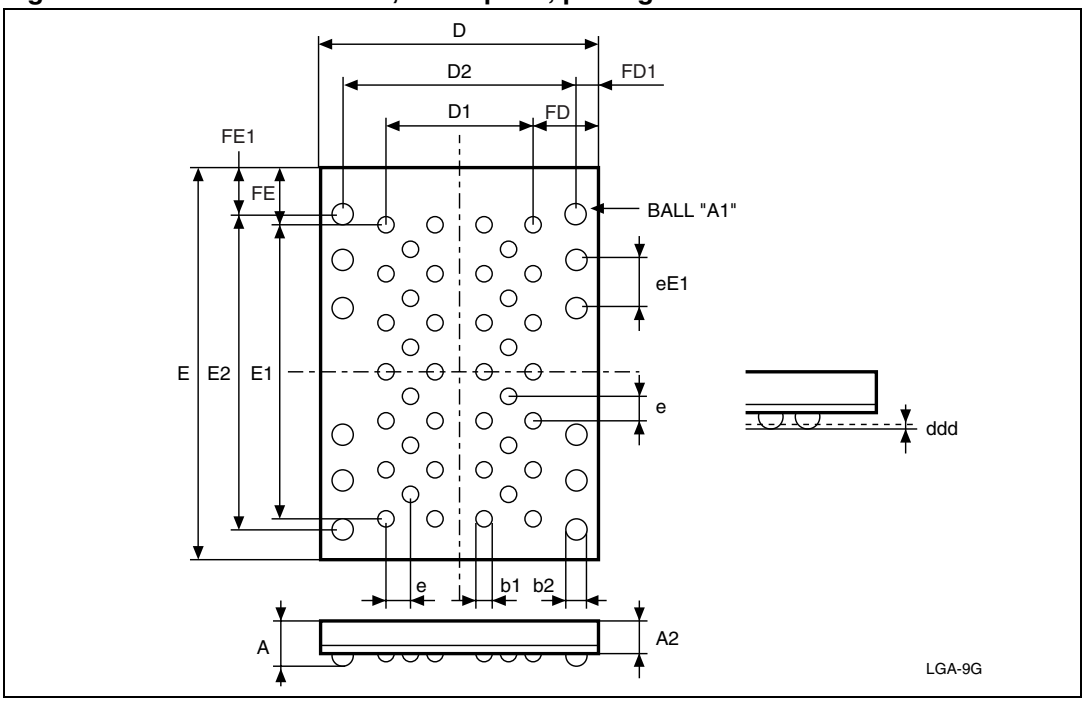


Table 33. LGA52 12 x 17 mm, 1 mm pitch, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			0.650			0.0256
A2			0.650			0.0256
b1	0.700	0.650	0.750	0.0276	0.0256	0.0295
b2	1.000	0.950	1.050	0.0394	0.0374	0.0413
D	12.000	11.900	12.100	0.4724	0.4685	0.4764
D1	6.000			0.2362		
D2	10.000			0.3937		
ddd			0.100			0.0039
E	17.000	16.900	17.100	0.6693	0.6654	0.6732
E1	12.000			0.4724		
E2	13.000			0.5118		
e	1.000	–	–	0.0394	–	–
eE1	2.000	–	–	0.0787	–	–
FD	3.000			0.1181		
FD1	1.000			0.0394		
FE	2.500			0.0984		
FE1	2.000			0.0787		

14 Part numbering

Table 34. Ordering information scheme

Example: NAND04GW3B2D N 6 E

Device type

NAND Flash memory

Density

04 G = 4 Gb

08 G = 8 Gb

Operating voltage

W = V_{DD} = 2.7 to 3.6 V

R = V_{DD} = 1.7 to 1.95 V

Bus width

3 = x8

4 = x16(1)

Family identifier

B = 2112 byte page

Device options

2 = Chip Enable ‘don't care’ enabled

4 = Chip Enable ‘don’t care’ enabled with dual interface

Product version

C= Third version (NAND08G-BxC)

D = Fourth version (NAND04G-B2D)

Package

N = TSOP48 12 x 20 mm

ZL = LGA52 12 x 17 mm

Temperature range

1 = 0 to 70 °C

6 = –40 to 85 °C

Option

E = ECOPACK package, standard packing

F = ECOPACK package, tape and reel packing

1. x16 organization only available for MCP products

Devices are shipped from the factory with the memory content bits, in valid blocks, erased to ’1’. For further information on any aspect of this device, please contact your nearest Numonyx Sales Office.

15 Revision history

Table 35. Document revision history

Date	Revision	Changes
22-June-2007	1	Initial release.
17-Sep-2007	2	Added the part numbers NAND08GR3B4C, NAND08GW3B4C, therefore referring to the 8 Gbit devices as the NAND08G-BxC. Modified all data throughout this document to reflect the addition of these part numbers, namely: – *Table 1*, *Table 2*, *Table 6*, and *Table 34*. – Added *Figure 5: LGA52 connections for the NAND08G-B4C devices*. Changed V_{LKO} value in *Table 28* from 1.1 to 1.2.
10-Dec-2007	3	Applied Numonyx branding.

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