# EN29LV320A
# 32 Megabit (4096K x 8-bit / 2048K x 16-bit) Flash Memory Boot Sector Flash Memory, CMOS 3.0 Volt-only

## FEATURES

- Single power supply operation
- Full voltage range: 2.7 to 3.6 volts read and write operations

- High performance
- Access times as fast as 70 ns

- Low power consumption (typical values at 5 MHz)
- 9 mA typical active read current
- 20 mA typical program/erase current
- Less than 1 μA current in standby or automatic sleep mode.

- Flexible Sector Architecture:
- Eight 8-Kbyte sectors, sixty-three 64k-byte sectors.
- 8-Kbyte sectors for Top or Bottom boot.
- Sector/Sector Group protection:
  Hardware locking of sectors to prevent program or erase operations within individual sectors
  Additionally, temporary Sector Group Unprotect allows code changes in previously locked sectors.

- High performance program/erase speed
- Word program time: 8μs typical
- Sector erase time: 500ms typical
- Chip erase time: 70s typical

- JEDEC Standard compatible

- Standard DATA# polling and toggle bits feature

- Unlock Bypass Program command supported

- Erase Suspend / Resume modes:
  Read and program another Sector during Erase Suspend Mode

- Support JEDEC Common Flash Interface (CFI).

- Low Vcc write inhibit ≤ 2.5V

- Minimum 100K program/erase endurance cycles.

- RESET# hardware reset pin
- Hardware method to reset the device to read mode.

- WP#/ACC input pin
- Write Protect (WP#) function allows protection of outermost two boot sectors, regardless of sector protect status
- Acceleration (ACC) function provides accelerated program times

- Package Options
- 48-pin TSOP (Type 1)
- 48 ball 6mm x 8mm FBGA

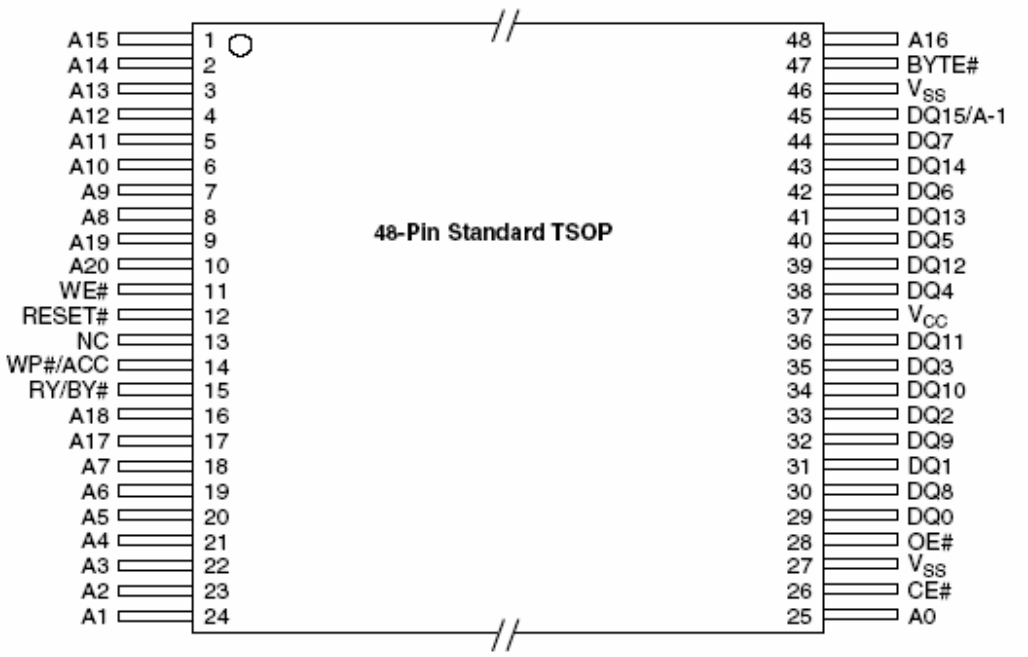
- Commercial and Industrial Temperature Range.

## GENERAL DESCRIPTION

The EN29LV320A is a 32-Megabit, electrically erasable, read/write non-volatile flash memory, organized as 4,194,304 bytes or 2.097,152 words. Any word can be programmed typically in 8μs. The EN29LV320A features 3.0V voltage read and write operation, with access times as fast as 70ns to eliminate the need for WAIT states in high-performance microprocessor systems.

The EN29LV320A has separate Output Enable (OE#), Chip Enable (CE#), and Write Enable (WE#) controls, which eliminate bus contention issues. This device is designed to allow either single Sector or full Chip erase operation, where each Sector can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each Sector.

## CONNECTION DIAGRAMS




**FBGA**

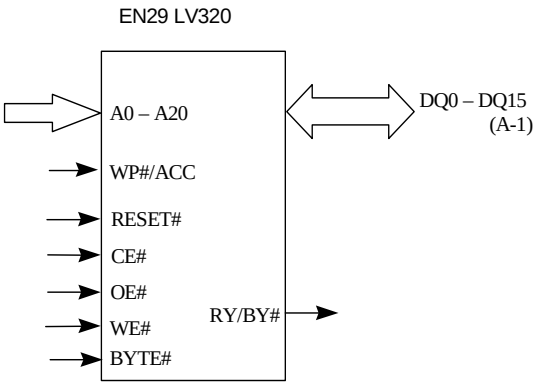
**Top View, Balls Facing Down**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A6 | B6 | C6 | D6 | E6 | F6 | G6 | H6 |
| A13 | A12 | A14 | A15 | A16 | BYTE# | DQ15/A-1 | Vss |
| A5 | B5 | C5 | D5 | E5 | F5 | G5 | H5 |
| A9 | A8 | A10 | A11 | DQ7 | DQ14 | DQ13 | DQ6 |
| A4 | B4 | C4 | D4 | E4 | F4 | G4 | H4 |
| WE# | RESET# | NC | A19 | DQ5 | DQ12 | Vcc | DQ4 |
| A3 | B3 | C3 | D3 | E3 | F3 | G3 | H3 |
| RY/BY# | WP# /ACC | A18 | A20 | DQ2 | DQ10 | DQ11 | DQ3 |
| A2 | B2 | C2 | D2 | E2 | F2 | G2 | H2 |
| A7 | A17 | A6 | A5 | DQ0 | DQ8 | DQ9 | DQ1 |
| A1 | B1 | C1 | D1 | E1 | F1 | G1 | H1 |
| A3 | A4 | A2 | A1 | A0 | CE# | OE# | Vss |

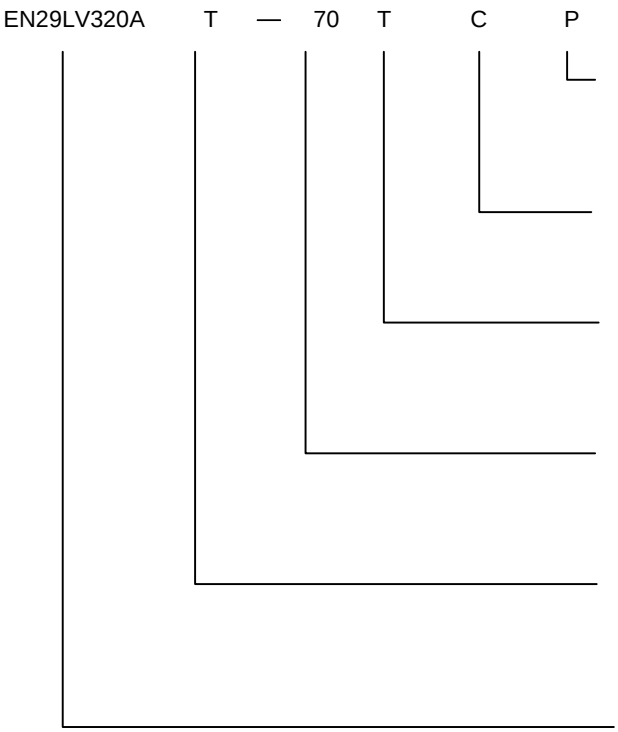
## TABLE 1. PIN DESCRIPTION

| Pin Name | Function |
|---|---|
| A0-A20 | 21 Address inputs |
| DQ0-DQ14 | 15 Data Inputs/Outputs |
| DQ15 / A-1 | DQ15 (data input/output, in word mode), A-1 (LSB address input, in byte mode) |
| CE# | Chip Enable |
| OE# | Output Enable |
| WE# | Write Enable |
| WP#/ACC | Write Protect / Acceleration Pin |
| RESET# | Hardware Reset Pin |
| BYTE# | Byte/Word mode selection |
| RY/BY# | Ready/Busy Output |
| Vcc | Supply Voltage (2.7-3.6V) |
| Vss | Ground |
| NC | Not Connected to anything |

## LOGIC DIAGRAM



## ORDERING INFORMATION




**PACKAGING CONTENT**
(Blank) = Conventional
P = Pb Free

**TEMPERATURE RANGE**
C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

**PACKAGE**
T = 48-pin TSOP
B = 48-Ball Fine Pitch Ball Grid Array (FBGA)
0.80mm pitch, 6mm x 8mm package

**SPEED**
70 = 70ns
90 = 90ns

**BOOT CODE SECTOR ARCHITECTURE**
T = Top boot Sector
B = Bottom boot Sector

**BASE PART NUMBER**
EN = EON Silicon Solution Inc.
29LV = FLASH, 3V Read, Program and Erase
320A = 32 Megabit (4M x 8 / 2M x 16)

## Table 2A. Top Boot Sector Address Tables (EN29LV320AT)

| Sector | A20 – A12 | Sector Size (Kbytes / Kwords) | Address Range (h) Byte mode (x8) | Address Range (h) Word Mode (x16) |
|---|---|---|---|---|
| SA0 | 000000xxx | 64/32 | 000000–00FFFF | 000000–007FFF |
| SA1 | 000001xxx | 64/32 | 010000–01FFFF | 008000–00FFFF |
| SA2 | 000010xxx | 64/32 | 020000–02FFFF | 010000–017FFF |
| SA3 | 000011xxx | 64/32 | 030000–03FFFF | 018000–01FFFF |
| SA4 | 000100xxx | 64/32 | 040000–04FFFF | 020000–027FFF |
| SA5 | 000101xxx | 64/32 | 050000–05FFFF | 028000–02FFFF |
| SA6 | 000110xxx | 64/32 | 060000–06FFFF | 030000–037FFF |
| SA7 | 000111xxx | 64/32 | 070000–07FFFF | 038000–03FFFF |
| SA8 | 001000xxx | 64/32 | 080000–08FFFF | 040000–047FFF |
| SA9 | 001001xxx | 64/32 | 090000–09FFFF | 048000–04FFFF |
| SA10 | 001010xxx | 64/32 | 0A0000–0AFFFF | 050000–057FFF |
| SA11 | 001011xxx | 64/32 | 0B0000–0BFFFF | 058000–05FFFF |
| SA12 | 001100xxx | 64/32 | 0C0000–0CFFFF | 060000–067FFF |
| SA13 | 001101xxx | 64/32 | 0D0000–0DFFFF | 068000–06FFFF |
| SA14 | 001110xxx | 64/32 | 0E0000–0EFFFF | 070000–077FFF |
| SA15 | 001111xxx | 64/32 | 0F0000–0FFFFF | 078000–07FFFF |
| SA16 | 010000xxx | 64/32 | 100000–10FFFF | 080000–087FFF |
| SA17 | 010001xxx | 64/32 | 110000–11FFFF | 088000–08FFFF |
| SA18 | 010010xxx | 64/32 | 120000–12FFFF | 090000–097FFF |
| SA19 | 010011xxx | 64/32 | 130000–13FFFF | 098000–09FFFF |
| SA20 | 010100xxx | 64/32 | 140000–14FFFF | 0A0000–0A7FFF |
| SA21 | 010101xxx | 64/32 | 150000–15FFFF | 0A8000–0AFFFF |
| SA22 | 010110xxx | 64/32 | 160000–16FFFF | 0B0000–0B7FFF |
| SA23 | 010111xxx | 64/32 | 170000–17FFFF | 0B8000–0BFFFF |
| SA24 | 011000xxx | 64/32 | 180000–18FFFF | 0C0000–0C7FFF |
| SA25 | 011001xxx | 64/32 | 190000–19FFFF | 0C8000–0CFFFF |
| SA26 | 011010xxx | 64/32 | 1A0000–1AFFFF | 0D0000–0D7FFF |
| SA27 | 011011xxx | 64/32 | 1B0000–1BFFFF | 0D8000–0DFFFF |
| SA28 | 011100xxx | 64/32 | 1C0000–1CFFFF | 0E0000–0E7FFF |
| SA29 | 011101xxx | 64/32 | 1D0000–1DFFFF | 0E8000–0EFFFF |
| SA30 | 011110xxx | 64/32 | 1E0000–1EFFFF | 0F0000–0F7FFF |
| SA31 | 011111xxx | 64/32 | 1F0000–1FFFFF | 0F8000–0FFFFF |
| SA32 | 100000xxx | 64/32 | 200000–20FFFF | 100000–107FFF |
| SA33 | 100001xxx | 64/32 | 210000–21FFFF | 108000–10FFFF |
| SA34 | 100010xxx | 64/32 | 220000–22FFFF | 110000–117FFF |
| SA35 | 100011xxx | 64/32 | 230000–23FFFF | 118000–11FFFF |
| SA36 | 100100xxx | 64/32 | 240000–24FFFF | 120000–127FFF |
| SA37 | 100101xxx | 64/32 | 250000–25FFFF | 128000–12FFFF |

| | | | | |
|---|---|---|---|---|
| SA38 | 100110xxx | 64/32 | 260000–26FFFF | 130000–137FFF |
| SA39 | 100111xxx | 64/32 | 270000–27FFFF | 138000–13FFFF |
| SA40 | 101000xxx | 64/32 | 280000–28FFFF | 140000–147FFF |
| SA41 | 101001xxx | 64/32 | 290000–29FFFF | 148000–14FFFF |
| SA42 | 101010xxx | 64/32 | 2A0000–2AFFFF | 150000–157FFF |
| SA43 | 101011xxx | 64/32 | 2B0000–2BFFFF | 158000–15FFFF |
| SA44 | 101100xxx | 64/32 | 2C0000–2CFFFF | 160000–167FFF |
| SA45 | 101101xxx | 64/32 | 2D0000–2DFFFF | 168000–16FFFF |
| SA46 | 101110xxx | 64/32 | 2E0000–2EFFFF | 170000–177FFF |
| SA47 | 101111xxx | 64/32 | 2F0000–2FFFFF | 178000–17FFFF |
| SA48 | 110000xxx | 64/32 | 300000–30FFFF | 180000–187FFF |
| SA49 | 110001xxx | 64/32 | 310000–31FFFF | 188000–18FFFF |
| SA50 | 110010xxx | 64/32 | 320000–32FFFF | 190000–197FFF |
| SA51 | 110011xxx | 64/32 | 330000–33FFFF | 198000–19FFFF |
| SA52 | 110100xxx | 64/32 | 340000–34FFFF | 1A0000–1A7FFF |
| SA53 | 110101xxx | 64/32 | 350000–35FFFF | 1A8000–1AFFFF |
| SA54 | 110110xxx | 64/32 | 360000–36FFFF | 1B0000–1B7FFF |
| SA55 | 110111xxx | 64/32 | 370000–37FFFF | 1B8000–1BFFFF |
| SA56 | 111000xxx | 64/32 | 380000–38FFFF | 1C0000–1C7FFF |
| SA57 | 111001xxx | 64/32 | 390000–39FFFF | 1C8000–1CFFFF |
| SA58 | 111010xxx | 64/32 | 3A0000–3AFFFF | 1D0000–1D7FFF |
| SA59 | 111011xxx | 64/32 | 3B0000–3BFFFF | 1D8000–1DFFFF |
| SA60 | 111100xxx | 64/32 | 3C0000–3CFFFF | 1E0000–1E7FFF |
| SA61 | 111101xxx | 64/32 | 3D0000–3DFFFF | 1E8000–1EFFFF |
| SA62 | 111110xxx | 64/32 | 3E0000–3EFFFF | 1F0000–1F7FFF |
| SA63 | 111111000 | 8/4 | 3F0000–3F1FFF | 1F8000–1F8FFF |
| SA64 | 111111001 | 8/4 | 3F2000–3F3FFF | 1F9000–1F9FFF |
| SA65 | 111111010 | 8/4 | 3F4000–3F5FFF | 1FA000–1FAFFF |
| SA66 | 111111011 | 8/4 | 3F6000–3F7FFF | 1FB000–1FBFFF |
| SA67 | 111111100 | 8/4 | 3F8000–3F9FFF | 1FC000–1FCFFF |
| SA68 | 111111101 | 8/4 | 3FA000–3FBFFF | 1FD000–1FDFFF |
| SA69 | 111111110 | 8/4 | 3FC000–3FDFFF | 1FE000–1FEFFF |
| SA70 | 111111111 | 8/4 | 3FE000–3FFFFF | 1FF000–1FFFFF |

Note: The address bus is A20:A-1 in byte mode where BYTE# = $V_{IL}$ or A20:A0 in word mode where BYTE# = $V_{IH}$

## Table 2B. Bottom Boot Sector Address Tables (EN29LV320AB)

| Sector | A20 – A12 | Sector Size (Kbytes / Kwords) | Address Range (h) Byte mode (x8) | Address Range (h) Word Mode (x16) |
|---|---|---|---|---|
| SA0 | 000000000 | 8/4 | 000000–001FFF | 000000–000FFF |
| SA1 | 000000001 | 8/4 | 002000–003FFF | 001000–001FFF |
| SA2 | 000000010 | 8/4 | 004000–005FFF | 002000–002FFF |
| SA3 | 000000011 | 8/4 | 006000–007FFF | 003000–003FFF |
| SA4 | 000000100 | 8/4 | 008000–009FFF | 004000–004FFF |
| SA5 | 000000101 | 8/4 | 00A000–00BFFF | 005000–005FFF |
| SA6 | 000000110 | 8/4 | 00C000–00DFFF | 006000–006FFF |
| SA7 | 000000111 | 8/4 | 00E000–00FFFF | 007000–007FFF |
| SA8 | 000001xxx | 64/32 | 010000–01FFFF | 008000–00FFFF |
| SA9 | 000010xxx | 64/32 | 020000–02FFFF | 010000–017FFF |
| SA10 | 000011xxx | 64/32 | 030000–03FFFF | 018000–01FFFF |
| SA11 | 000100xxx | 64/32 | 040000–04FFFF | 020000–027FFF |
| SA12 | 000101xxx | 64/32 | 050000–05FFFF | 028000–02FFFF |
| SA13 | 000110xxx | 64/32 | 060000–06FFFF | 030000–037FFF |
| SA14 | 000111xxx | 64/32 | 070000–07FFFF | 038000–03FFFF |
| SA15 | 001000xxx | 64/32 | 080000–08FFFF | 040000–047FFF |
| SA16 | 001001xxx | 64/32 | 090000–09FFFF | 048000–04FFFF |
| SA17 | 001010xxx | 64/32 | 0A0000–0AFFFF | 050000–057FFF |
| SA18 | 001011xxx | 64/32 | 0B0000–0BFFFF | 058000–05FFFF |
| SA19 | 001100xxx | 64/32 | 0C0000–0CFFFF | 060000–067FFF |
| SA20 | 001101xxx | 64/32 | 0D0000–0DFFFF | 068000–06FFFF |
| SA21 | 001110xxx | 64/32 | 0E0000–0EFFFF | 070000–077FFF |
| SA22 | 001111xxx | 64/32 | 0F0000–0FFFFF | 078000–07FFFF |
| SA23 | 010000xxx | 64/32 | 100000–10FFFF | 080000–087FFF |
| SA24 | 010001xxx | 64/32 | 110000–11FFFF | 088000–08FFFF |
| SA25 | 010010xxx | 64/32 | 120000–12FFFF | 090000–097FFF |
| SA26 | 010011xxx | 64/32 | 130000–13FFFF | 098000–09FFFF |
| SA27 | 010100xxx | 64/32 | 140000–14FFFF | 0A0000–0A7FFF |
| SA28 | 010101xxx | 64/32 | 150000–15FFFF | 0A8000–0AFFFF |
| SA29 | 010110xxx | 64/32 | 160000–16FFFF | 0B0000–0B7FFF |
| SA30 | 010111xxx | 64/32 | 170000–17FFFF | 0B8000–0BFFFF |
| SA31 | 011000xxx | 64/32 | 180000–18FFFF | 0C0000–0C7FFF |
| SA32 | 011001xxx | 64/32 | 190000–19FFFF | 0C8000–0CFFFF |
| SA33 | 011010xxx | 64/32 | 1A0000–1AFFFF | 0D0000–0D7FFF |
| SA34 | 011011xxx | 64/32 | 1B0000–1BFFFF | 0D8000–0DFFFF |
| SA35 | 011100xxx | 64/32 | 1C0000–1CFFFF | 0E0000–0E7FFF |
| SA36 | 011101xxx | 64/32 | 1D0000–1DFFFF | 0E8000–0EFFFF |
| SA37 | 011110xxx | 64/32 | 1E0000–1EFFFF | 0F0000–0F7FFF |
| SA38 | 011111xxx | 64/32 | 1F0000–1FFFFF | 0F8000–0FFFFF |

| | | | | |
|---|---|---|---|---|
| SA39 | 100000xxx | 64/32 | 200000–20FFFF | 100000–107FFF |
| SA40 | 100001xxx | 64/32 | 210000–21FFFF | 108000–10FFFF |
| SA41 | 100010xxx | 64/32 | 220000–22FFFF | 110000–117FFF |
| SA42 | 100011xxx | 64/32 | 230000–23FFFF | 118000–11FFFF |
| SA43 | 100100xxx | 64/32 | 240000–24FFFF | 120000–127FFF |
| SA44 | 100101xxx | 64/32 | 250000–25FFFF | 128000–12FFFF |
| SA45 | 100110xxx | 64/32 | 260000–26FFFF | 130000–137FFF |
| SA46 | 100111xxx | 64/32 | 270000–27FFFF | 138000–13FFFF |
| SA47 | 101000xxx | 64/32 | 280000–28FFFF | 140000–147FFF |
| SA48 | 101001xxx | 64/32 | 290000–29FFFF | 148000–14FFFF |
| SA49 | 101010xxx | 64/32 | 2A0000–2AFFFF | 150000–157FFF |
| SA50 | 101011xxx | 64/32 | 2B0000–2BFFFF | 158000–15FFFF |
| SA51 | 101100xxx | 64/32 | 2C0000–2CFFFF | 160000–167FFF |
| SA52 | 101101xxx | 64/32 | 2D0000–2DFFFF | 168000–16FFFF |
| SA53 | 101110xxx | 64/32 | 2E0000–2EFFFF | 170000–177FFF |
| SA54 | 101111xxx | 64/32 | 2F0000–2FFFFF | 178000–17FFFF |
| SA55 | 110000xxx | 64/32 | 300000–30FFFF | 180000–187FFF |
| SA56 | 110001xxx | 64/32 | 310000–31FFFF | 188000–18FFFF |
| SA57 | 110010xxx | 64/32 | 320000–32FFFF | 190000–197FFF |
| SA58 | 110011xxx | 64/32 | 330000–33FFFF | 198000–19FFFF |
| SA59 | 110100xxx | 64/32 | 340000–34FFFF | 1A0000–1A7FFF |
| SA60 | 110101xxx | 64/32 | 350000–35FFFF | 1A8000–1AFFFF |
| SA61 | 110110xxx | 64/32 | 360000–36FFFF | 1B0000–1B7FFF |
| SA62 | 110111xxx | 64/32 | 370000–37FFFF | 1B8000–1BFFFF |
| SA63 | 111000xxx | 64/32 | 380000–38FFFF | 1C0000–1C7FFF |
| SA64 | 111001xxx | 64/32 | 390000–39FFFF | 1C8000–1CFFFF |
| SA65 | 111010xxx | 64/32 | 3A0000–3AFFFF | 1D0000–1D7FFF |
| SA66 | 111011xxx | 64/32 | 3B0000–3BFFFF | 1D8000–1DFFFF |
| SA67 | 111100xxx | 64/32 | 3C0000–3CFFFF | 1E0000–1E7FFF |
| SA68 | 111101xxx | 64/32 | 3D0000–3DFFFF | 1E8000–1EFFFF |
| SA69 | 111110xxx | 64/32 | 3E0000–3EFFFF | 1F0000–1F7FFF |
| SA70 | 111111xxx | 64/32 | 3F0000–3FFFFF | 1F8000–1FFFFF |

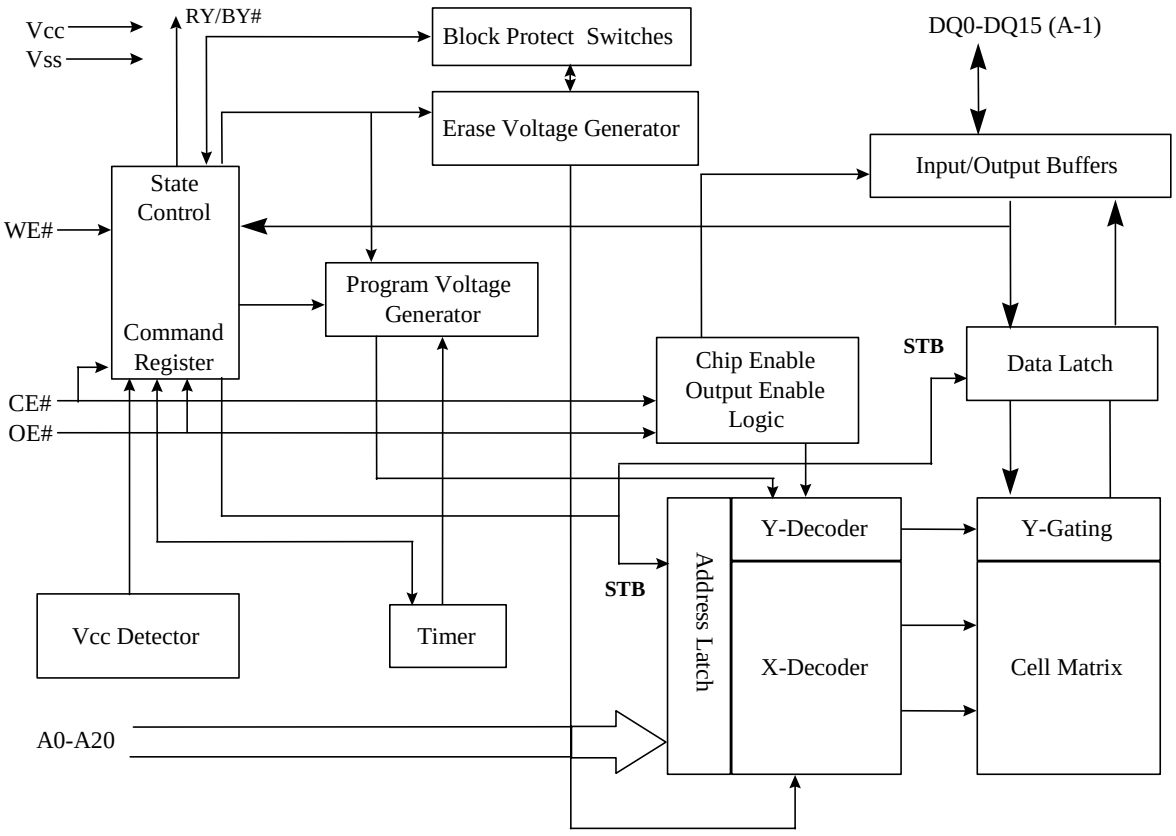
Note: The address bus is A20:A-1 in byte mode where BYTE# = $V_{IL}$ or A20:A0 in word mode where BYTE# = $V_{IH}$

## PRODUCT SELECTOR GUIDE

| Product Number | EN29LV320A | |
|---|---|---|
| Speed Option | **-70** | **-90** |
| Max Access Time, ns ($t_{acc}$) | 70 | 90 |
| Max CE# Access, ns ($t_{ce}$) | 70 | 90 |
| Max OE# Access, ns ($t_{oe}$) | 30 | 35 |

**Notes:**
1. Vcc=3.0 – 3.6 V for 70ns read operation

## BLOCK DIAGRAM



## TABLE 3. OPERATING MODES

### 32M FLASH USER MODE TABLE

| Operation | CE# | OE# | WE# | RESET # | WP#/ACC | A0-A20 | DQ0-DQ7 | DQ8-DQ15 | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | BYTE# = $V_{IH}$ | BYTE# = $V_{IL}$ |
| Read | L | L | H | H | L/H | $A_{IN}$ | $D_{OUT}$ | $D_{OUT}$ | DQ8-DQ14= High-Z, DQ15 = A-1 |
| Write | L | H | L | H | (Note 1) | $A_{IN}$ | $D_{IN}$ | $D_{IN}$ | |
| Accelerated Program | L | H | L | H | $V_{HH}$ | $A_{IN}$ | $D_{IN}$ | $D_{IN}$ | |
| CMOS Standby | $V_{cc}$ ± 0.3V | X | X | $V_{cc}$ ± 0.3V | H | X | High-Z | High-Z | High-Z |
| TTL Standby | H | X | X | H | H | X | High-Z | High-Z | High-Z |
| Output Disable | L | H | H | H | L/H | X | High-Z | High-Z | High-Z |
| Hardware Reset | X | X | X | L | L/H | X | High-Z | High-Z | High-Z |
| Sector (Group) Protect | L | H | L | $V_{ID}$ | L/H | SA, A6=L, A1=H, A0=L | (Note 2) | X | X |
| Sector Unprotect | L | H | L | $V_{ID}$ | (Note 1) | SA, A6=H, A1=H, A0=L | (Note 2) | X | X |
| Temporary Sector Unprotect | X | X | X | $V_{ID}$ | (Note 1) | $A_{IN}$ | (Note 2) | (Note 2) | High-Z |

L=logic low= $V_{IL}$, H=Logic High= $V_{IH}$, $V_{ID}$ =$V_{HH}$ =11 ± 0.5V = 10.5-11.5V, X=Don't Care (either L or H, but not floating ), SA=Sector Addresses, $D_{IN}$=Data In, $D_{OUT}$=Data Out, $A_{IN}$=Address In

**Notes:**

1. If WP#/ACC = $V_{IL}$ , the two outermost boot sectors remain protected. If WP# / ACC = $V_{IH}$, the outermost boot sector protection depends on whether they were last protected or unprotected. If WP#/ACC = $V_{HH}$, all sectors will be unprotected.

2. Please refer to "Sector/Sector Group Protection & Chip Unprotection", Flowchart 7a and Flowchart 7b.

## TABLE 4. Autoselect Codes (Using High Voltage, $V_{ID}$)

### 32M FLASH MANUFACTURER/DEVICE ID TABLE

| Description | | CE# | OE# | WE# | A20 to A12 | A11 to A10 | A9[2] | A8 | A7 | A6 | A5 to A2 | A1 | A0 | DQ8 to DQ15 | DQ7 to DQ0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer ID: Eon | | L | L | H | X | X | $V_{ID}$ | H[1] | X | L | X | L | L | X | 1Ch |
| | | | | | | | | L | | | | | | | 7Fh |
| Device ID (top boot sector) | Word | L | L | H | X | X | $V_{ID}$ | X | X | L | X | L | H | 22h | F6h |
| | Byte | L | L | H | | | | | | | | | | X | F6h |
| Device ID (bottom boot sector) | Word | L | L | H | X | X | $V_{ID}$ | X | X | L | X | L | H | 22h | F9h |
| | Byte | L | L | H | | | | | | | | | | X | F9h |
| Sector Protection Verification | | L | L | H | SA | X | $V_{ID}$ | X | X | L | X | H | L | X | 01h (Protected) |
| | | | | | | | | | | | | | | X | 00h (Unprotected) |

L=logic low= $V_{IL}$, H=Logic High= $V_{IH}$, $V_{ID}$ =11 ± 0.5V, X=Don't Care (either L or H, but not floating!), SA=Sector Addresses

**Note:**

1. A8=H is recommended for Manufacturing ID check. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh.
2. A9 = $V_{ID}$ is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.

# USER MODE DEFINITIONS

## Word / Byte Configuration

The signal set on the BYTE# pin controls whether the device data I/O pins DQ15-DQ0 operate in the byte or word configuration. When the BYTE# Pin is set at logic '1', then the device is in word configuration, DQ15-DQ0 are active and are controlled by CE# and OE#.

On the other hand, if the BYTE# Pin is set at logic '0', then the device is in byte configuration, and only data I/O pins DQ0-DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

## Standby Mode

The EN29LV320A has a CMOS-compatible standby mode, which reduces the current to $< 1\mu A$ (typical). It is placed in CMOS-compatible standby when the CE# pin is at $V_{CC} \pm 0.5$. RESET# and BYTE# pin must also be at CMOS input levels. The device also has a TTL-compatible standby mode, which reduces the maximum $V_{CC}$ current to < 1mA. It is placed in TTL-compatible standby when the CE# pin is at $V_{IH}$. When in standby modes, the outputs are in a high-impedance state independent of the OE# input.

## Automatic Sleep Mode

The EN29LV320A has a automatic sleep mode, which minimizes power consumption. The devices will enter this mode automatically when the states of address bus remain stable for $t_{acc}$ + 30ns. $ICC_4$ in the DC Characteristics table shows the current specification. With standard access times, the device will output new data when addresses change.

## Read Mode

The device is automatically set to reading array data after device power-up or hardware reset. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm

After the device accepts an Sector Erase Suspend command, the device enters the Sector Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Sector Erase Suspend mode, the system may once again read array data with the same exception. See "Sector Erase Suspend/Resume Commands" for more additional information.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high or while in the autoselect mode. See the "Reset Command" for additional details.

## Output Disable Mode

When the OE# pin is at a logic high level ($V_{IH}$), the output from the EN29LV320A is disabled. The output pins are placed in a high impedance state.

## Autoselect Identification Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires $V_{ID}$ (10.5 V to 11.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes table. In addition, when verifying

sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The “Command Definitions” table shows the remaining address bits that are don’t-care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0.

To access the autoselect codes in-system; the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require $V_{ID}$. See “Command Definitions” for details on using the autoselect mode.

## Writing Command Sequences

To write a command or command sequence to program data to the device or erase data, the system has to drive WE# and CE# to $V_{IL}$, and OE# to $V_{IH}$.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. An erase operation can erase one sector or the whole chip.

The system can also read the autoselect codes by entering the autoselect mode, which need the autoselect command sequence to be written. Please refer to the “Command Definitions” for all the available commands.

## RESET#: Hardware Reset

When RESET# is driven low for $t_{RP}$, all output pins are tristates. All commands written in the internal state machine are reset to reading array data.

Please refer to timing diagram for RESET# pin in “AC Characteristics”.

## Sector/Sector Group Protection & Chip Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector. The hardware chip unprotection feature re-enables both program and erase operations in previously protected sectors. A sector group implies three or four adjacent sectors that would be protected at the same time. Please see the following tables which show the organization of sector groups.

There are two methods to enable this hardware protection circuitry. The first one requires only that the RESET# pin be at $V_{ID}$ and then standard microprocessor timings can be used to enable or disable this feature. See Flowchart 7a and 7b for the algorithm and Figure. 12 for the timings.
When doing Chip Unprotect, all the unprotected sector groups must be protected prior to any unprotect write cycle.

The second method is for programming equipment. This method requires $V_{ID}$ to be applied to both OE# and A9 pins and non-standard microprocessor timings are used. This method is described in a separate document named EN29LV320A Supplement, which can be obtained by contacting a representative of Eon Silicon Solution, Inc.

## Top Boot Sector/Sector Group Organization Table (EN29LV320AT) for (Un)Protection

| Sector Group | Sectors | A20-A12 | Sector Group Size |
|---|---|---|---|
| SG 0 | SA 0-SA 3 | 0000XXXXX | 64 Kbytes x 4 |
| SG 1 | SA 4-SA 7 | 0001XXXXX | 64 Kbytes x 4 |
| SG 2 | SA 8-SA11 | 0010XXXXX | 64 Kbytes x 4 |
| SG 3 | SA12-SA15 | 0011XXXXX | 64 Kbytes x 4 |
| SG 4 | SA16-SA19 | 0100XXXXX | 64 Kbytes x 4 |
| SG 5 | SA20-SA23 | 0101XXXXX | 64 Kbytes x 4 |
| SG 6 | SA24-SA27 | 0110XXXXX | 64 Kbytes x 4 |
| SG 7 | SA28-SA31 | 0111XXXXX | 64 Kbytes x 4 |
| SG 8 | SA32-SA35 | 1000XXXXX | 64 Kbytes x 4 |
| SG 9 | SA36-SA39 | 1001XXXXX | 64 Kbytes x 4 |
| SG10 | SA40-SA43 | 1010XXXXX | 64 Kbytes x 4 |
| SG11 | SA44-SA47 | 1011XXXXX | 64 Kbytes x 4 |
| SG12 | SA48-SA51 | 1100XXXXX | 64 Kbytes x 4 |
| SG13 | SA52-SA55 | 1101XXXXX | 64 Kbytes x 4 |
| SG14 | SA56-SA59 | 1110XXXXX | 64 Kbytes x 4 |
| SG15 | SA60-SA62 | 111100XXX<br>111101XXX<br>111110XXX | 64 Kbytes x 3 |
| SG16 | SA63 | 111111000 | 8 Kbytes |
| SG17 | SA64 | 111111001 | 8 Kbytes |
| SG18 | SA65 | 111111010 | 8 Kbytes |
| SG19 | SA66 | 111111011 | 8 Kbytes |
| SG20 | SA67 | 111111100 | 8 Kbytes |
| SG21 | SA68 | 111111101 | 8 Kbytes |
| SG22 | SA69 | 111111110 | 8 Kbytes |
| SG23 | SA70 | 111111111 | 8 Kbytes |

## Bottom Boot Sector/Sector Group Organization Table (EN29LV320AB) for (Un)Protection

| Sector Group | Sectors | A20-A12 | Sector Group Size |
|---|---|---|---|
| SG23 | SA70-SA67 | 1111XXXXX | 64 Kbytes x 4 |
| SG22 | SA66-SA63 | 1110XXXXX | 64 Kbytes x 4 |
| SG21 | SA62-SA59 | 1101XXXXX | 64 Kbytes x 4 |
| SG20 | SA58-SA55 | 1100XXXXX | 64 Kbytes x 4 |
| SG19 | SA54-SA51 | 1011XXXXX | 64 Kbytes x 4 |
| SG18 | SA50-SA47 | 1010XXXXX | 64 Kbytes x 4 |
| SG17 | SA46-SA43 | 1001XXXXX | 64 Kbytes x 4 |
| SG16 | SA42-SA39 | 1000XXXXX | 64 Kbytes x 4 |
| SG15 | SA38-SA35 | 0111XXXXX | 64 Kbytes x 4 |
| SG14 | SA34-SA31 | 0110XXXXX | 64 Kbytes x 4 |
| SG13 | SA30-SA27 | 0101XXXXX | 64 Kbytes x 4 |
| SG12 | SA26-SA23 | 0100XXXXX | 64 Kbytes x 4 |
| SG11 | SA22-SA19 | 0011XXXXX | 64 Kbytes x 4 |
| SG10 | SA18-SA15 | 0010XXXXX | 64 Kbytes x 4 |
| SG 9 | SA14-SA11 | 0001XXXXX | 64 Kbytes x 4 |
| SG 8 | SA10-SA 8 | 000011XXX<br>000010XXX<br>000001XXX | 64 Kbytes x 3 |
| SG 7 | SA 7 | 000000111 | 8 Kbytes |
| SG 6 | SA 6 | 000000110 | 8 Kbytes |
| SG 5 | SA 5 | 000000101 | 8 Kbytes |
| SG 4 | SA 4 | 000000100 | 8 Kbytes |
| SG 3 | SA 3 | 000000011 | 8 Kbytes |
| SG 2 | SA 2 | 000000010 | 8 Kbytes |
| SG 1 | SA 1 | 000000001 | 8 Kbytes |
| SG 0 | SA 0 | 000000000 | 8 Kbytes |

## Write Protect / Accelerated Program (WP# / ACC)

The WP#/ACC pin provides two functions. The Write Protect (WP#) function provides a hardware method of protecting the outermost two 8K-byte Boot Sector. The ACC function allows faster manufacturing throughput at the factory, using an external high voltage.

When WP#/ACC is Low, the device protects the outermost tw 8K-byte Boot Sector; no matter the sectors are protected or unprotected using the method described in “Sector/Sector Group Protection & Chip Unprotection”, Program and Erase operations in these sectors are ignored.

When WP#/ACC is High, the device reverts to the previous protection status of the outermost two 8K-byte boot sector. Program and Erase operations can now modify the data in the two outermost 8K-byte Boot Sector unless the sector is protected using Sector Protection.

When WP#/ACC is raised to $V_{HH}$ the memory automatically enters the Unlock Bypass mode(please refer to “Command Definitions”), temporarily unprotects every protected sectors, and reduces the time required for program operation. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. When WP#/ACC returns to $V_{IH}$ or $V_{IL}$, normal operation resumes. The transitions from $V_{IH}$ or $V_{IL}$ to $V_{HH}$ and from $V_{HH}$ to $V_{IH}$ or $V_{IL}$ must be slower than $t_{VHH}$, see Figure 11.

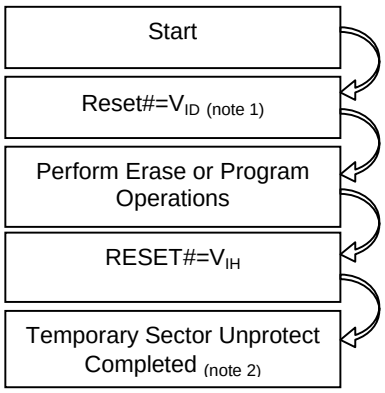
Note that the WP#/ACC pin must not be left floating or unconnected. In addition, WP#/ACC pin must not be at $V_{HH}$ for operations other than accelerated programming. It could cause the device to be damaged.

Never raise this pin to $V_{HH}$ from any mode except Read mode, otherwise the memory may be left in an indeterminate state.

A 0.1µF capacitor should be connected between the WP#/ACC pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program.

## Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data while in-system. The Temporary Sector Unprotect mode is activated by setting the RESET# pin to VBIDB. During this mode, formerly protected sectors can be programmed or erased by simply selecting the sector addresses. Once VBIDB is removed from the RESET# pin, all the previously protected sectors are protected again. See accompanying flowchart and figure 10 for more timing details.




**Notes:**
1. All protected sectors are unprotected. (If WP#/ACC=$V_{IL}$, outermost boot sectors will remain protected.)
2. Previously protected sectors are protected again.

## COMMON FLASH INTERFACE (CFI)

The common flash interface (CFI) specification outlines device and host systems software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data.

The system can read CFI information at the addresses given in Tables 5-8.In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode and the system can read CFI data at the addresses given in Tables 5–8. The system must write the reset command to return the device to the autoselect mode.

## Table 5. CFI Query Identification String

| Addresses (Word Mode) | Adresses (Byte Mode) | Data | Description |
|---|---|---|---|
| 10h<br>11h<br>12h | 20h<br>22h<br>24h | 0051h<br>0052h<br>0059h | Query Unique ASCII string “QRY” |
| 13h<br>14h | 26h<br>28h | 0002h<br>0000h | Primary OEM Command Set |
| 15h<br>16h | 2Ah<br>2Ch | 0040h<br>0000h | Address for Primary Extended Table |
| 17h<br>18h | 2Eh<br>30h | 0000h<br>0000h | Alternate OEM Command set (00h = none exists) |
| 19h<br>1Ah | 32h<br>34h | 0000h<br>0000h | Address for Alternate OEM Extended Table (00h = none exists) |

## Table 6. System Interface String

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|---|---|---|---|
| 1Bh | 36h | 0027h | Vcc Min (write/erase)<br>DQ7-DQ4: volt, DQ3 –DQ0: 100 millivolt |
| 1Ch | 38h | 0036h | Vcc Max (write/erase)<br>DQ7-DQ4: volt, DQ3 –DQ0: 100 millivolt |
| 1Dh | 3Ah | 0000h | Vpp Min. voltage (00h = no Vpp pin present) |
| 1Eh | 3Ch | 0000h | Vpp Max. voltage (00h = no Vpp pin present) |
| 1Fh | 3Eh | 0004h | Typical timeout per single byte/word write $2^N$ µS |
| 20h | 40h | 0000h | Typical timeout for Min, size buffer write $2^N$ µS (00h = not supported) |
| 21h | 42h | 000Ah | Typical timeout per individual block erase $2^N$ ms |
| 22h | 44h | 0000h | Typical timeout for full chip erase $2^N$ ms (00h = not supported) |
| 23h | 46h | 0005h | Max. timeout for byte/word write $2^N$ times typical |
| 24h | 48h | 0000h | Max. timeout for buffer write $2^N$ times typical |
| 25h | 4Ah | 0004h | Max. timeout per individual block erase $2^N$ times typical |
| 26h | 4Ch | 0000h | Max timeout for full chip erase $2^N$ times typical (00h = not supported) |

## Table 7. Device Geometry Definition

| Addresses (Word mode) | Addresses (Byte Mode) | Data | Description |
|---|---|---|---|
| 27h | 4Eh | 0016h | Device Size = $2^N$ bytes |
| 28h<br>29h | 50h<br>52h | 0002h<br>0000h | Flash Device Interface description (refer to CFI publication 100) |

| | | | |
|---|---|---|---|
| 2Ah<br>2Bh | 54h<br>56h | 0000h<br>0000h | Max. number of byte in multi-byte write = $2^N$<br>(00h = not supported) |
| 2Ch | 58h | 0002h | Number of Erase Block Regions within device |
| 2Dh<br>2Eh<br>2Fh<br>30h | 5Ah<br>5Ch<br>5Eh<br>60h | 0007h<br>0000h<br>0020h<br>0000h | Erase Block Region 1 Information<br>(refer to the CFI specification of CFI publication 100) |
| 31h<br>32h<br>33h<br>34h | 62h<br>64h<br>66h<br>68h | 003Eh<br>0000h<br>0000h<br>0001h | Erase Block Region 2 Information |
| 35h<br>36h<br>37h<br>38h | 6Ah<br>6Ch<br>6Eh<br>70h | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 3 Information |
| 39h<br>3Ah<br>3Bh<br>3Ch | 72h<br>74h<br>76h<br>78h | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 4 Information |

## Table 8. Primary Vendor-specific Extended Query

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|---|---|---|---|
| 40h<br>41h<br>42h | 80h<br>82h<br>84h | 0050h<br>0052h<br>0049h | Query-unique ASCII string “PRI” |
| 43h | 86h | 0031h | Major version number, ASCII |
| 44h | 88h | 0031h | Minor version number, ASCII |
| 45h | 8Ah | 0000h | Address Sensitive Unlock<br>0 = Required, 1 = Not Required |
| 46h | 8Ch | 0002h | Erase Suspend<br>0 = Not Supported, 1 = To Read Only, 2 = To Read & Write |
| 47h | 8Eh | 0004h | Sector Protect<br>0 = Not Supported, X = Number of sectors in per group |
| 48h | 90h | 0001h | Sector Temporary Unprotect<br>00 = Not Supported, 01 = Supported |
| 49h | 92h | 0004h | Sector Protect/Unprotect scheme<br>01 = 29F040 mode, 02 = 29F016 mode,<br>03 = 29F400 mode, 04 = 29LV800A mode |
| 4Ah | 94h | 0000h | Simultaneous Operation<br>00 = Not Supported, 01 = Supported |
| 4Bh | 96h | 0000h | Burst Mode Type<br>00 = Not Supported, 01 = Supported |
| 4Ch | 98h | 0000h | Page Mode Type<br>00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page |
| 4Dh | 9Ah | 00A5h | Minimum ACC (Acceleration) Supply Voltage<br>00 = Not Supported, DQ7-DQ4 : Volts, DQ3-DQ0 : 100mV |
| 4Eh | 9Ch | 00B5h | Maximum ACC (Acceleration) Supply Voltage<br>00 = Not Supported, DQ7-DQ4 : Volts, DQ3-DQ0 : 100mV |
| 4Fh | 9Eh | 0002h/<br>0003h | Top/Bottom Boot Sector Identifier<br>02h = Bottom Boot, 03h = Top Boot |

## Hardware Data protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes as seen in the Command Definitions table. Additionally, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by false system level signals during Vcc power up and power down transitions, or from system noise.

### Low $V_{CC}$ Write Inhibit

When Vcc is less than $V_{LKO}$, the device does not accept any write cycles. This protects data during Vcc power up and power down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until Vcc is greater than $V_{LKO}$. The system must provide the proper signals to the control pins to prevent unintentional writes when Vcc is greater than $V_{LKO}$.

### Write Pulse “Glitch” protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

### Logical Inhibit

Write cycles are inhibited by holding any one of OE# = $V_{IL}$, CE# = $V_{IH}$, or WE# = $V_{IH}$. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one. If CE#, WE#, and OE# are all logical zero (not recommended usage), it will be considered a read.

### Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with CE# = $V_{IL}$, WE#= $V_{IL}$ and OE# = $V_{IH}$, the device will not accept commands on the rising edge of WE#.

## COMMAND DEFINITIONS

The operations of the device are selected by one or more commands written into the command register. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Definitions table (Table 9). Incorrect addresses, incorrect data values or improper sequences will reset the device to Read Mode.

### Table 9. EN29LV320A Command Definitions

| Command Sequence | | | Cycles | Bus Cycles | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1st Cycle | | 2nd Cycle | | 3rd Cycle | | 4th Cycle | | 5th Cycle | | 6th Cycle | |
| | | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read | | | 1 | RA | RD | | | | | | | | | | |
| Reset | | | 1 | xxx | F0 | | | | | | | | | | |
| Autoselect | Manufacturer ID | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | 000 | 7F | | | | |
| | | | | | | | | | | 100 | 1C | | | | |
| | | Byte | | AAA | | 555 | | AAA | | 000 | 7F | | | | |
| | | | | | | | | | | 200 | 1C | | | | |
| | Device ID Top Boot | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | x01 | 22F6 | | | | |
| | | Byte | | AAA | | 555 | | AAA | | x02 | F6 | | | | |
| | Device ID Bottom Boot | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | x01 | 22F9 | | | | |
| | | Byte | | AAA | | 555 | | AAA | | x02 | F9 | | | | |
| | Sector Protect Verify | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | (SA) X02 | 00 | | | | |
| | | | | | | | | | | | 01 | | | | |
| | | Byte | | AAA | | 555 | | AAA | | (SA) X04 | 00 | | | | |
| | | | | | | | | | | | 01 | | | | |
| Program | | Word | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | |
| Unlock Bypass | | Word | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| | | Byte | | AAA | | 555 | | AAA | | | | | | | |
| Unlock Bypass Program | | | 2 | XXX | A0 | PA | PD | | | | | | | | |
| Unlock Bypass Reset | | | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| Chip Erase | | Word | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |
| | | Byte | | AAA | | 555 | | AAA | | AAA | | 555 | | AAA | |
| Sector Erase | | Word | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 |
| | | Byte | | AAA | | 555 | | AAA | | AAA | | 555 | | | |
| Sector Erase Suspend | | | 1 | xxx | B0 | | | | | | | | | | |
| Sector Erase Resume | | | 1 | xxx | 30 | | | | | | | | | | |
| CFI Query | | Word | 1 | 55 | 98 | | | | | | | | | | |
| | | Byte | | AA | | | | | | | | | | | |

Address and Data values indicated are in hex. Unless specified, all bus cycles are write cycles
RA = Read Address: address of the memory location to be read. This is a read cycle.
RD = Read Data: data read from location RA during Read operation. This is a read cycle.
PA = Program Address: address of the memory location to be programmed. X = Don't-Care
PD = Program Data: data to be programmed at location PA
SA = Sector Address: address of the Sector to be erased or verified. Address bits A20-A12 uniquely select any Sector.

## Reading Array Data

The device is automatically set to reading array data after power up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

Following a Sector Erase Suspend command, Sector Erase Suspend mode is entered. The system can read array data using the standard read timings from sectors other than the one which is being erase-suspended. If the system reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Sector Erase Suspend mode, the system may once again read array data with the same exception.

The Reset command must be issued to re-enable the device for reading array data if DQ5 goes high during an active program or erase operation or while in the autoselect mode. See next section for details on Reset.

## Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't-care for this command.

The reset command may be written between the cycle sequences in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Sector Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the cycle sequences in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies in Sector Erase Suspend mode).

## Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices ID codes, and determine whether or not a sector (group) is protected. The Command Definitions table shows the address and data requirements. This is an alternative to the method that requires $V_{ID}$ on address bit A9 and is intended for commercial programmers.

Two unlock cycles followed by the autoselect command initiate the autoselect command sequence. Autoselect mode is then entered and the system may read at addresses shown in Table 9 any number of times, without needing another command sequence.

The system **must write the reset command** to exit the autoselect mode and return to reading array data.

## Word / Byte Programming Command

The device can be programmed by byte or by word, depending on the state of the BYTE# Pin. Programming the EN29LV320A is performed by using a four-bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. An internal timer terminates the program operation automatically. Address is latched on the falling edge of CE# or WE#, whichever is last; data is latched on the rising edge of CE# or WE#, whichever is first.

Any commands written to the device during the program operation are ignored. Programming status can be checked by sampling data on DQ7 (DATA# polling) or on DQ6 (toggle bit). When the program operation is successfully completed, the device returns to read mode and the user can read the data programmed to the device at that address. Note that data can not be programmed from a "0" to a "1". Attempting to do so may halt the operation and set DQ5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1". When programming time limit is exceeded, DQ5 will produce a logical "1" and a Reset command can return the device to Read mode.

Programming is allowed in any sequence across sector boundaries.

## Unlock Bypass

To speed up programming operation, the Unlock Bypass Command may be used. Once this feature is activated, the shorter two-cycle Unlock Bypass Program command can be used instead of the normal four-cycle Program Command to program the device. During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset command can be accepted. This mode is exited after issuing the Unlock Bypass Reset Command. The device powers up with this feature disabled

The device provides accelerated program operations through the WP#/ACC pin. When WP#/ACC is asserted to $V_{HH}$, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass Program command sequence.

## Chip Erase Command

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Chip Erase algorithm are ignored.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

## Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

Once the sector erase operation has begun, only the Sector Erase Suspend command is valid. All other commands are ignored. If there are several sectors to be erased, Sector Erase Command sequences must be issued for each sector. That is, only **a sector address can be specified for each Sector Erase command**. Users must issue another Sector Erase command for the next sector to be erased after the previous one is completed.

When the Embedded Erase algorithm is completed, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to “Write Operation Status” for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

### Sector Erase Suspend / Resume Command

The Sector Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation. The Sector Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don’t-cares when writing the Sector Erase Suspend command.

When the Sector Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. Normal read and write timings and command definitions apply. Please note that **Autoselect command sequence can not be accepted during Sector Erase Suspend**.

Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See “Write Operation Status” for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “Write Operation Status” for more information. The Autoselect command is not supported during Sector Erase Suspend Mode.

The system must write the Sector Erase Resume command (address bits are don’t-care) to exit the sector erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Sector Erase Suspend command can be written after the device has resumed erasing.

## WRITE OPERATION STATUS

### DQ7: DATA# Polling

The EN29LV320A provides DATA# polling on DQ7 to indicate the status of the embedded operations. The DATA# Polling feature is active during the Word/Byte Programming, Sector Erase, Chip Erase, and Sector Erase Suspend. (See Table 10)

When the embedded programming is in progress, an attempt to read the device will produce the complement of the data written to DQ7. Upon the completion of the programming operation, an attempt to read the device will produce the true data written to DQ7. DATA# polling is valid after the rising edge of the fourth WE# or CE# pulse in the four-cycle sequence for program.

When the embedded Erase is in progress, an attempt to read the device will produce a “0” at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the “1” at the DQ7 output during the read cycles. For Chip Erase or Sector Erase, DATA# polling is valid after the rising edge of the last WE# or CE# pulse in the six-cycle sequence.

DATA# Polling must be performed at any address within a sector that is being programmed or erased and not a protected sector. Otherwise, DATA# polling may give an inaccurate result if the address used is in a protected sector.

Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable (OE#) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on the time the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operation and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 should be read on the subsequent read attempts.

The flowchart for DATA# Polling (DQ7) is shown on Flowchart 5. The DATA# Polling (DQ7) timing diagram is shown in Figure 6.

## RY/BY#: Ready/Busy Status output

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or completed. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to Vcc.

In the output-low period, signifying Busy, the device is actively erasing or programming. This includes programming in the Erase Suspend mode. If the output is high, signifying the Ready, the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

## DQ6: Toggle Bit I

The EN29LV320A provides a “Toggle Bit” on DQ6 to indicate the status of the embedded programming and erase operations. (See Table 10)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by active OE# or CE#) will result in DQ6 toggling between “zero” and “one”. Once the embedded Program or Erase operation is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During Programming, the Toggle Bit is valid after the rising edge of the fourth WE# pulse in the four-cycle sequence. During Erase operation, the Toggle Bit is valid after the rising edge of the sixth WE# pulse for sector erase or chip erase.

In embedded programming, if the sector being written to is protected, DQ6 will toggles for about 2 μs, then stop toggling without the data in the sector having changed. In Sector Erase or Chip Erase, if all selected sectors are protected, DQ6 will toggle for about 100 μs. The chip will then return to the read mode without changing data in all protected sectors.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 6. The Toggle Bit timing diagram is shown in Figure 7.

## DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed. Since it is possible that DQ5 can become a 1 when the device has successfully completed its operation and has returned to read mode, the user must check again to see if the DQ6 is toggling after detecting a “1” on DQ5.

The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits,

DQ5 produces a “1.” Under both these conditions, the system must issue the reset command to return the device to reading array data.

### DQ3: Sector Erase Timer

After writing a sector erase command sequence, the output on DQ3 can be checked to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) When sector erase starts, DQ3 switches from “0” to “1”. This device does not support multiple sector erase (continuous sector erase) command sequences so it is not very meaningful since it immediately shows as a “1” after the first 30h command. Future devices may support this feature.

### DQ2: Erase Toggle Bit II

The “Toggle Bit” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to the following table to compare outputs for DQ2 and DQ6.

Flowchart 6 shows the toggle bit algorithm, and the section “DQ2: Toggle Bit” explains the algorithm. See also the “DQ6: Toggle Bit I” subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

### Reading Toggle Bits DQ6/DQ2

Refer to Flowchart 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, after the initial two read cycles, the system determines that the toggle bit is still toggling. And the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

## Write Operation Status

| Operation | | DQ7 | DQ6 | DQ5 | DQ3 | DQ2 | RY/BY# |
|---|---|---|---|---|---|---|---|
| Standard Mode | Embedded Program Algorithm | DQ7# | Toggle | 0 | N/A | No toggle | 0 |
| | Embedded Erase Algorithm | 0 | Toggle | 0 | 1 | Toggle | 0 |
| Erase Suspend Mode | Reading within Erase Suspended Sector | 1 | No Toggle | 0 | N/A | Toggle | 1 |
| | Reading within Non-Erase Suspended Sector | Data | Data | Data | Data | Data | 1 |
| | Erase-Suspend Program | DQ7# | Toggle | 0 | N/A | N/A | 0 |

## Table 10. Status Register Bits

| DQ | Name | Logic Level | Definition |
|---|---|---|---|
| 7 | DATA# POLLING | '1' | Erase Complete or erased sector in Sector Erase Suspend |
| | | '0' | Erase On-Going |
| | | DQ7 | Program Complete or data of non-erased sector during Sector Erase Suspend |
| | | DQ7# | Program On-Going |
| 6 | TOGGLE BIT | '-1-0-1-0-1-0-1-' | Erase or Program On-going |
| | | DQ6 | Read during Sector Erase Suspend |
| | | '-1-1-1-1-1-1-1-' | Erase Complete |
| 5 | ERROR BIT | '1' | Program or Erase Error |
| | | '0' | Program or Erase On-going |
| 3 | SECTOR ERASE TIME BIT | '1' | Erase operation start |
| | | '0' | Erase timeout period on-going |
| 2 | TOGGLE BIT | '-1-0-1-0-1-0-1-' | Chip Erase, Sector Erase or Read within Erase-Suspended sector. (When DQ5=1, Erase Error due to currently addressed Sector or Program on Erase-Suspended sector |
| | | DQ2 | Read on addresses of non Erase-Suspend sectors |

**Notes:**

DQ7: DATA# Polling: indicates the P/E status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6: Toggle Bit: remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

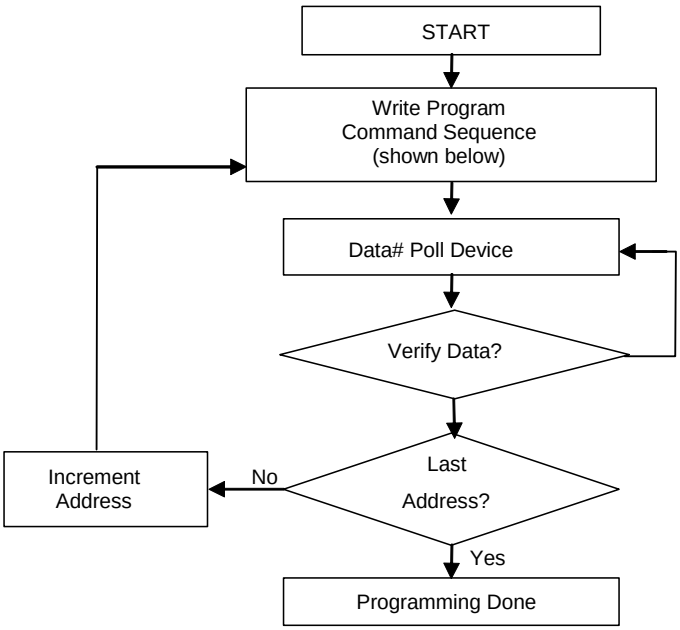
DQ5: Error Bit: set to "1" if failure in programming or erase

DQ3: Sector Erase Command Timeout Bit: Operation has started. Only possible command is Erase suspend (ES).

DQ2: Toggle Bit: indicates the Erase status and allows identification of the erased Sector.

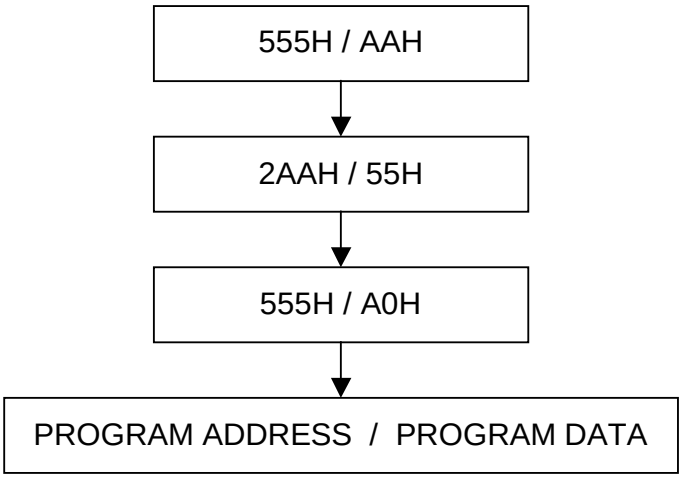
# EMBEDDED ALGORITHMS

## Flowchart 1. Embedded Program

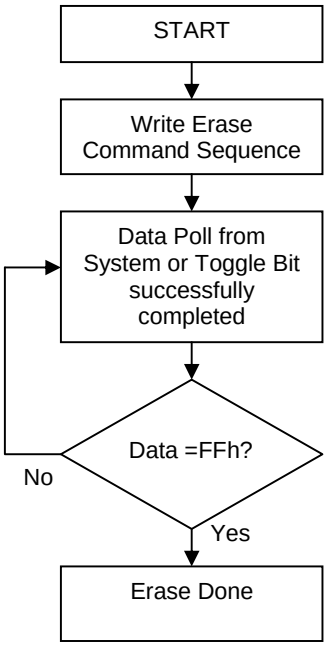



## Flowchart 2. Embedded Program Command Sequence

(See the Command Definitions section for more information.)

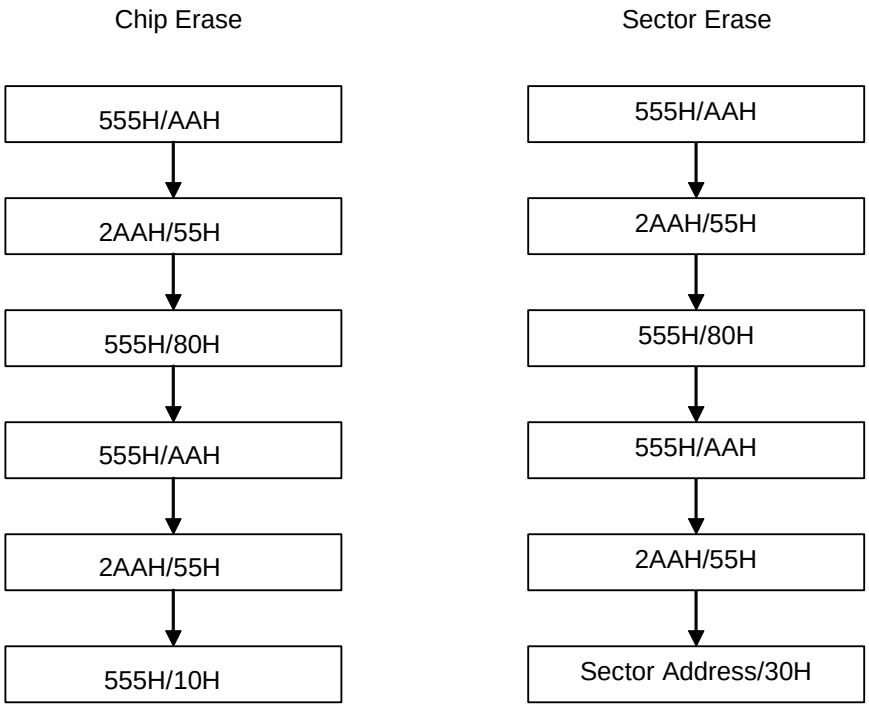


## Flowchart 3. Embedded Erase



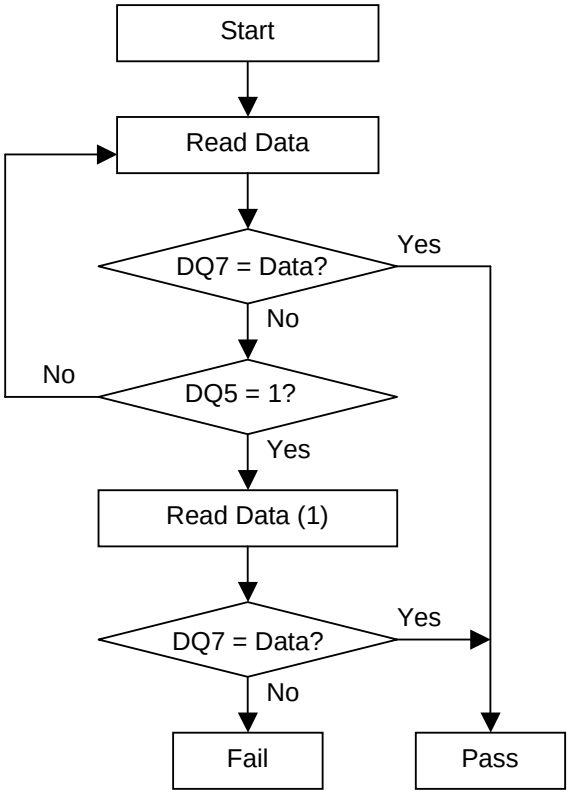

## Flowchart 4. Embedded Erase Command Sequence

(See the Command Definitions section for more information.)



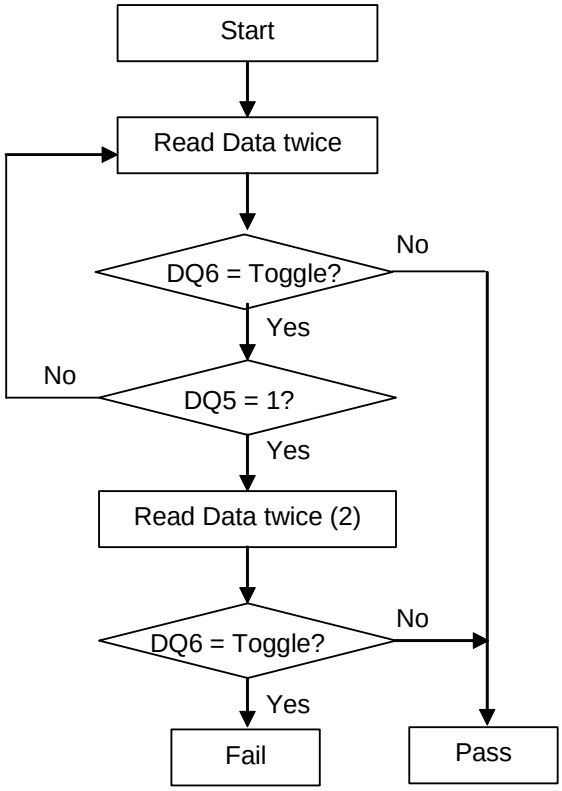

 

## Flowchart 5. DATA# Polling Algorithm



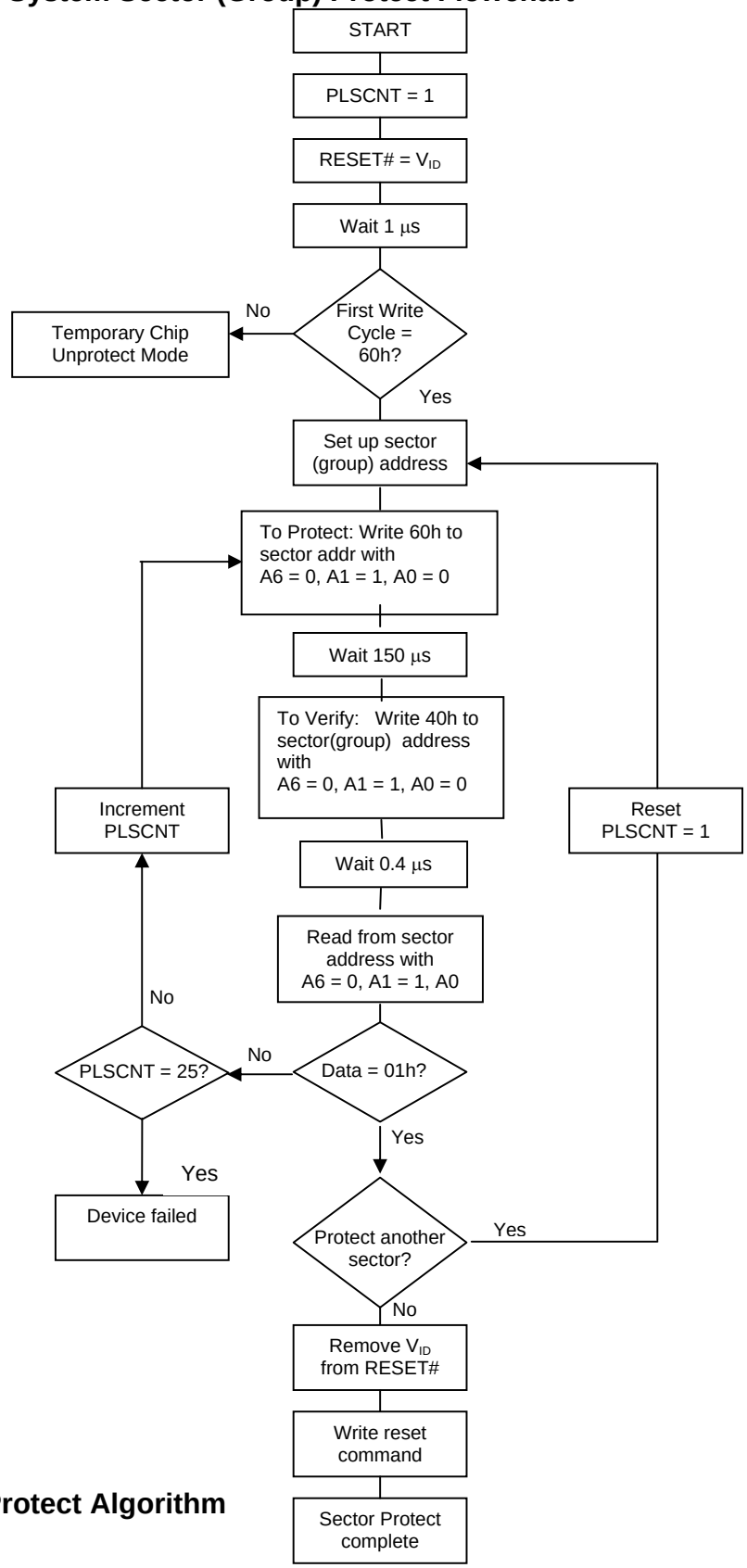

**Notes:**
(1) This second read is necessary in case the first read was done at the exact instant when the status data was in transition.

## Flowchart 6. Toggle Bit Algorithm



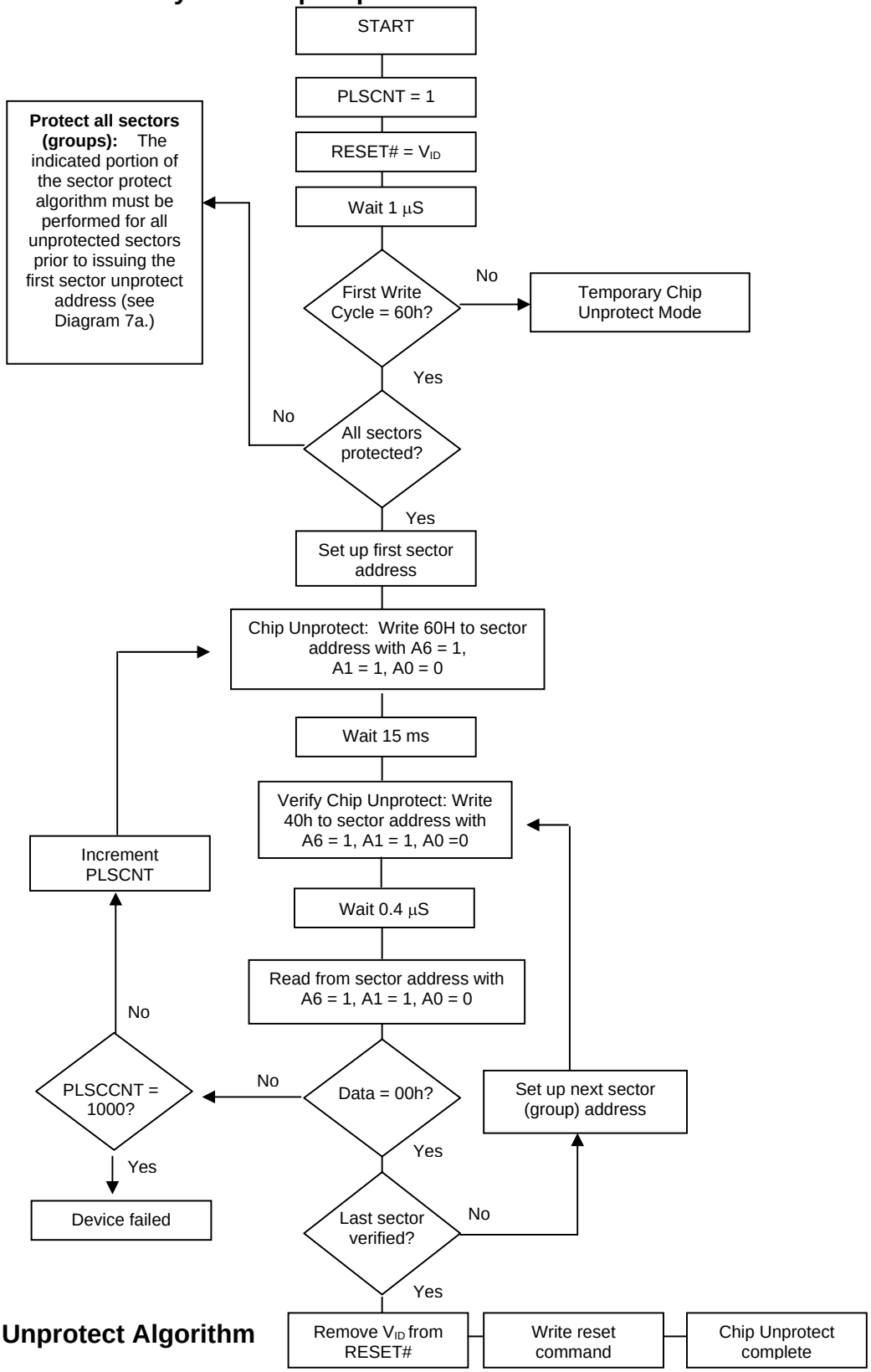

**Notes:**
(2) This second set of reads is necessary in case the first set of reads was done at the exact instant when the status data was in transition.

## Flowchart 7a. In-System Sector (Group) Protect Flowchart




## Sector Protect Algorithm

## Flowchart 7b. In-System Chip Unprotect Flowchart




## Chip Unprotect Algorithm

## ABSOLUTE MAXIMUM RATINGS

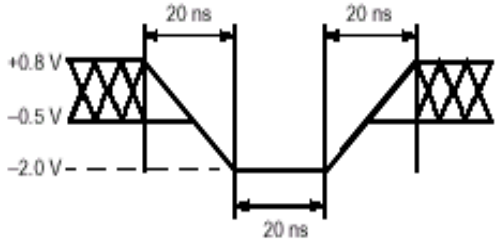
| Parameter | | Value | Unit |
|---|---|---|---|
| Storage Temperature | | -65 to +125 | °C |
| Plastic Packages | | -65 to +125 | °C |
| Ambient Temperature With Power Applied | | -55 to +125 | °C |
| Output Short Circuit Current[1] | | 200 | MA |
| Voltage with Respect to Ground | A9, OE#, RESET# and WP#/ACC[2] | -0.5 to +11.5 | V |
| | All other pins [3] | -0.5 to Vcc+0.5 | V |
| | Vcc | -0.5 to + 4.0 | V |

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC input voltage on A9, OE#, RESET# and WP#/ACC pins is –0.5V. During voltage transitions, A9, OE#, RESET# and WP#/ACC pins may undershoot $V_{ss}$ to –1.0V for periods of up to 50ns and to –2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on A9, OE#, and RESET# is 11.5V which may overshoot to 12.5V for periods up to 20ns.
3. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot $V_{ss}$ to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is $V_{cc}$ + 0.5 V. During voltage transitions, outputs may overshoot to $V_{cc}$ + 1.5 V for periods up to 20ns. See figure below.
4. Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

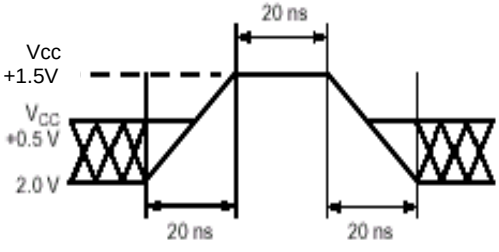
## RECOMMENDED OPERATING RANGES[1]

| Parameter | Value | Unit |
|---|---|---|
| Ambient Operating Temperature Commercial Devices Industrial Devices | 0 to 70 -40 to 85 | °C |
| Operating Supply Voltage Vcc | Full Voltage Range: 2.7 to 3.6V | V |

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.




Maximum Negative Overshoot Waveform




Maximum Positive Overshoot Waveform

## DC Characteristics

### Table 11. DC Characteristics

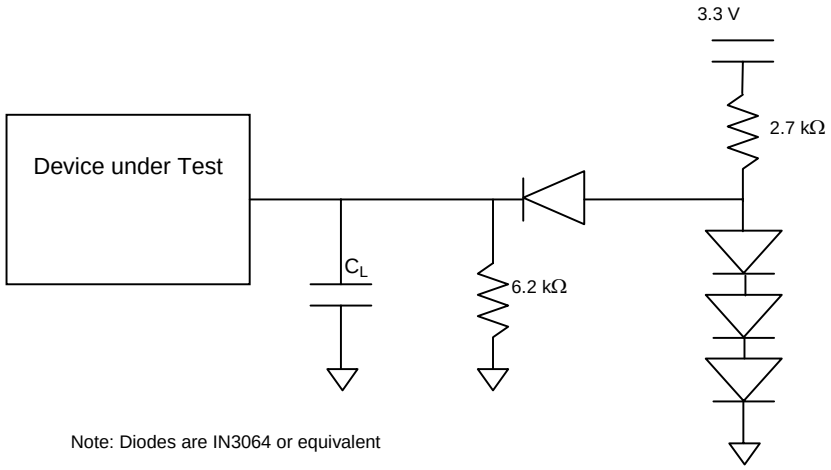
($T_a$ = 0°C to 70°C or - 40°C to 85°C; $V_{CC}$ = 2.7-3.6V)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | 0V≤ $V_{IN}$ ≤ Vcc | | | ±5 | µA |
| $I_{LO}$ | Output Leakage Current | 0V≤ $V_{OUT}$ ≤ Vcc | | | ±5 | µA |
| $I_{CC1}$ | Active Read Current ( Byte mode ) | CE# = $V_{IL}$ ; OE# = $V_{IH}$ ; f = 5MHZ | | 9 | 16 | mA |
| | Active Read Current ( Word mode ) | | | 9 | 16 | mA |
| $I_{CC2}$ | Supply Current (Program or Erase) | CE# = $V_{IL}$, OE# = $V_{IH}$ , WE# = $V_{IL}$ | | 20 | 30 | mA |
| $I_{CC3}$ | Supply Current (Standby - CMOS) | CE# = BYTE# = RESET# = Vcc ± 0.3V (Note 1) | | 1 | 5.0 | µA |
| $I_{CC4}$ | Reset Current | RESET# = Vss ± 0.3V | | 1 | 5.0 | µA |
| $I_{CC5}$ | Automatic Sleep Mode | $V_{IH}$ = Vcc ± 0.3V<br>$V_{IL}$ = Vss ± 0.3V | | 1 | 5.0 | uA |
| $V_{IL}$ | Input Low Voltage | | -0.5 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 0.7 x Vcc | | Vcc ± 0.3 | V |
| $V_{HH}$ | #WP/ACC Voltage (Write Protect / Program Acceleration) | | 10.5 | | 11.5 | V |
| $V_{ID}$ | Voltage for Autoselect or Temporary Sector Unprotect | | 10.5 | | 11.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 4.0 mA | | | 0.45 | V |
| $V_{OH}$ | Output High Voltage TTL | $I_{OH}$ = -2.0 mA | 0.85 x Vcc | | | V |
| | Output High Voltage CMOS | $I_{OH}$ = -100 µA, | Vcc - 0.4V | | | V |
| $V_{LKO}$ | Supply voltage (Erase and Program lock-out) | | 2.3 | | 2.5 | V |

**Notes:**

1. BYTE# pin can also be GND ± 0.3V. BYTE# and RESET# pin input buffers are always enabled so that they draw power if not at full CMOS supply voltages.
2. Maximum $I_{CC}$ specifications are tested with Vcc = Vcc max.

## Test Conditions




Note: Diodes are IN3064 or equivalent

## Test Specifications

| Test Conditions | -70 | -90 | | Unit |
|---|---|---|---|---|
| Output Load | 1 TTL Gate | | | |
| Output Load Capacitance, $C_L$ | 30 | 100 | | pF |
| Input Rise and Fall times | 5 | 5 | | ns |
| Input Pulse Levels | 0.0-3.0 | 0.0-3.0 | | V |
| Input timing measurement reference levels | 1.5 | 1.5 | | V |
| Output timing measurement reference levels | 1.5 | 1.5 | | V |

**Notes:**
1. Vcc=3.0 – 3.6 V for 70ns read operation

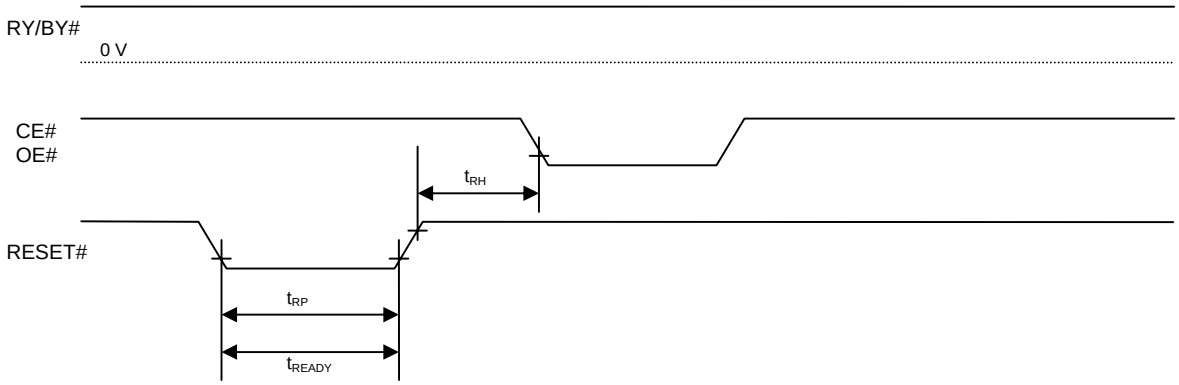
## AC CHARACTERISTICS

### Hardware Reset (RESET#)

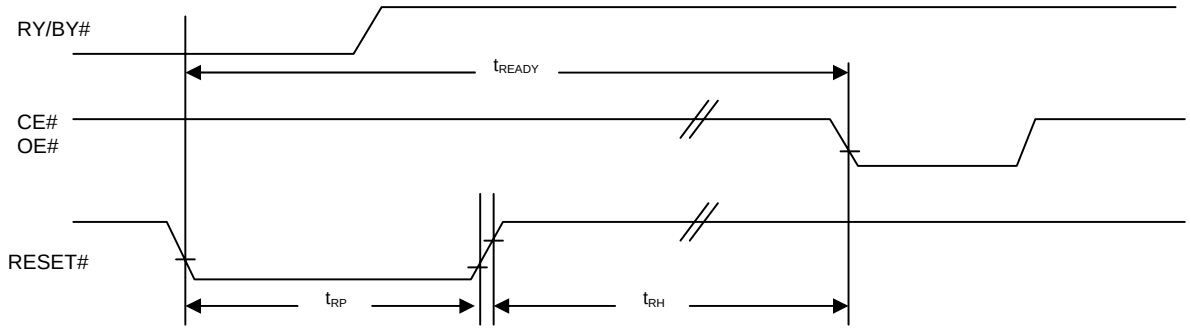
| Parameter Std | Description | Test Setup | Speed options | | Unit |
|---|---|---|---|---|---|
| | | | -70 | -90 | |
| $t_{READY}$ | Reset# Pin Low to Read or Write Embedded Algorithms | Max | 20 | | µs |
| $t_{READY}$ | Reset# Pin Low to Read or Write Non Embedded Algorithms | Max | 500 | | nS |
| $t_{RP}$ | Reset# Pulse Width | Min | 500 | | nS |
| $t_{RH}$ | Reset# High Time Before Read | Min | 50 | | nS |
| $t_{RPD}$ | Reset# to Standby Mode | Min | 20 | | µs |

### Figure 1. AC Waveforms for RESET#

### Reset# Timings




**Reset Timings NOT During Automatic Algorithms**



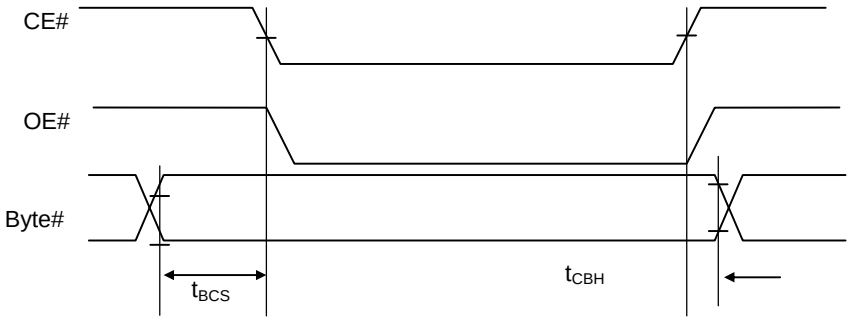

**Reset Timings During Automatic Algorithms**

## AC CHARACTERISTICS

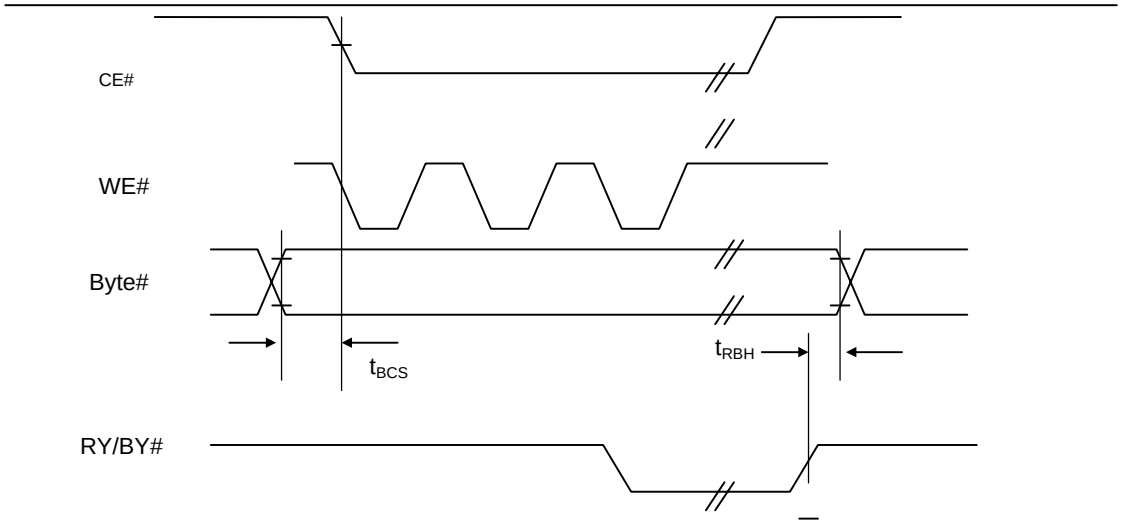
### Word / Byte Configuration (BYTE#)

| Std Parameter | Description | | Speed | | | Unit |
|---|---|---|---|---|---|---|
| | | | -70 | -90 | | |
| $t_{BCS}$ | BYTE# to CE# switching setup time | Min | 0 | 0 | | ns |
| $t_{CBH}$ | CE# to BYTE# switching hold time | Min | 0 | 0 | | ns |
| $t_{RBH}$ | RY/BY# to BYTE# switching hold time | Min | 0 | 0 | | ns |

### Figure 2. AC Waveforms for BYTE#




Byte# timings for Read Operations




Byte #timings for Write Operations

**Note:** Switching BYTE# pin not allowed during embedded operations

## AC CHARACTERISTICS

### Table 12. Read-only Operations Characteristics

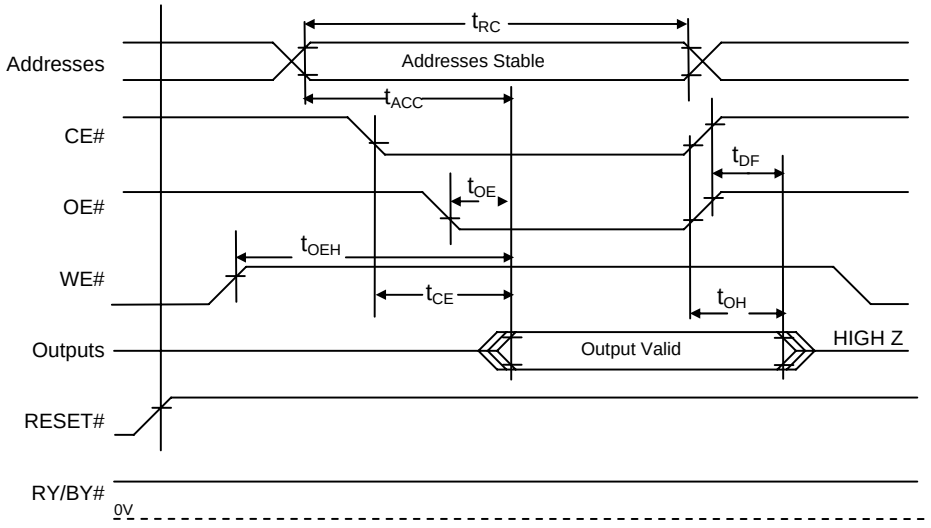
| Parameter Symbols | | Description | | Test Setup | | Speed Options | | |
|---|---|---|---|---|---|---|---|---|
| JEDEC | Standard | | | | | -70 | -90 | Unit |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | | | Min | 70 | 90 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | | CE# = $V_{IL}$ OE# = $V_{IL}$ | Max | 70 | 90 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable To Output Delay | | OE# = $V_{IL}$ | Max | 70 | 90 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | | Max | 30 | 35 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High Z | | | Max | 20 | 20 | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z | | | Max | 20 | 20 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time from Addresses, CE# or OE#, whichever occurs first | | | Min | 0 | 0 | ns |
| | $t_{OEH}$ | Output Enable Hold Time | Read | | Min | 0 | 0 | ns |
| | | | Toggle and Data# Polling | | Min | 10 | 10 | ns |

**Notes:**

For - 70
Vcc = 3.0V – 3.6V
Output Load: 1 TTL gate and 30pF
Input Rise and Fall Times: 5ns
Input Pulse Levels: 0.0 V to 3.0 V
Timing Measurement Reference Level, Input and Output: 1.5 V

- 90
Vcc = 2.7V – 3.6V
Output Load: 1 TTL gate and 100 pF
Input Rise and Fall Times: 5 ns
Input Pulse Levels: 0.0 V to 3.0 V
Timing Measurement Reference Level, Input and Output: 1.5 V

### Figure 3. AC Waveforms for READ Operations



## AC CHARACTERISTICS

### Table 13. Write (Erase/Program) Operations

| Parameter Symbols | | Description | | | Speed Options | | Unit |
|---|---|---|---|---|---|---|---|
| JEDEC | Standard | | | | -70 | -90 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | | Min | 70 | 90 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | 0 | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | | Min | 45 | 45 | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | | Min | 30 | 45 | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | 0 | ns |
| | $t_{OES}$ | Output Enable Setup Time | | Min | 0 | 0 | ns |
| | $t_{OEH}$ | Output Enable Hold Time | Read | MIn | 0 | 0 | ns |
| | | | Toggle and DATA# Polling | Min | 10 | 10 | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recovery Time before Write (OE# High to WE# Low) | | Min | 0 | 0 | ns |
| $t_{ELWL}$ | $t_{CS}$ | CE# Setup Time | | Min | 0 | 0 | ns |
| $t_{WHEH}$ | $t_{CH}$ | CE# Hold Time | | Min | 0 | 0 | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | | Min | 45 | 45 | ns |
| $t_{WHDL}$ | $t_{WPH}$ | Write Pulse Width High | | Min | 20 | 20 | ns |
| $t_{WHW1}$ | $t_{WHWH1}$ | Programming Operation | Byte | Typ | 8 | 8 | µs |
| | | | Word | Typ | 8 | 8 | |
| $t_{WHW1}$ | $t_{WHWH1}$ | Accelerated Programming Operation (Word AND Byte Mode) | | Typ | 7 | 7 | µs |
| $t_{WHW2}$ | $t_{WHWH2}$ | Sector Erase Operation | | Typ | 0.5 | 0.5 | s |
| $t_{WHW3}$ | $t_{WHWH3}$ | Chip Erase Operation | | Typ | 70 | 70 | s |
| | $t_{VCS}$ | Vcc Setup Time | | Min | 50 | 50 | µs |

## AC CHARACTERISTICS

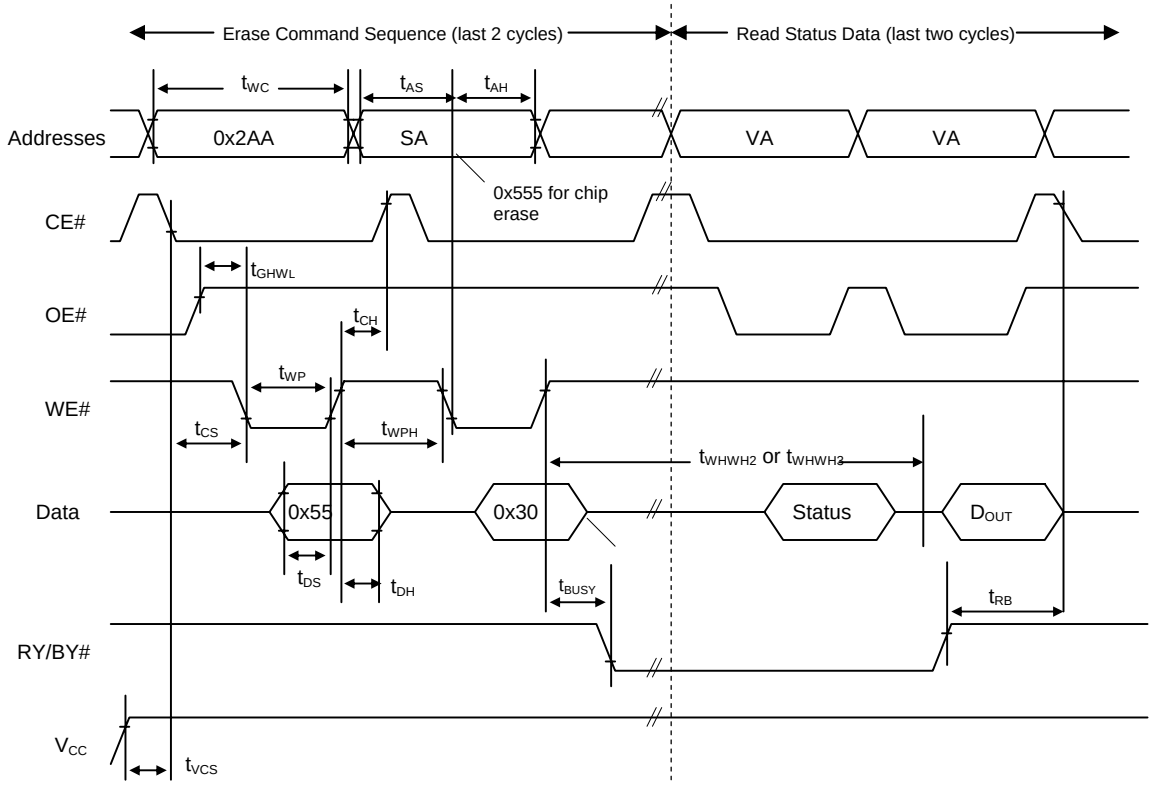
### Table 14. Write (Erase/Program) Operations

**Alternate CE# Controlled Writes**

| Parameter Symbols | | Description | | | Speed Options | | |
|---|---|---|---|---|---|---|---|
| JEDEC | Standard | | | | -70 | -90 | Unit |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | | Min | 70 | 90 | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | 0 | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | | Min | 45 | 45 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | | Min | 30 | 45 | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | 0 | ns |
| | $t_{OES}$ | Output Enable Setup Time | | Min | 0 | 0 | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recovery Time before Write (OE# High to CE# Low) | | Min | 0 | 0 | ns |
| $t_{WLEL}$ | $t_{WS}$ | WE# Setup Time | | Min | 0 | 0 | ns |
| $t_{EHWH}$ | $t_{WH}$ | WE# Hold Time | | Min | 0 | 0 | ns |
| $t_{ELEH}$ | $t_{CP}$ | CE# Pulse Width | | Min | 35 | 45 | ns |
| $t_{EHEL}$ | $t_{CPH}$ | CE# Pulse Width High | | Min | 20 | 20 | ns |
| $t_{WHW1}$ | $t_{WHWH1}$ | Programming Operation | Byte | Typ | 8 | 8 | µs |
| | | | Word | Typ | 8 | 8 | |
| $t_{WHW1}$ | $t_{WHWH1}$ | Accelerated Programming Operation (Word AND Byte Mode) | | Typ | 7 | 7 | µs |
| $t_{WHW2}$ | $t_{WHWH2}$ | Sector Erase Operation | | Typ | 0.5 | 0.5 | s |

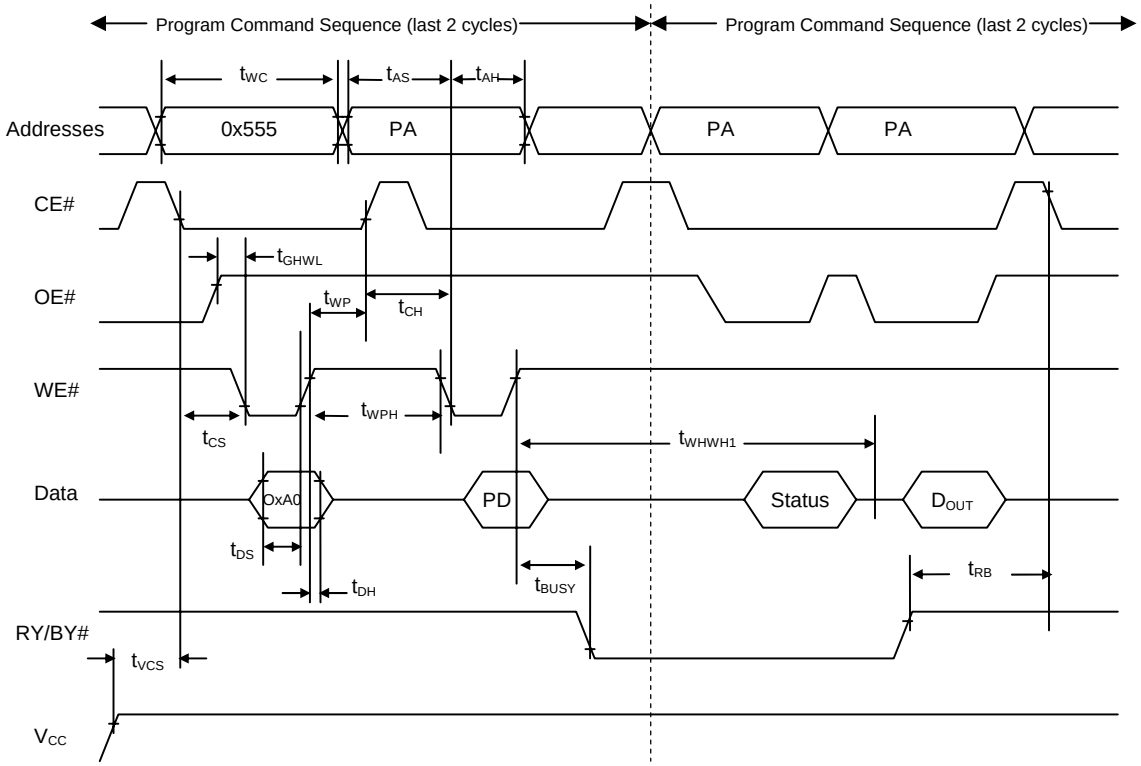
## AC CHARACTERISTICS

### Figure 4. AC Waveforms for Chip/Sector Erase Operations Timings



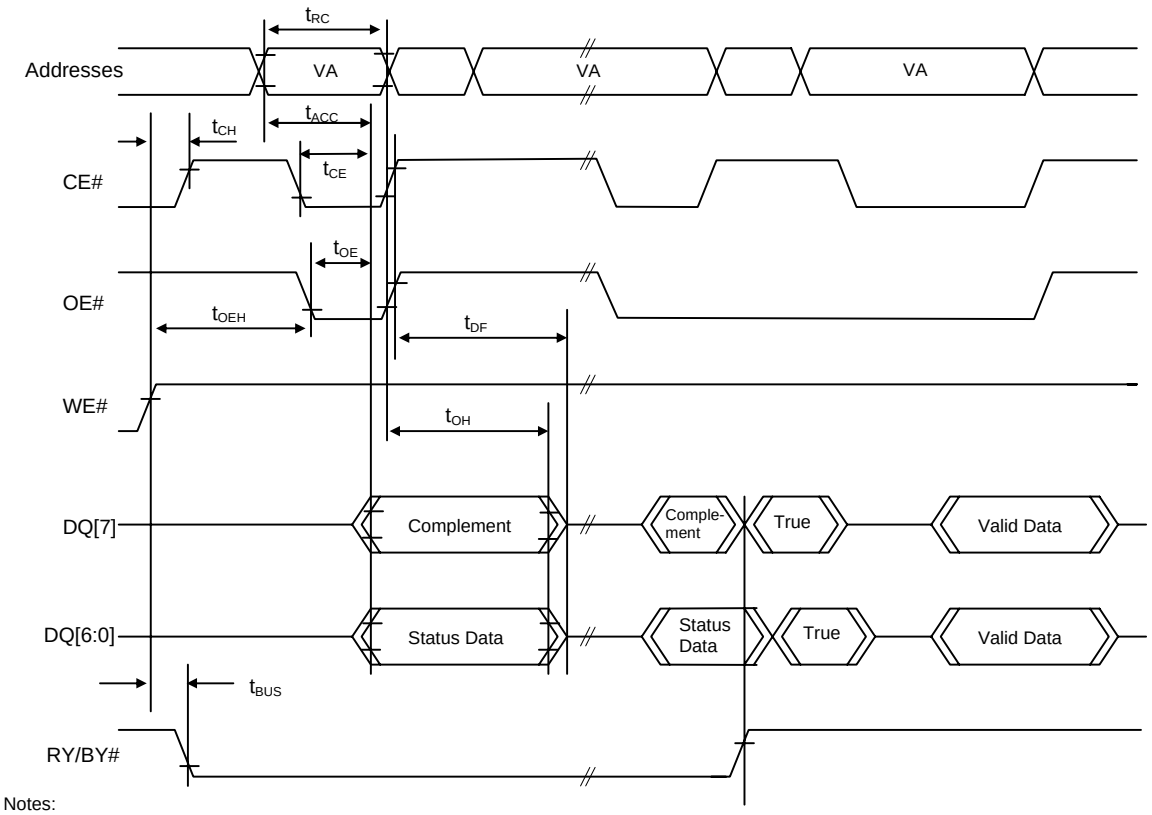

**Notes:**
1. SA=Sector Address (for sector erase), VA=Valid Address for reading status, $D_{out}$=true data at read address.
2. $V_{cc}$ shown only to illustrate $t_{vcs}$ measurement references. It cannot occur as shown during a valid command sequence.

## Figure 5. Program Operation Timings




**Notes:**
1. PA=Program Address, PD=Program Data, $D_{OUT}$ is the true data at the program address.
2. $V_{CC}$ shown in order to illustrate $t_{VCS}$ measurement references. It cannot occur as shown during a valid command sequence.

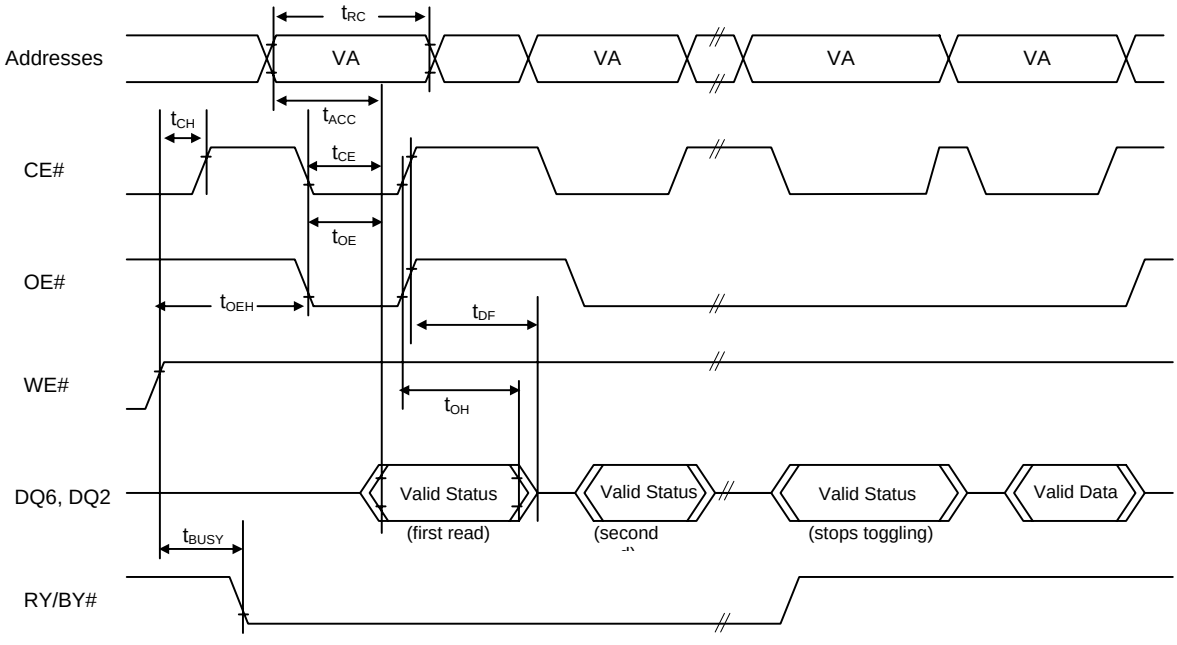
## Figure 6. AC Waveforms for /DATA Polling During Embedded Algorithm Operations



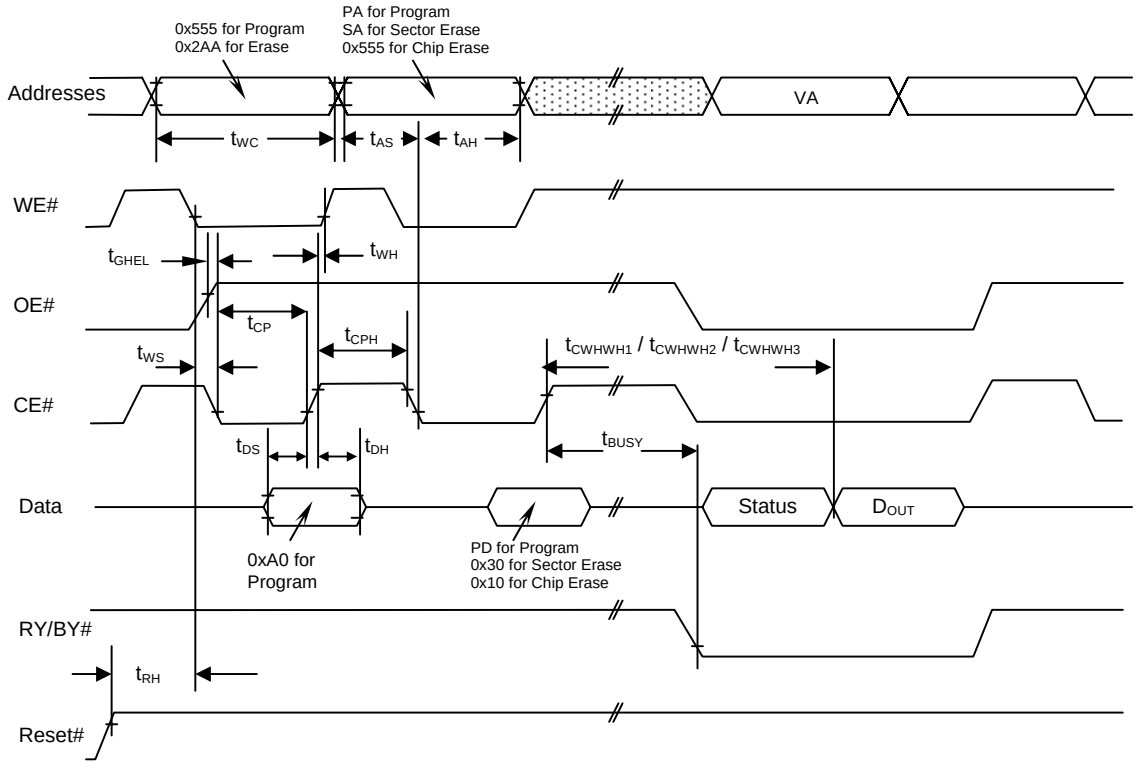

Notes:

1. VA=Valid Address for reading Data# Polling status data
2. This diagram shows the first status cycle after the command sequence, the last status read cycle and the array data read cycle.

## Figure 7. AC Waveforms for Toggle Bit During Embedded Algorithm Operations



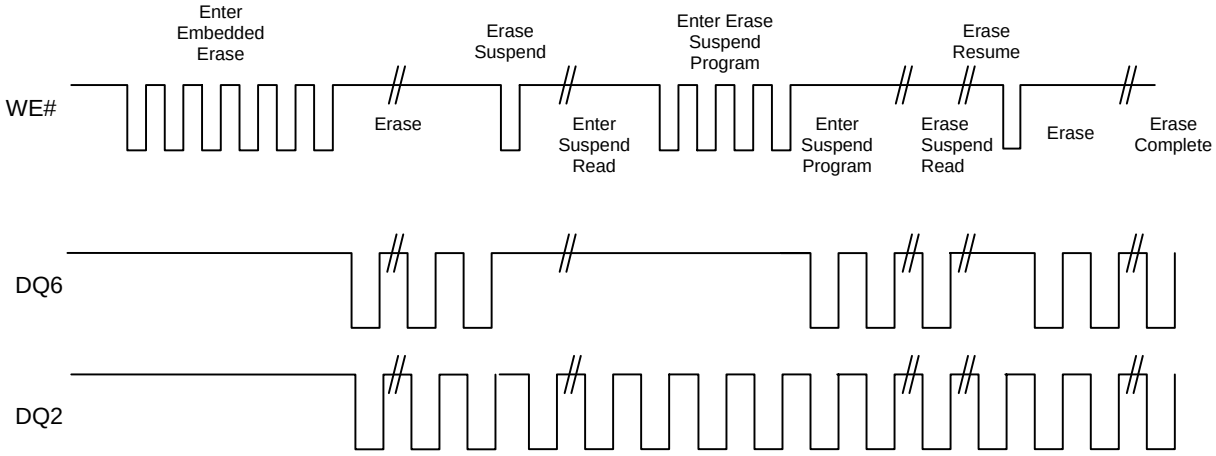
## Figure 8. Alternate CE# Controlled Write Operation Timings




**Notes:**

PA = address of the memory location to be programmed.
PD = data to be programmed at byte address.
VA = Valid Address for reading program or erase status
$D_{out}$ = array data read at VA
Shown above are the last two cycles of the program or erase command sequence and the last status read cycle
RESETt# shown to illustrate $t_{RH}$ measurement references. It cannot occur as shown during a valid command sequence.

## Figure 9. DQ2 vs. DQ6

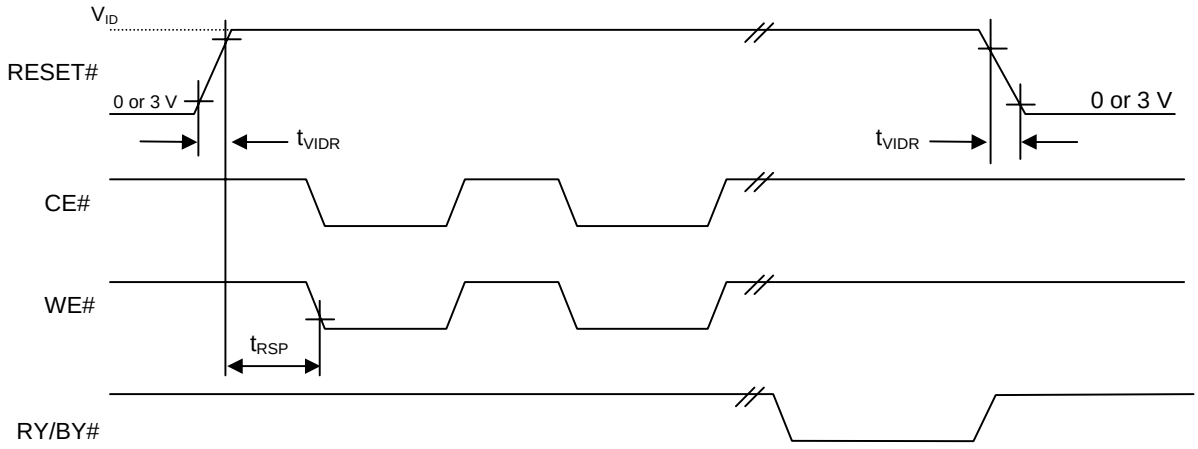


## AC CHARACTERISTICS

### Temporary Sector Unprotect

| Parameter Std | Description | | Speed Option | | Unit |
|---|---|---|---|---|---|
| | | | -70 | -90 | |
| $t_{VIDR}$ | $V_{ID}$ Rise and Fall Time | Min | 500 | | Ns |
| $t_{VIHH}$ | $V_{HH}$ Rise and Fall Time | Min | 500 | | Ns |
| $t_{RSP}$ | RESET# Setup Time for Temporary Sector Unprotect | Min | 4 | | µs |

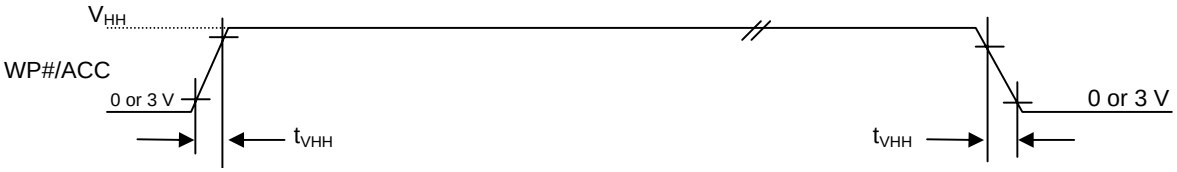
**Figure 10. Temporary Sector Unprotect Timing Diagram**




## AC CHARACTERISTICS

### Write Protect / Accelerated Program

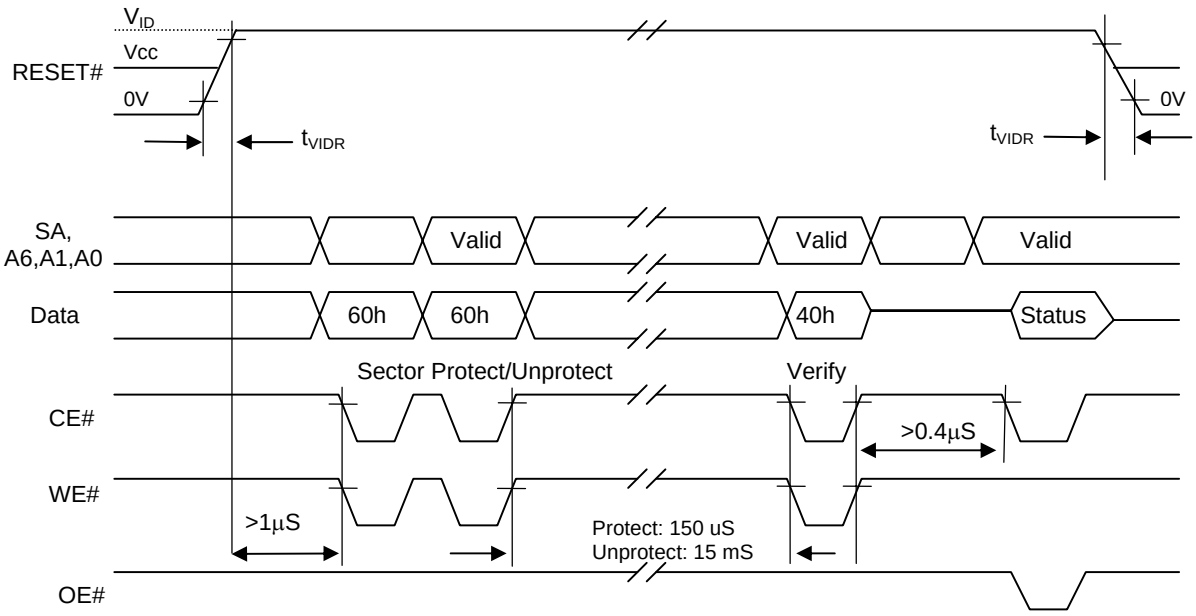
**Figure 11. Accelerated Program Timing Diagram**



## AC CHARACTERISTICS

### Sector (Group) Protect and Chip Unprotect

### Figure 12. Sector (Group) Protect and Chip Unprotect Timing Diagram




**Notes:**

Use standard microprocessor timings for this device for read and write cycles.
For Sector (Group) Protect, use A6=0, A1=1, A0=0. For Chip Unprotect, use A6=1, A1=1, A0=0.

## ERASE AND PROGRAM PERFORMANCE

| Parameter | | Limits | | | Comments |
|---|---|---|---|---|---|
| | | Typ | Max | Unit | |
| Sector Erase Time | | 0.5 | 10 | Sec | Excludes 00h programming prior to erasure |
| Chip Erase Time | | 70 | | Sec | |
| Byte Programming Time | | 8 | 300 | µS | Excludes system level overhead |
| Accelerated Byte/Word Program Time | | 7 | 200 | µS | |
| Word Programming Time | | 8 | 300 | µS | |
| Chip Programming Time | Byte | 35 | 100 | Sec | |
| | Word | 17 | 50 | | |
| Erase/Program Endurance | | 100K | | Cycles | Minimum 100K cycles |

**Note:** Typical Conditions are room temperature, 3V and checkboard pattern programmed.

## LATCH UP CHARACTERISTICS

| Parameter Description | Min | Max |
|---|---|---|
| Input voltage with respect to $V_{ss}$ on all pins except I/O pins (including A9, Reset and OE#) | -1.0 V | 12.0 V |
| Input voltage with respect to $V_{ss}$ on all I/O Pins | -1.0 V | Vcc + 1.0 V |
| Vcc Current | -100 mA | 100 mA |

**Note:** These are latch up characteristics and the device should never be put under these conditions. Refer to Absolute Maximum ratings for the actual operating limits.

## 48-PIN TSOP PACKAGE CAPACITANCE

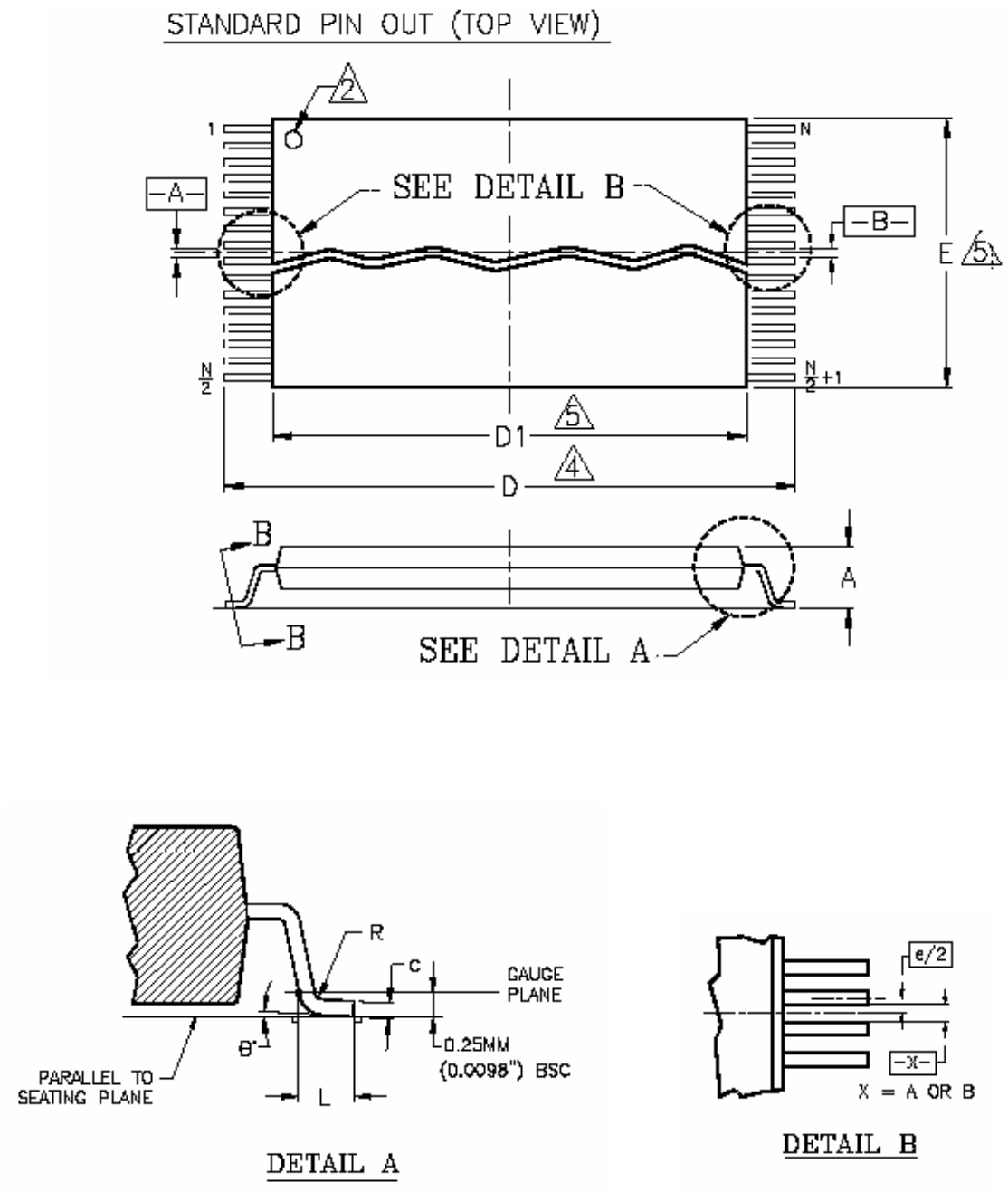
| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 7.5 | 9 | pF |

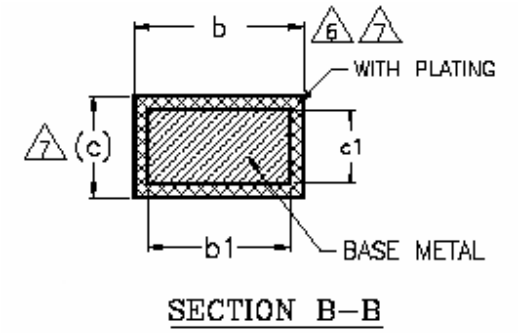
**Note:** Test conditions are Temperature = 25°C and f = 1.0 MHz.

## DATA RETENTION

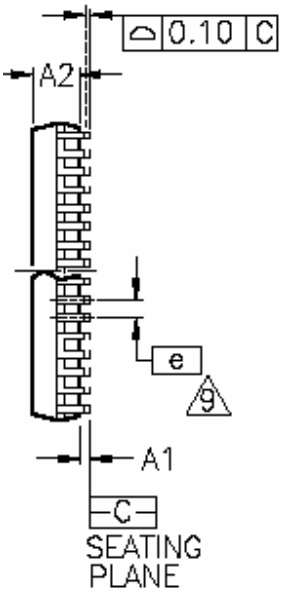
| Parameter Description | Test Conditions | Min | Unit |
|---|---|---|---|
| Minimum Pattern Data Retention Time | 150°C | 10 | Years |
| | 125°C | 20 | Years |

**FIGURE 13. TSOP 12mm x 20mm**






SECTION B–B

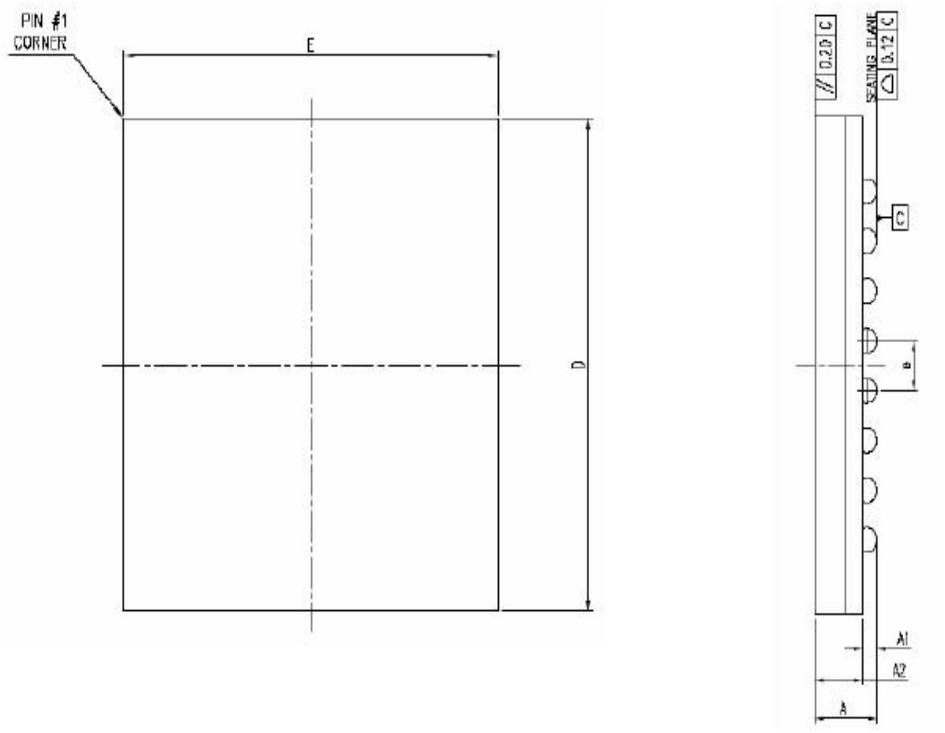


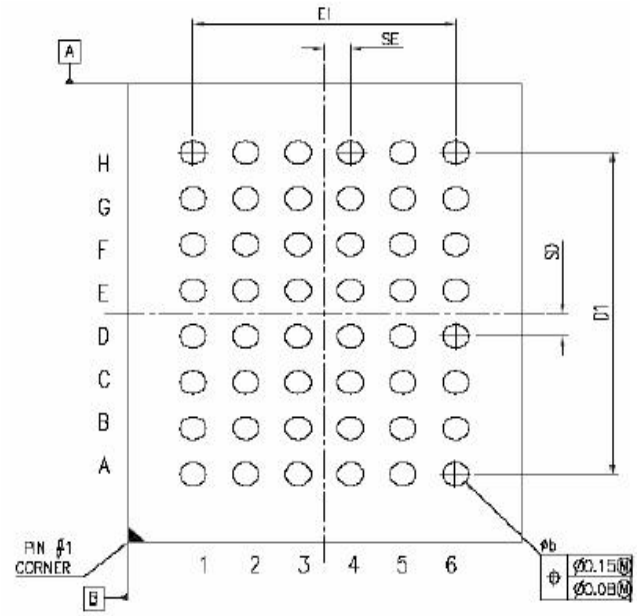

| Package | TS 48 | | |
|---|---|---|---|
| Jedec | MO-142 (B) DD | | |
| Symbol | MIN | NOM | MAX |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 19.80 | 20.00 | 20.20 |
| D1 | 18.30 | 18.40 | 18.50 |
| E | 11.90 | 12.00 | 12.10 |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | 3° | 5° |
| R | 0.08 | — | 0.20 |
| N | 48 | | |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

**FIGURE 14. 48TFBGA package outline**




| SYMBOL | DIMENSION IN MM | | |
|---|---|---|---|
| | MIN. | NOR | MAX |
| A | --- | --- | 1.31 |
| A1 | 0.23 | 0.28 | 0.33 |
| A2 | 0.86 | 0.92 | 0.98 |
| D | 7.90 | 8.00 | 8.10 |
| E | 5.90 | 6.00 | 6.10 |
| D1 | --- | 5.60 | --- |
| E1 | --- | 4.00 | --- |
| SD | --- | 0.40 | --- |
| SE | --- | 0.40 | --- |
| e | --- | 0.80 | --- |
| b | 0.35 | 0.40 | 0.45 |

## Revisions List

| Revision No | Description | Date |
|---|---|---|
| A | Initial Release | 2006/11/06 |
| B | To correct the Table 11. DC Characteristics, $I_{CC4}$ (Reset Current) Unit from mA to µA in page 32 | 2007/07/17 |