

DATA SHEET

# SKY13290-313LF: PHEMT 10 W SPDT Switch 500 MHz–2.5 GHz

## Features

- Broadband: 500 MHz–2.5 GHz
- Very low insertion loss: 0.4 dB typ. @ 900 MHz
- High isolation: 26 dB typ. @ 900 MHz
- High input power compression: 0.1 dB at > 40 dBm
- Low current consumption: <100  $\mu$ A @ 3 V
- Miniature QFN-6 2 x 3 mm package
- Lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

## Description

The SKY13290-313LF is a PHEMT IC high-power SPDT switch. This high-power switch has been designed for use from 500 MHz–2.5 GHz, where low loss, high isolation, low control voltage and ultraminiature package size are required. It can be controlled with positive, negative or a combination of both voltages. The RF signal paths within the SKY13290-313LF are fully bilateral.

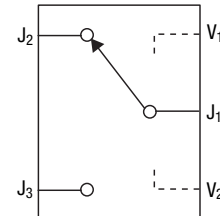
Some standard implementations include T/R switching for telematic applications at elevated power levels.

Switching is controlled via two control voltage inputs. Depending upon the voltage level applied to the control voltage pins, the common RF port ( $J_1$ ) is connected to one of two RF ports ( $J_2$  or  $J_3$ ) via a low insertion loss path, while the path between  $J_1$  and the other RF port is in its isolation state. When the control voltages are toggled, the states between  $J_1$  and  $J_2$ , as well as  $J_1$  and  $J_3$ , are also toggled.

The SKY13290-313LF is available in a lead (Pb)-free, RoHS-compliant, QFN-6 2 x 3 mm plastic package.

An evaluation board is available upon request.

## Functional Block Diagram



**NEW**

Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.



[查询"SKY13290-313LF"供应商](#)**Electrical Specifications at 25 °C** **$V_{\text{CTRL}} = 0/3 \text{ V}$ ,  $T = 25^\circ\text{C}$ ,  $P_{\text{INPUT}} = 0 \text{ dbm}$ ,  $Z_0 = 50 \Omega$ , unless otherwise noted**

Parameter	Frequency	Min.	Typ.	Max.	Unit
Insertion loss	0.5–1.0 GHz		0.40	0.5	dB
	1.0–2.0 GHz		0.45	0.6	dB
	2.0–2.5 GHz		0.55	0.7	dB
Isolation	0.5–1.0 GHz	23	26		dB
	1.0–2.0 GHz	17	20		dB
	2.0–2.5 GHz	15	18		dB
Return loss <sup>(1)</sup>	0.5–1.0 GHz		20		dB
	1.0–2.5 GHz		20		dB

1. Return loss state. Lower frequency return loss is dependent on value of the DC blocks.

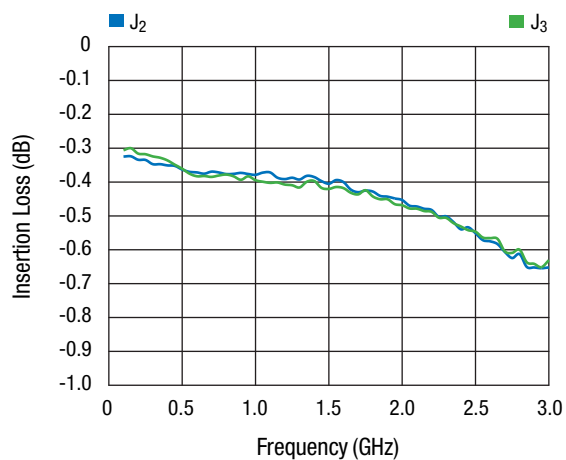
**Operating Characteristics at 25 °C** **$V_{\text{CTRL}} = 0/3 \text{ V}$ ,  $T = 25^\circ\text{C}$ ,  $P_{\text{INPUT}} = 0 \text{ dbm}$ ,  $Z_0 = 50 \Omega$ , unless otherwise noted**

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics:						
Rise/fall time	10/90% or 90/10% RF			650		ns
On/off time	50% $V_{\text{CTL}}$ to 90/10% RF			800		ns
Input power for 0.1 dB compression		900 MHz		40.5		dBm
Thermal resistance				45		°C/W
Control voltage	$V_{\text{LOW}} = 0 \text{ V @ } 20 \mu\text{A maximum}$ $V_{\text{HIGH}} = 2.7 \text{ V @ } 100 \mu\text{A maximum to } 10 \text{ V @ } 200 \mu\text{A maximum}$					

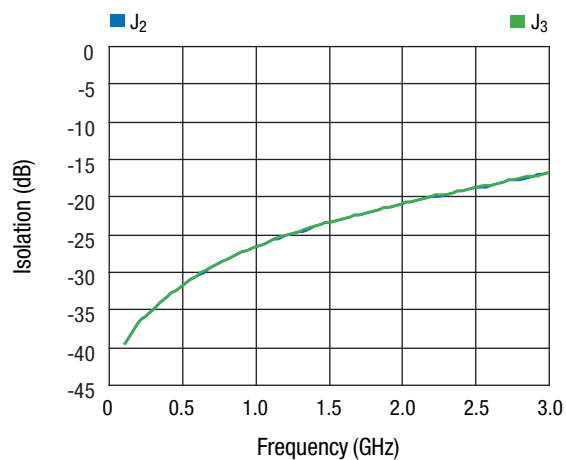
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## Typical Performance Data

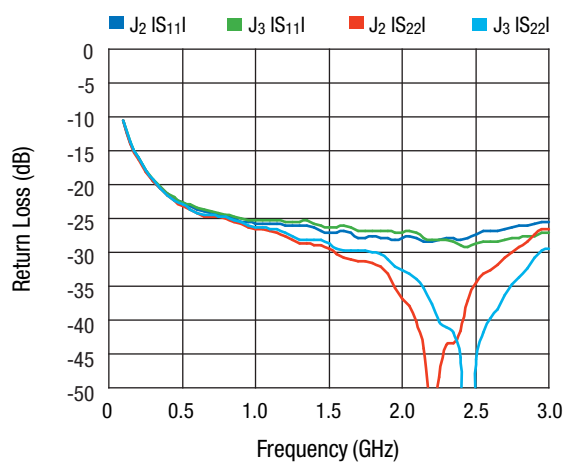
$Z_0 = 50\ \Omega$ ,  $V_{CTRL} = 0/3\ V$ , unless otherwise noted



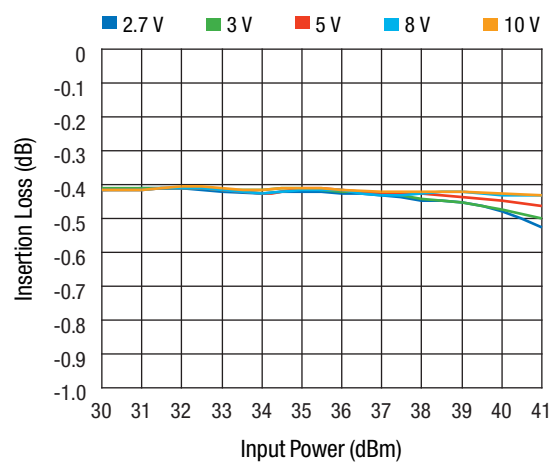
Insertion Loss vs. Frequency



Isolation vs. Frequency



Return Loss vs. Frequency  
(Insertion Loss State)



Insertion Loss vs. Input Power  
F = 900 MHz

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**Absolute Maximum Ratings**

Characteristic	Value
Control voltage range	$0 \leq V_C \leq 10\text{ V}$
RF input power	43.5 dBm, $f > 900\text{ MHz}$
Operating temperature	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
Storage temperature	$-65\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

**CAUTION:** Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

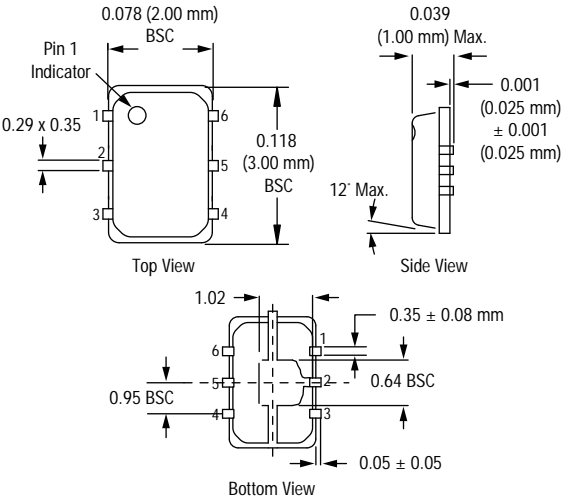
**Recommended Solder Reflow Profiles**

Refer to the [“Recommended Solder Reflow Profile”](#) Application Note.

**Tape and Reel Information**

Refer to the [“Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation”](#) Application Note.

**QFN-6**

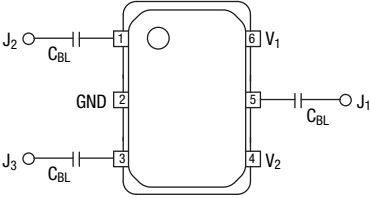


**Truth Table**

$V_1$	$V_2$	$J_1-J_2$	$J_1-J_3$
$V_{LOW}$	$V_{HIGH}$	Isolation	Insertion loss
$V_{HIGH}$	$V_{LOW}$	Insertion loss	Isolation
$V_{LOW}$	$V_{LOW}$	Not recommended <sup>(1)</sup>	
$V_{HIGH}$	$V_{HIGH}$	Not recommended <sup>(1)</sup>	

$2.7\text{ V} < V_{HIGH} < 10\text{ V}$ ,  $0 < V_{LOW} < 0.2\text{ V}$ .  
1. Switch in undefined state.

**Pin Out (Top View)**



DC blocking capacitors ( $C_{BL}$ ) must be supplied externally.

**Pin Descriptions**

Pin Number	Pin Name	Description
1	$J_2$	RF Input/Output – RF input/output port which is either connected to $J_1$ via a low insertion loss path or isolated from $J_1$ , according to the logic voltage levels applied to $V_1$ and $V_2$ .
2	GND	Equipotential Point – Internal circuit common, which must be connected to the pcb ground or common via the lowest possible impedance.
3	$J_3$	RF Input/Output – RF input/output port which is either connected to $J_1$ via a low insertion loss path or isolated from $J_1$ , according to the logic voltage levels applied to $V_1$ and $V_2$ .
4	$V_2$	Control Voltage 2 – Control voltage input #2. The logic voltage level applied to this pin, along with the voltage level applied to $V_1$ (pin 6), determines the states of the RF paths between $J_1-J_2$ and $J_1-J_3$ .
5	$J_1$	RF Common Input/Output – RF common input/output port which is either connected to $J_2$ or to $J_3$ via a low insertion loss and isolated from the other RF port, according to the logic voltage levels applied to $V_1$ and $V_2$ .
6	$V_1$	Control Voltage 1 – Control voltage input #1. The logic voltage level applied to this pin, along with the voltage level applied to $V_2$ (pin 4), determines the states of the RF paths between $J_1-J_2$ and $J_1-J_3$ .

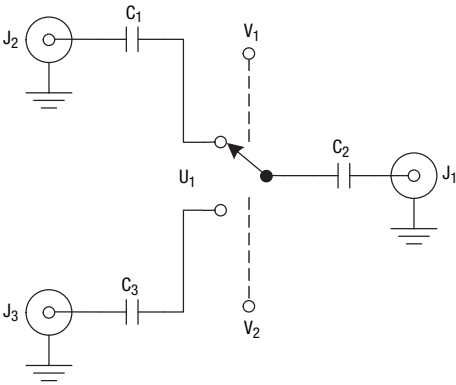
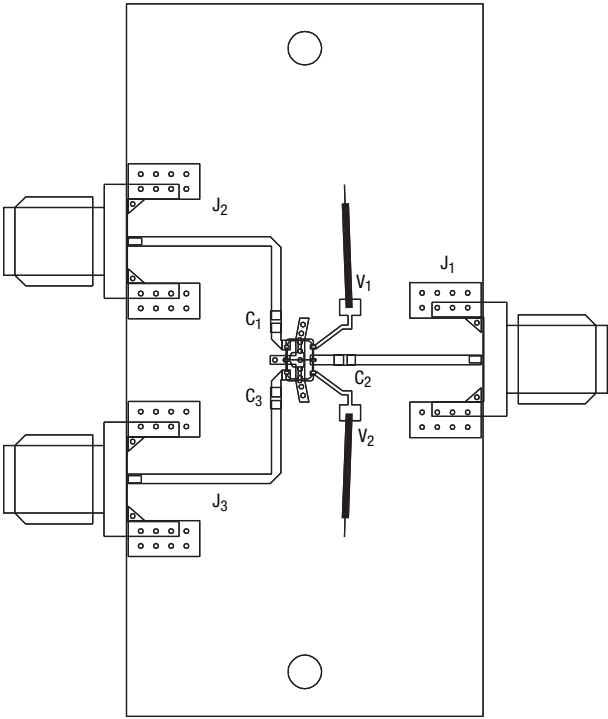
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**Evaluation Board**

The evaluation board for the SKY13290-313 allows the switch to be fully exercised. The RF common port is marked “J<sub>1</sub>”, and the two switched RF ports are marked “J<sub>2</sub>” and “J<sub>3</sub>”. All of the RF ports have SMA connectors mounted. The control voltage inputs are marked “V<sub>1</sub>” and “V<sub>2</sub>”.

The printed circuit board material is Rogers 4003. The RF dielectric layer is 0.012 inches thick, ½ oz. copper. The RF transmission lines are each 50 Ω (nominal) microstrip.

There are three DC blocking capacitors on the board, C<sub>1</sub>, C<sub>2</sub> and C<sub>3</sub>, each of which is in series with one of the RF ports. These capacitors are 47 pF. For improved insertion loss at signal frequencies below approximately 500 MHz these capacitors should be replaced with larger capacitance capacitors, such as 1000 pF.

Item	Description	Comments
C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>	DC Blocking Capacitor, 47 pF	0402
J <sub>1</sub> , J <sub>2</sub> , J <sub>3</sub>	SMA Connector, Edge Mount	
U1	SKY13290-313	
Printed Circuit Board	Skyworks SK39990	



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