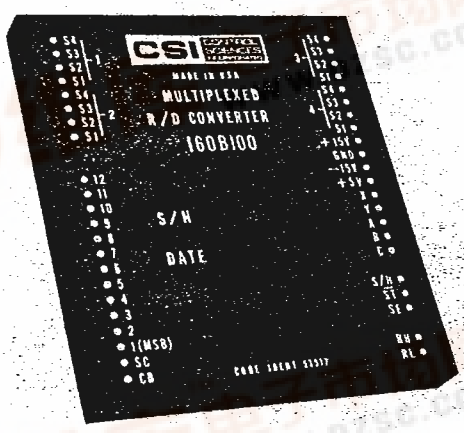
synchro/resolver to digital converter
low cost multiplexed 12 bit
series 160B



FEATURES

- Synchro or resolver inputs
- Four channels — single module
- Expandable
- 12-bit output resolution
- 100-microsecond conversion
- 57 to 5000 Hz operation
- Simultaneous sampling
- Capacity to 40 channels
- Random access
- CMOS/TTL compatible

APPLICATIONS

Air Data Computers — Robotics — Machine Tool Controls — Data Logging

GENERAL DATA

The 160B100 series is a complete 4-channel multiplexed S/D or R/D converter contained in a single low profile module. Any synchro or resolver line-to-line voltage between 2.5 and 130 volts can be specified at frequencies from 57 Hz to 5 KHz.

Up to 40 input channels can be accommodated by the addition of external input modules. Twelve bits of parallel binary angle are converted in less than 100 microseconds per channel. All channels are simultaneously sampled on negative carrier peaks.

Signal and reference inputs are differential solid state with high common mode rejection and inherent transient protection.

THEORY OF OPERATION

The 160B100 module is a complete 4-channel multiplexed S/D or R/D converter (see figure 4). Each synchro or resolver is connected to a separate input channel. The module contains one reference processor, therefore all input synchros or resolvers must share a common reference.

The purpose of the reference processor is to produce a sample/hold (S/H) pulse at or near the reference negative peaks. The S/H pulse can be inhibited by applying a logic "0" to the sample enable (SE) input. The synchro or resolver inputs are sampled simultaneously during each S/H pulse.

The outputs from each signal input circuit are two ac voltages proportional to the sine and cosine of the input angle. These signals are sampled by the dual sample/hold circuits at a time close to the negative peaks of the reference waveform. The sampled dc outputs are muxed together to the central processor input. The MUX select lines determine which of these outputs will be processed.

After a conversion cycle is initiated on an SC "0" to "1" transition, the successive approximation register is reset. Bit 1 is then set to logic "0," all other bits remain high, and the SSCT performs the trigonometric computation: $\theta - \phi = \sin\theta \cos\phi - \cos\theta \sin\phi$. On the next clock "0" to "1" transition the D input to the register is set into bit 1 and bit 2 is set to a logic "0." This operation is repeated for each register bit in turn until the register has been filled. When the data goes into bit 12, the CB signal goes low approximately one microsecond later, and the register is inhibited from further change until reset by an SC command.

The parallel binary angle ϕ contained in the register is equal to the selected input synchro or resolver angle θ.

Parameter	Value
Resolution	12 bits (0.088°)
Accuracy[1]	±8.5 minutes
Conversion time	100 μs max
Signal Sample Rate	Once per reference cycle, all channels sampled simultaneously
Channel Access[2]	Random, binary coded
Number of Channels	4, expandable to 40
Digital Inputs[3]	
Start Convert (SC)	1 to 70 μs positive pulse, leading edge initiates conversion
Sample Enable (SE)	Logic "0" inhibits sample
Channel Select (A,B,&C)	Binary coded, C used for expansion
Digital Outputs	
12 Parallel Data Bits	Natural binary angle, positive logic 2 TTL loads max
Sample Time Output ($\overline{ST}$)	Logic "0" when peak sampling 2 TTL loads max
Converter Busy (CB)	100 μs max, logic "1" during conversion 4 TTL loads max
Synchro/Resolver Inputs	
Input Type[4]	Differential solid state
Input Voltage (E_{L-L})	2.5 to 130V rms
Input Impedance	8.8 (E_{L-L}) kohms
Reference Input	
Input Type[4]	Differential solid state
Input Voltage (E_{RH-RL})	2.5 to 130V rms
Input Impedance	6.6 (E_{RH-RL}) kohms
Frequency Range	47 Hz to 5 kHz
Power Supplies	
+5V	50 mA max (45 mA typ)
+15V	65 mA max (55 mA typ)
−15V	90 mA max (80 mA typ)
Temperature Ranges	
Operating	0° to 70°C
Storage	−55° to 125°C
Dimensions	3.4″ x 4.0″ x 0.4″
Weight	6.0 oz.

NOTES:

1. Accuracy applies for:
   a) ±10% signal amplitude and frequency variations
   b) 10% signal and reference harmonic distortion
   c) ±5% power supply variation
   d) over operating temperature range
2. Except during peak sampling.
3. All digital inputs are CMOS with internal 33 kohms pull-up to +5V.
4. Any one stator and/or rotor line may be grounded. Common mode voltage up to specified L-L voltage have no effect on operation.

Timing and control for the 160B100 are shown in figures 1 thru 3. The basic timing sequence is as follows:

1. Start conversion with a 1 to 70-microsecond start convert (SC) pulse. The leading edge of the SC pulse will cause a converter busy (CB) pulse to be generated.
2. Select the channel to be converted as described in Table 1 prior to or within one microsecond after the CB leading edge.

This sequence is repeated for each conversion. A new conversion can be immediately initiated after the CB pulse goes low.

For best results, the MUX converter should not be commanded totally asynchronously. If a conversion occurs during a sample time ($\overline{ST}$ = 0), errors of several LSB's are possible. To prevent this, it is necessary to program the conversions around the $\overline{ST}$ pulse or interlock the sample/hold pulse (S/H). An interlock circuit has to cover the two situations when the sample time can interfere with the conversion:

1. When the converter is busy (CB = 1), then the S/H pulse must be inhibited by setting SE to logic "0" until the conversion is complete.
2. When the sampler is busy ($\overline{ST}$ = 0), then the SC pulse must be delayed until $\overline{ST}$ goes to logic "1."

It is important to note the manner in which the sample enable input (SE) affects the S/H generation. When SE = 1, the S/H pulse will occur at its normal time, near each negative peak of the reference waveform. The S/H pulse is inhibited only if the SE is at logic "0" at the moment the $\overline{ST}$ is initiated. Once the $\overline{ST}$ begins, a subsequent drop to logic "0" of the SE input will not affect the S/H pulse completion. If the SE input is brought to logic "1" when the $\overline{ST}$ is low, a 10 to 15-microsecond pulse is generated.

The $\overline{ST}$ pulse is not affected by the SE input; the $\overline{ST}$ pulse always occurs at the negative carrier peaks no matter what the state of the SE input.

The maximum number of conversions per carrier cycle may be calculated as follows:

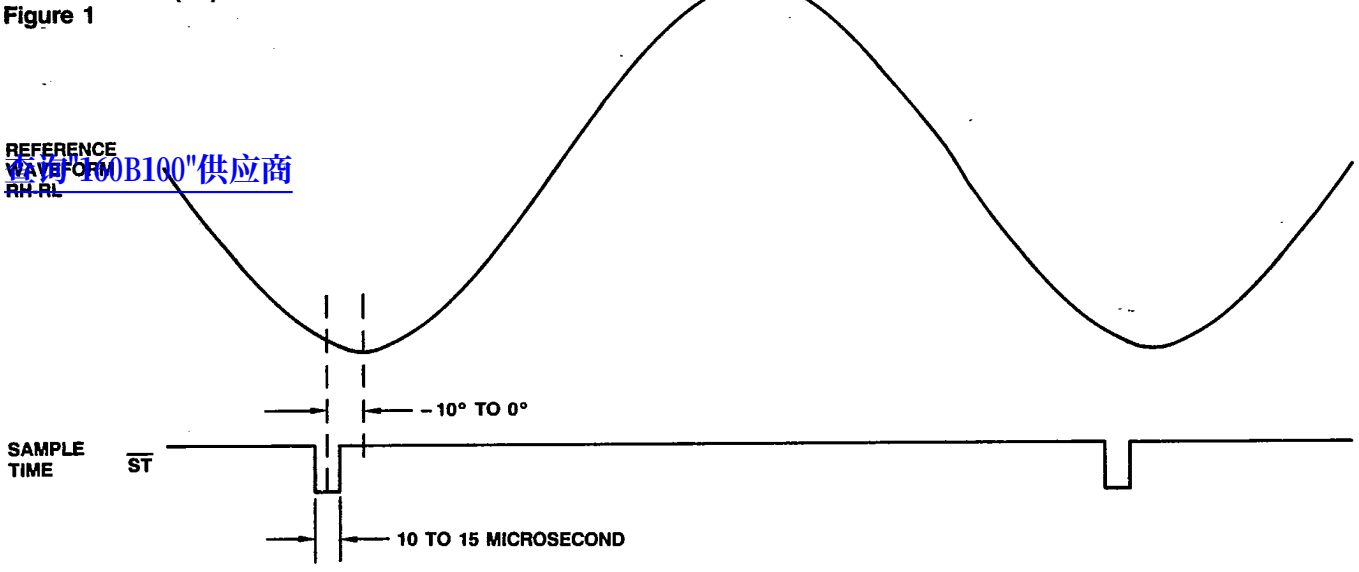
$$\text{maximum number of conversions/cycle} = \frac{\text{minimum period - 15 } \mu s}{100\ \mu s}$$

Channel selection is accomplished by means of a 3-bit binary address (A, B, & C). C is tied to ground for 4-channel applications. The channel select code must not be changed during a conversion cycle (CB = 1). See table 1 for channel select coding.

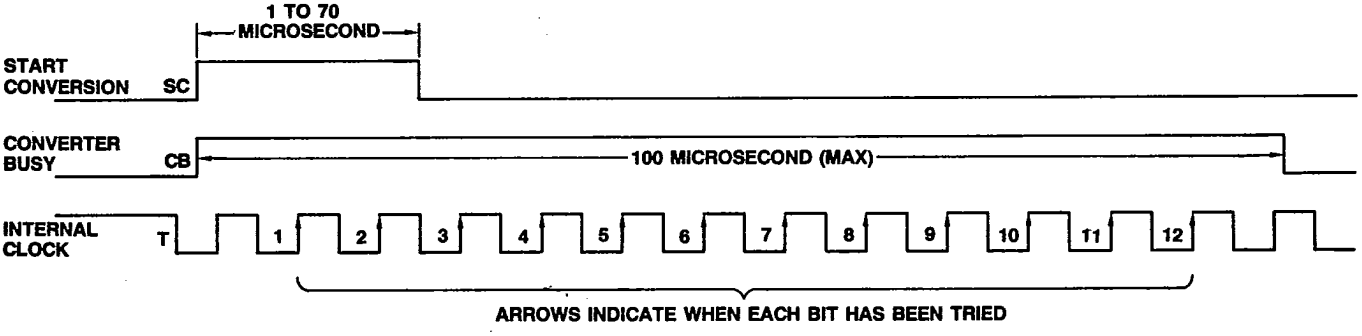
CHANNEL SELECT CODING
Table 1

A	B	C	SELECT CHANNEL
0	0	0	1
1	0	0	2
0	1	0	3
1	1	0	4

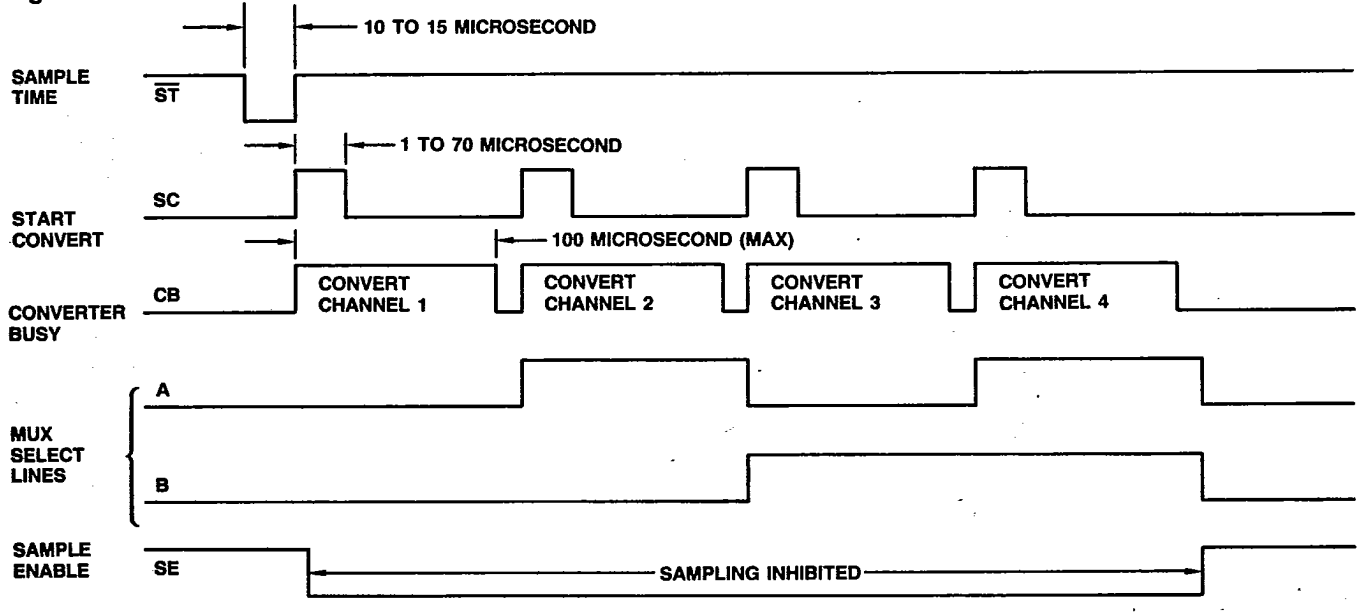
Figure 1



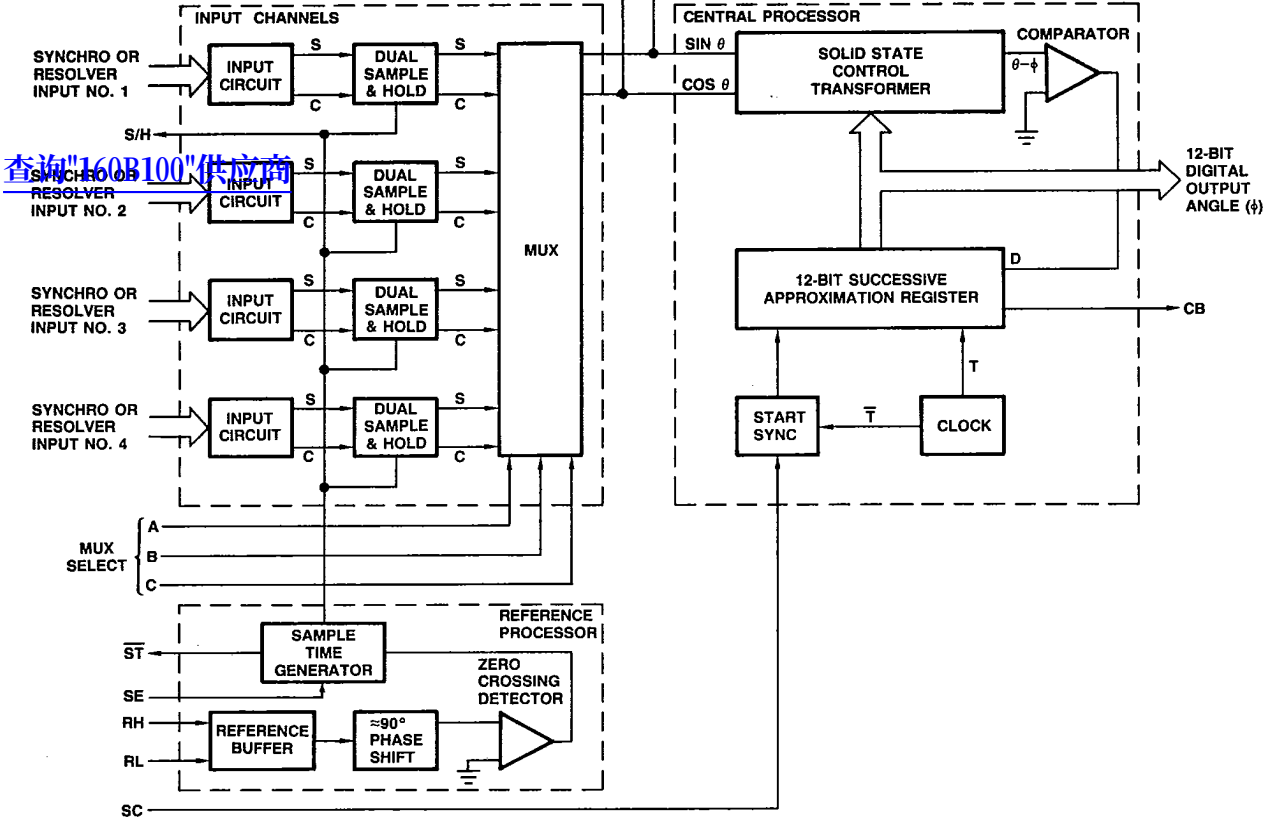
CENTRAL PROCESSOR TIMING
Figure 2



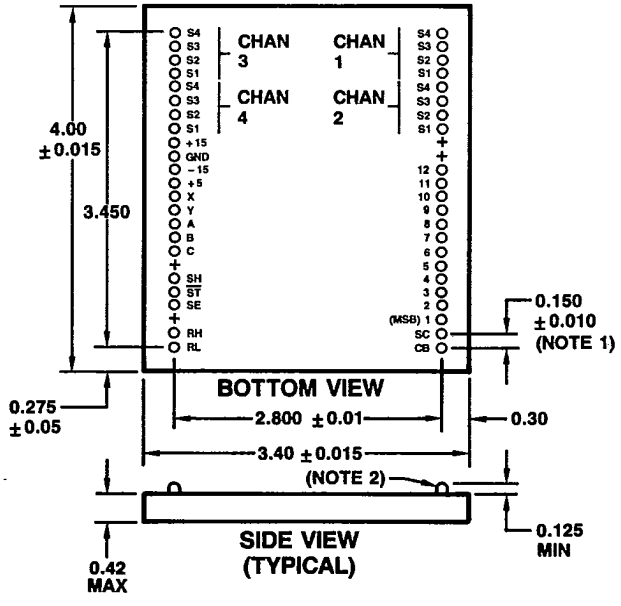
TIMING DIAGRAM
Figure 3



3



MECHANICAL OUTLINE



NOTES:

1. Noncumulative.
2. Rigid 0.040 diameter pins for solder-in or plug-in applications.
3. Dimensions are in inches unless otherwise specified.

ORDERING INFORMATION

160B Suffix	Input Type	Reference Voltage	L-L Voltage	Frequency
100	SYNC	115V	90V	60 Hz
101	SYNC	115V	90V	400 Hz
102	SYNC	26V	11.8V	400 Hz
103	RSVR	26V	11.8V	400 Hz
104	SYNC	26V	11.8V	2.6 kHz
105	RSVR	26V	11.8V	2.6 kHz
106	RSVR	26V	11.8V	5 kHz

The above ordering information lists only the most popular voltages and frequencies; for other voltages and frequencies consult factory for part number assignment.

WARRANTY

All units warranted against defects in materials and workmanship for 1 year from date of shipment. Liability is limited to servicing, adjusting, or replacing any CSI product returned to our factory with delivery charges prepaid. In no case shall our liability exceed the original purchase price.

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