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ANALOG DEVICES INC

65E D

# CMOS Dual 8-Bit Buffered Multiplying DAC

## AD7528

### 1.1 Scope.

This specification covers the detail requirements for a monolithic dual 8-bit CMOS multiplying digital-to-analog converter with on-chip latches for each DAC to allow easy microprocessor interface.

### 1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number <sup>1</sup>
-1	AD7528S(X)/883B
-2	AD7528T(X)/883B
-3	AD7528U(X)/883B

#### NOTE

<sup>1</sup>See paragraph 1.2.3 for package identifier.

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

### 1.3 Absolute Maximum Ratings. (T<sub>A</sub> = 25°C unless otherwise noted)

V <sub>DD</sub> to AGND	0V, +17V
V <sub>DD</sub> to DGND	0V, +17V
AGND to DGND	-0.3V, V <sub>DD</sub> + 0.3V
DGND to AGND	V <sub>DD</sub>
Digital Input Voltage to DGND	-0.3V to +15V
V <sub>FIN2</sub> , V <sub>FIN20</sub> to AGND	-0.3V to +15V
V <sub>REFA</sub> , V <sub>REFB</sub> to AGND	±25V
V <sub>RFBA</sub> , V <sub>RFBB</sub> to DGND	±25V
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

### 1.5 Thermal Characteristics.

Thermal Resistance  $\theta_{JC} = 35^\circ\text{C/W}$  for Q-20 and E-20A  
 $\theta_{JA} = 120^\circ\text{C/W}$  for Q-20 and E-20A

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Table 1.

Test	Symbol	Device	Design Limit T <sub>min</sub> -T <sub>max</sub>	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition <sup>1</sup> V <sub>DD</sub> = +15V	Units
Resolution	RES	-1, 2, 3	8					Bits
Relative Accuracy	RA	-1	1	1	1			± LSB max
		-2	1/2	1	1/2	1/2		
		-3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	-1, 2, 3	1	1	1		All Grades Guaranteed Monotonic to 8 Bits Over Operating Temperature Range	± LSB max
Gain Error <sup>2</sup>	A <sub>E</sub>	-1	5	4	5			± LSB max
		-2	3	4	3	2		
		-3	1	4	1	1		
Gain Tempo	dA <sub>E</sub> /dT	-1, 2, 3	35					± ppm/°C max
Power Supply Rejection	PSRR	-1, 2, 3	0.02	0.01	0.02		ΔV <sub>DD</sub> = ±5%	± %/°C max
Output Leakage Current Pin 2	I <sub>OL</sub>	-1, 2, 3	200	50	200		DAC Latches Loaded with 0000 0000.	± nA max
Pin 20	I <sub>OL</sub>	-1, 2, 3	200	50	200		DAC Latches Loaded with 0000 0000.	± nA max
Output Current Settling Time	t <sub>SL</sub>	-1, 2, 3	350				To ± 1/2LSB; R <sub>OUTA</sub> /R <sub>OUTB</sub> = 100Ω; C <sub>OUTA</sub> /C <sub>OUTB</sub> = 13pF; $\overline{WR} = \overline{CS} = 0V$ ; DB0-DB7 = 0V to V <sub>DD</sub> or V <sub>DD</sub> to 0V.	ns max
Feedthrough Error <sup>3</sup> V <sub>REFA</sub> to OUTA V <sub>REFB</sub> to OUTB	FTE	-1, 2, 3	55				V <sub>REFA</sub> /V <sub>REFB</sub> = ± 10V, 100kHz Sinewave; DAC Latches Loaded with 0000 0000.	- dB max
	FTE	-1, 2, 3	55					
Channel-to-Channel Isolation V <sub>REFA</sub> to OUTB V <sub>REFB</sub> to OUTA	V <sub>CT</sub>	-1, 2, 3	60				V <sub>REFA</sub> = ± 10V, 100kHz Sinewave; V <sub>REFB</sub> = 0V.	- dB max
		-1, 2, 3	60				V <sub>REFB</sub> = ± 10V, 100kHz Sinewave; V <sub>REFA</sub> = 0V.	- dB max
Reference Input Resistance V <sub>REFA</sub> , V <sub>REFB</sub>	R <sub>I</sub>	-1, 2, 3	8					kΩ min
			15					kΩ max
Reference Input Resistance Match	RM <sub>IN</sub>	-1, 2, 3	1	1	1			± % max
Digital Input High Voltage	V <sub>IH</sub>	-1, 2, 3	13.5	13.5	13.5			V min
Digital Input Low Voltage	V <sub>IL</sub>	-1, 2, 3	1.5	1.5	1.5			V max
Digital Input Leakage Current	I <sub>IN</sub>	-1, 2, 3	10	1	10		V <sub>IN</sub> = 0V or V <sub>DD</sub>	± μA max
Digital Input Capacitance DB0-DB7 WR, CS, DACA/DACB	C <sub>I</sub>	-1, 2, 3	10					pF max
			15					
Output Capacitance Pin 2 Pin 20 Pin 2 Pin 20	C <sub>O</sub>	-1, 2, 3	50				DAC Latches Loaded with 0000 0000.	pF max
			50					
	C <sub>O</sub>	-1, 2, 3	120				DAC Latches Loaded with 1111 1111.	pF max
			120					
Supply Current from V <sub>DD</sub>	I <sub>DD</sub>	-1, 2, 3	2				All Digital Inputs = V <sub>IH</sub> or V <sub>IH</sub>	mA max
	I <sub>DD</sub>	-1, 2, 3	500	100	500		All Digital Inputs = 0V or V <sub>DD</sub>	μA max
Chip Select to Write Setup Time <sup>4</sup>	t <sub>CS</sub>	-1, 2, 3	180					ns min
Chip Select to Write Hold Time <sup>4</sup>	t <sub>CH</sub>	-1, 2, 3	10					ns min
DAC Select to Write Setup Time <sup>4</sup>	t <sub>AS</sub>	-1, 2, 3	180					ns min
DAC Select to Write Hold Time <sup>4</sup>	t <sub>AH</sub>	-1, 2, 3	10					ns min
Data Valid to Write Setup Time <sup>4</sup>	t <sub>DS</sub>	-1, 2, 3	180					ns min
Data Valid to Write Hold Time <sup>4</sup>	t <sub>DH</sub>	-1, 2, 3	10					ns min
Write Pulse Width <sup>4</sup>	t <sub>WR</sub>	-1, 2, 3	180					ns min

NOTES

<sup>1</sup>V<sub>OUTA</sub> = V<sub>OUTB</sub> = 0V; V<sub>REF</sub> = +10V unless otherwise stated.

<sup>2</sup>Measured using internal R<sub>FB</sub> and includes effect of leakage current and gain TC.

<sup>3</sup>Feedthrough error can be reduced by connecting the lid on the package to ground.

<sup>4</sup>Timing per Figure 1.

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Table 2.

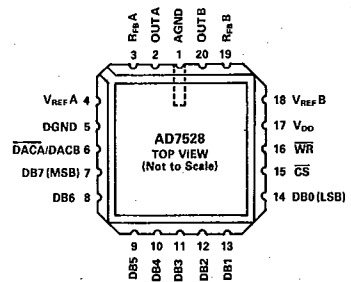
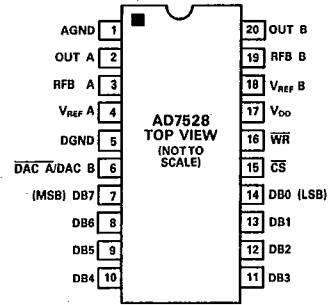
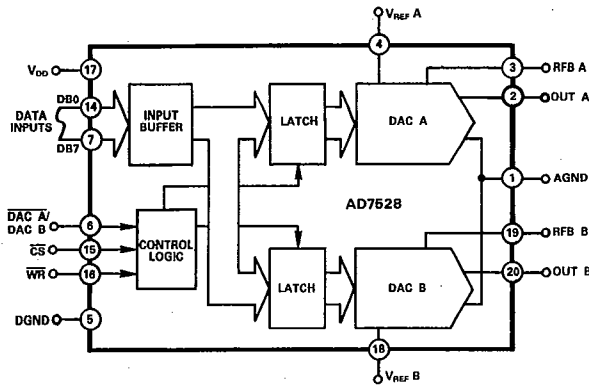
Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition <sup>1</sup> $V_{DD} = +5V$	Units
Resolution	RES	-1,2,3	8					Bits
Relative Accuracy	RA	-1	1	1	1			± LSB max
		-2	1/2	1	1/2	1/2		
		-3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	-1,2,3	1	1	1	All Grades Guaranteed Monotonic to 8 Bits Over Operating Temperature Range	± LSB max	
Gain Error <sup>2</sup>	$A_E$	-1	6	4	6			± LSB max
		-2	4	4	4	2		
		-3	3	4	3	1		
Gain Tempco	$dA_E/dT$	-1,2,3	70				± ppm/°C max	
Power Supply Rejection	PSRR	-1,2,3	0.04	0.02	0.04	$\Delta V_{DD} = \pm 5\%$	± %/% max	
Output Leakage Current Pin 2	$I_{OL}$	-1,2,3	400	50	400	DAC Latches Loaded with 0000 0000.	± nA max	
Pin 20	$I_{OL}$	-1,2,3	400	50	400	DAC Latches Loaded with 0000 0000.	± nA max	
Output Current Settling Time	$t_{SL}$	-1,2,3	600			To ± 1/2LSB; $R_{OUTA}/R_{OUTB} = 100\Omega$ , $C_{OUTA}/C_{OUTB} = 13pF$ ; $\overline{WR} = \overline{CS} = 0V$ ; DB0-DB7 = 0V to $V_{DD}$ or $V_{DD}$ to 0V.	ns max	
Feedthrough Error <sup>3</sup> $V_{REFA}$ to $V_{OUTA}$ $V_{REFB}$ to $V_{OUTB}$	FTE	-1,2,3	55			$V_{REFA}/V_{REFB} = \pm 10V$ , 100kHz Sinewave; DAC Latches Loaded with 0000 0000.	-dB max	
	FTE	-1,2,3	55					
Channel-to-Channel Isolation $V_{REFA}$ to $V_{OUTB}$	$V_{CT}$	-1,2,3	60			$V_{REFA} = \pm 10V$ , 100kHz Sinewave; $V_{REFB} = 0V$ .	-dB max	
		$V_{REFB}$ to $V_{OUTA}$	-1,2,3	60			$V_{REFB} = \pm 10V$ , 100kHz Sinewave; $V_{REFA} = 0V$ .	-dB max
Reference Input Resistance $V_{REFA}$ , $V_{REFB}$	$R_I$	-1,2,3	8	8	8		kΩ min	
			15	15	15		kΩ max	
Reference Input Resistance Match	$RM_{IN}$	-1,2,3	1				± % max	
Digital Input High Voltage	$V_{IH}$	-1,2,3	2.4	2.4	2.4		V min	
Digital Input Low Voltage	$V_{IL}$	-1,2,3	0.8	0.8	0.8		V max	
Digital Input Leakage Current	$I_{IN}$	-1,2,3	10			$V_{IN} = 0V$ or $V_{DD}$	± μA max	
Digital Input Capacitance DB0-DB7 $\overline{WR}$ , $\overline{CS}$ , $DACA/DACB$	$C_I$	-1,2,3	10				pF max	
			15					
Output Capacitance Pin 2 Pin 20	$C_O$	-1,2,3	50			DAC Latches Loaded with 0000 0000.	pF max	
		-1,2,3	50					
Pin 2 Pin 20	$C_O$	-1,2,3	120			DAC Latches Loaded with 1111 1111.	pF max	
		-1,2,3	120					
Supply Current from $V_{DD}$	$I_{DD}$	-1,2,3	2	2	2	All Digital Inputs = $V_{IL}$ or $V_{IH}$ All Digital Inputs = 0V or $V_{DD}$	mA max	
		-1,2,3	500				μA max	
Chip Select to Write Setup Time <sup>4</sup>	$t_{CS}$	-1,2,3	250				ns min	
Chip Select to Write Hold Time <sup>4</sup>	$t_{CH}$	-1,2,3	20				ns min	
DAC Select to Write Setup Time <sup>4</sup>	$t_{AS}$	-1,2,3	250				ns min	
DAC Select to Write Hold Time <sup>4</sup>	$t_{AH}$	-1,2,3	20				ns min	
Data Valid to Write Setup Time <sup>4</sup>	$t_{DS}$	-1,2,3	220				ns min	
Data Valid to Write Hold Time <sup>4</sup>	$t_{DH}$	-1,2,3	10				ns min	
Write Pulse Width <sup>4</sup>	$t_{WR}$	-1,2,3	220				ns min	

## NOTES

<sup>1</sup> $V_{OUTA} = V_{OUTB} = 0V$ ;  $V_{REF} = +10V$  unless otherwise stated.<sup>2</sup>Measured using internal  $R_{FB}$  and includes effect of leakage current and gain TC.<sup>3</sup>Feedthrough error can be reduced by connecting the lid on the package to ground.<sup>4</sup>Timing per Figure 1.

### 3.2.1 Functional Block Diagram and Terminal Assignments.

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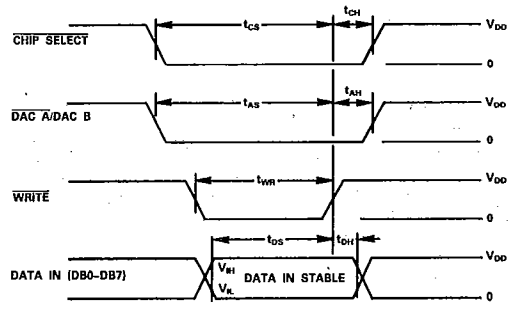
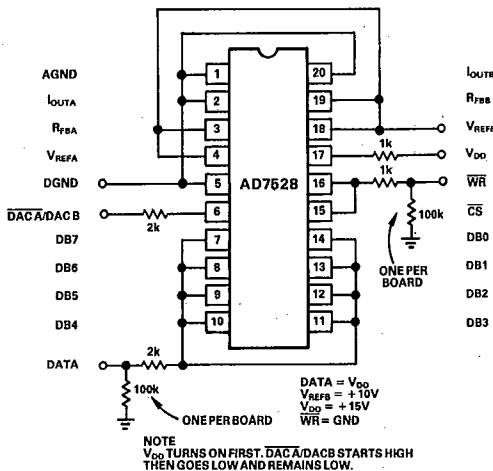


### 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

### 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



- NOTES:  
 1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF  $V_{DD}$ .  
 $V_{DD} = +5V, t_r = t_f = 20ns$ ;  
 $V_{DD} = +15V, t_r = t_f = 40ns$ .  
 2. TIMING MEASUREMENT REFERENCE LEVEL IS  $\frac{V_{HI} + V_{LI}}{2}$

Figure 1. Write Cycle Timing Diagram

Table 3. Mode Selection Table

DAC A/ DAC B	CS	WR	DACA	DACB
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care