RAD-TOLERANT CLASS-V, HIGH-SPEED PWM CONTROLLER

FEATURES

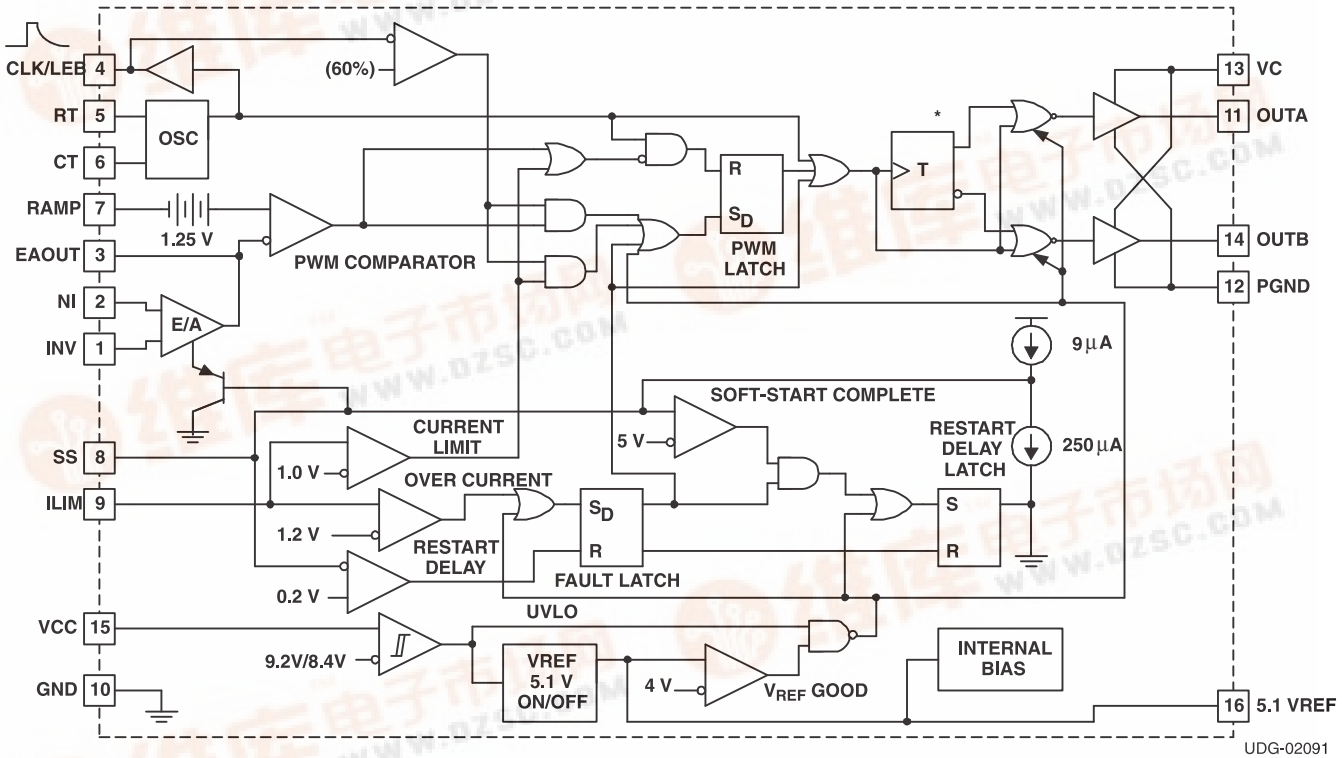
- **QML-V Qualified, SMD 5962-87681**
- **Rad-Tolerant: 30 kRad (Si) TID** (1)
- **Compatible With Voltage-Mode or Current-Mode Control Methods**
- **Practical Operation at Switching Frequencies to 1 MHz**
- **50-ns Propagation Delay to Output**
- **High-Current Dual Totem Pole Outputs (2-A Peak)**
- **Trimmed Oscillator Discharge Current**
- **Low 100-μA Startup Current**
- **Pulse-by-Pulse Current Limiting Comparator**
- **Latched Overcurrent Comparator With Full Cycle Restart**

(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.

DESCRIPTION

The UC1825A PWM controller is an improved version of the standard UC1825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12 MHz, while input offset voltage is 2 mV. Current limit threshold is assured to a tolerance of 5%. Oscillator discharge current is specified at 10 mA for accurate dead time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100 μA, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the startup current specification. In addition each output is capable of 2-A peak currents during transitions.

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This device has limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Functional improvements have also been implemented in this family. The UC1825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2 V. The overcurrent comparator sets a latch that ensures full discharge of the soft-start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft-start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC1825 CLOCK pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

The UC1825A has dual alternating outputs and the same pin configuration of the UC1825. *A* version parts have UVLO thresholds identical to the original UC1825.

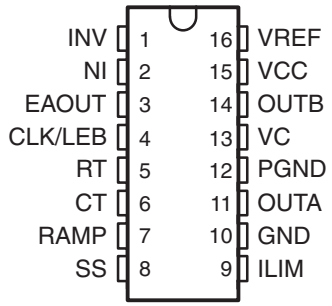
ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP-16	5962-8768105VEA	UC1825AJ-SP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN ASSIGNMENTS

J PACKAGE
(TOP VIEW)



THERMAL INFORMATION

PACKAGE	θ_{JA}	θ_{JC}
J-16	80-120	28(1)

(1) θJC data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states, "The baseline values shown are worst case (mean + 2s) for a 60 x 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die size greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W".

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CLK/LEB	4	O	Output of the internal oscillator
CT	6	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.
EAOUT	3	O	Output of the error amplifier for compensation
GND	10		Analog ground return pin
ILIM	9	I	Input to the current limit comparator
INV	1	I	Inverting input to the error amplifier
NI	2	I	Non-inverting input to the error amplifier
OUTA	11	O	High current totem pole output A of the on-chip drive stage.
OUTB	14	O	High current totem pole output B of the on-chip drive stage.
PGND	12		Ground return pin for the output driver stage
RAMP	7	I	Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation, this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input.
RT	5	I	Timing resistor connection pin for oscillator frequency programming
SS	8	I	Soft-start input pin which also doubles as the maximum duty cycle clamp.
VC	13		Power supply pin for the output stage. This pin should be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor with minimal trace lengths.
VCC	15		Power supply pin for the device. This pin should be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor with minimal trace lengths
VREF	16	O	5.1-V reference. For stability, the reference should be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			VALUE	UNIT
V_{IN}	Supply voltage,	VC, VCC	22	V
I_O	Source or sink current,DC	OUTA, OUTB	0.5	A
I_O	Source or sink current, pulse (0.5 µs)	OUTA, OUTB	2.2	A
	Analog inputs	INV, NI, RAMP	–0.3 to 7	V
		ILIM, SS	–0.3 to 6	V
	Power ground	PGND	±0.2	V
	Outputs	OUTA, OUTB	P_{GND} - 0.3 to V_C + 0.3	V
I_{CLK}	Clock output current	CLK/LEB	–5	mA
$I_{O(EA)}$	Error amplifier output current	EAOUT	5	mA
I_{SS}	Soft-start sink current	SS	20	mA
I_{OSC}	Oscillator charging current	RT	–5	mA
T_J	Operating virtual junction temperature range		–55 to 150	°C
T_{STG}	Storage temperature		–65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds		300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (T_A = T_J = –55°C to 125°C), unless otherwise noted.

		MIN	MAX	UNIT
V_{CC}	Supply voltage	12	20	V
	Sink/source output current (continuous or time average)	0	100	mA
	Reference load current	0	10	mA

ELECTRICAL CHARACTERISTICS

T_A = –55°C to 125°C, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 12 V, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE, V_{REF}						
V_O	Ouput voltage range	T_J = 25°C, I_O = 1 mA	5.05	5.1	5.15	V
	Line regulation	12 V ≤ VCC ≤ 20 V		2	15	mV
	Load regulation	1 mA ≤ I_O ≤ 10 mA		5	20	mV
	Total output variation	Line, load, temperature	5.03		5.17	V
	Temperature stability(1)	$T_{(min)}$ < T_A < $T_{(max)}$		0.2	0.4	mV/°C
	Output noise voltage	10 Hz < f < 10 kHz		50		μV_{RMS}
	Short circuit current	VREF = 0 V	30	60	90	mA
OSCILLATOR						
f_{OSC}	Initial accuracy(1)	T_J = 25°C	375	400	425	kHz
		R_T = 6.6 kΩ, C_T = 220 pF, T_A = 25°C	0.9	1	1.1	MHz
	Total variation(1)	Line, temperature	350		450	kHz
		R_T = 6.6 kΩ, C_T = 220 pF	0.82		1.18	MHz
	Voltage stability	12 V < VCC < 20 V			1%	
	Temperature stability	$T_{(min)}$ < T_A < $T_{(max)}$		±5%		
	High-level output voltage, clock		3.7	4		V
	Low-level output voltage, clock			0	0.2	V
	Ramp peak		2.6	2.8	3	V
	Ramp valley		0.7	1	1.25	V
	Ramp valley-to-peak		1.55	1.8	2	V
I_{OSC}	Oscillator discharge current	R_T = OPEN, V_{CT} = 2 V	8.5	10	11	mA
ERROR AMPLIFIER						
	Input offset voltage			2	10	mV
	Input bias current			0.6	3	µA
	Input offset current			0.1	1	µA
	Open loop gain	1 V < V_O < 4 V	60	95		dB
CMRR	Common mode rejection ratio	1.5 V < V_{CM} < 5.5 V	75	95		dB
PSRR	Power supply rejection ratio	12 V < V_{CC} < 20 V	85	110		dB
$I_{O(sink)}$	Output sink current	V_{EAOUT} = 1 V	1	2.5		mA
$I_{O(src)}$	Output source current	V_{EAOUT} = 4 V	–0.5	–1.3		mA
	High-level output voltage	I_{EAOUT} = –0.5 mA	4.5	4.7	5	V
	Low-level output voltage	I_{EAOUT} = –1 mA	0	0.5	1	V
	Gain bandwidth product(1)	f = 200 kHz	6	12		Mhz
	Slew rate(1)		5	7		V/µs

(1) Parameters ensured by design and/or characterization, if not production tested.

ELECTRICAL CHARACTERISTICS (Continued)

T_A = –55°C to 125°C, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 12 V, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIIONS	MIN	TYP	MAX	UNIT
PWM COMPARATOR						
I_{BIAS}	Bias current, RAMP	V_{RAMP} = 0 V		–1	–8	µA
	Minimum duty cycle				0%	
	Maximum duty cycle		85%			
t_{LEB}	Leading edge blanking time	R_{LEB} = 2 kΩ, C_{LEB} = 470 pF	300	375	450	ns
R_{LEB}	Leading edge blanking resistance	$V_{CLK/LEB}$ = 3 V	8.5	10.0	11.5	kΩ
V_{ZDC}	Zero dc threshold voltage, EAOUT	V_{RAMP} = 0 V	1.10	1.25	1.4	V
t_{DELAY}	Delay-to-output time(1)	V_{EAOUT} = 5 V to 0 V step		50	120	ns
CURRENT LIMIT / START SEQUENCE / FAULT						
I_{SS}	Soft-start charge current	V_{SS}= 2.5 V	8	14	20	µA
V_{SS}	Full soft-start threshold voltage		4.3	5		V
I_{DSCH}	Restart discharge current	V_{SS}= 2.5 V	100	250	350	µA
I_{SS}	Restart threshold voltage			0.3	0.5	V
I_{BIAS}	ILIM bias current	0 V ≤ V_{ILIM} ≤ 1.5 V			15	µA
I_{CL}	Current limit threshold voltage		0.95	1	1.05	V
	Overcurrent threshold voltage		1.14	1.2	1.26	
t_d	Delay-to-output time, ILIM(1)	V_{ILIM} = 0 V to 2 V step		50	80	ns
OUTPUT						
	Low-level output saturation voltage	I_{OUT} = 20 mA		0.25	0.45	V
		I_{OUT} = 200 mA		1.2	2.2	
	High-level output saturation voltage	I_{OUT} = -20 mA		1.9	2.9	
		I_{OUT} = -200 mA		2	3	
t_r, t_f	Rise/fall time(1)	C_L = 1 nF		20	45	ns
UNDERVOLTAGE LOCKOUT (UVLO)						
	Start threshold voltage		8.3	9.2	9.6	V
	UVLO hysteresis		0.4	0.8	1.25	
SUPPLY CURRENT						
I_{su}	Startup current	VC = VCC = 8 V		100	300	µA
I_{CC}	Input current			28	36	mA

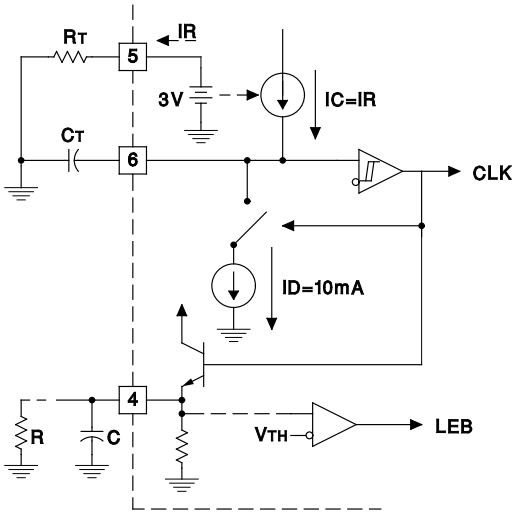
(1) Parameters ensured by design and/or characterization, if not production tested.

APPLICATION INFORMATION

The oscillator of the UC1825A is a saw tooth. The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin (C_{CT}). The falling edge of the sawtooth sets dead time for the outputs. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on the desired frequency (RT) and D_{MAX}. The design equations are:

$$R_T = \frac{3\ V}{(10\ mA) \times \left(1 - D_{MAX}\right)} \qquad C_T = \frac{\left(1.6 \times D_{MAX}\right)}{\left(R_T \times f\right)} \tag{1}$$

Recommended values for R_T range from 1 kΩ to 100 kΩ. Control of D_{MAX} less than 70% is not recommended.



UDG-95102

Figure 1. Oscillator

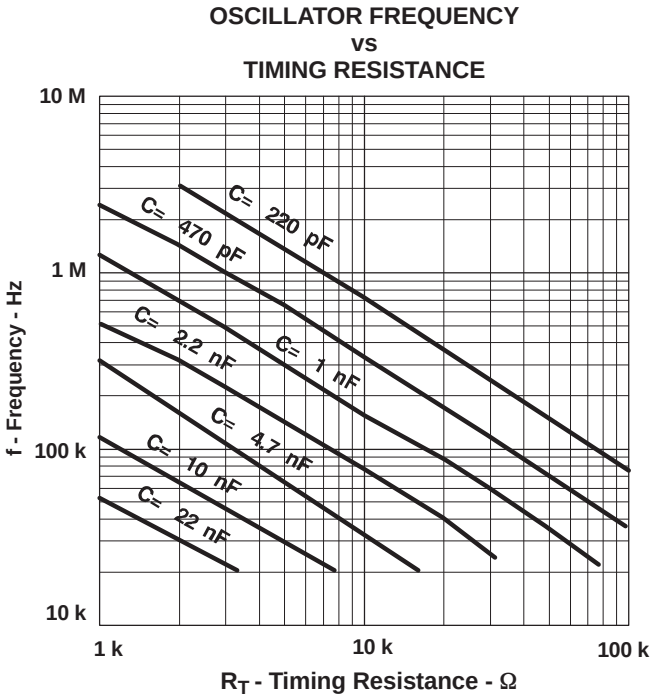


Figure 2.

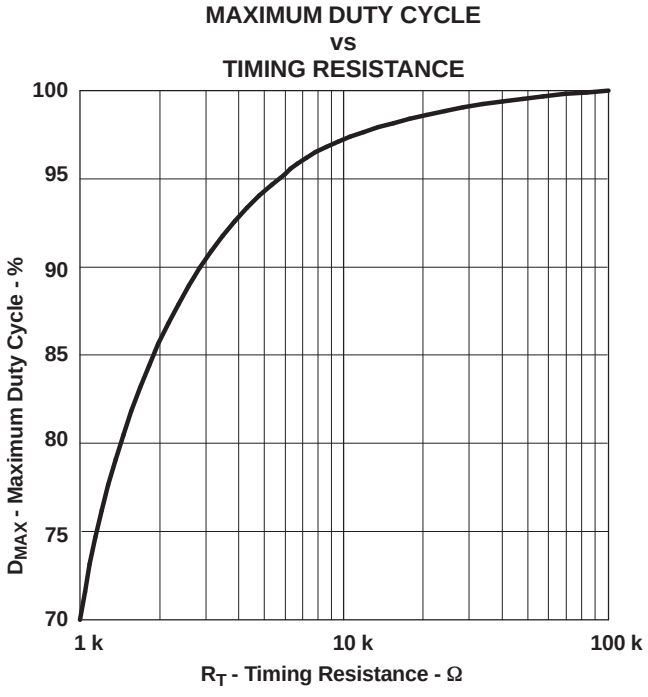


Figure 3.

LEADING EDGE BLANKING

The UC1825A performs fixed frequency pulse width modulation control. The UC1825A outputs are alternately controlled. During every other cycle, one output is off. Each output then switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

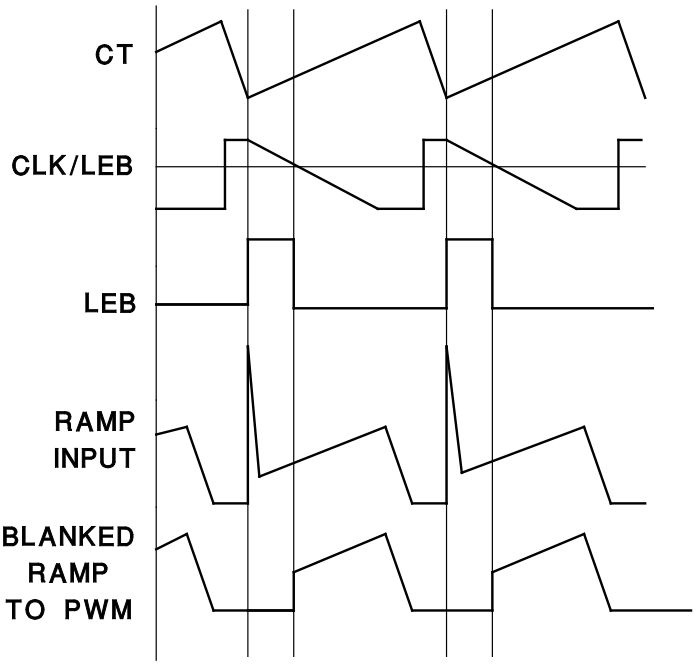
Normally the PWM comparator senses a ramp crossing a control voltage (error amplifier output) and terminates the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

To program a leading edge blanking (LEB) period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10-kΩ resistor determines the blanked interval. The 10-kΩ resistor has a 10% tolerance. For more accuracy, an external 2-kΩ 1% resistor (R) can be added, resulting in an equivalent resistance of 1.66 kΩ with a tolerance of 2.4%. The design equation is:

$$t_{LEB} = 0.5 \times (R \parallel 10\ k\Omega) \times C \quad (2)$$

Values of R less than 2 kΩ should not be used.

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the 1-V threshold, the pulse is terminated. The overcurrent comparator, however, is not blanked. It catches catastrophic overcurrent faults without a blanking delay. Any time the ILIM pin exceeds 1.2 V, the fault latch is set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.



UDG-95105

Figure 4. Leading Edge Blanking Operational Waveforms

UVLO, SOFT-START AND FAULT MANAGEMENT

Soft-start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amplifier output is also forced low. While the internal 9-μA source charges the SS pin, the error amplifier output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2 V, the fault latch is set and the output pins are driven low. The soft-start cap is then discharged by a 250-µA current sink. No more output pulses are allowed until soft-start is fully discharged and ILIM is below 1.2 V. At this point the fault latch resets and the chip executes a soft-start.

Should the fault latch get set during soft-start, the outputs are immediately terminated, but the soft-start capacitor does not discharge until it has been fully charged first. This results in a controlled hiccup interval for continuous fault conditions.

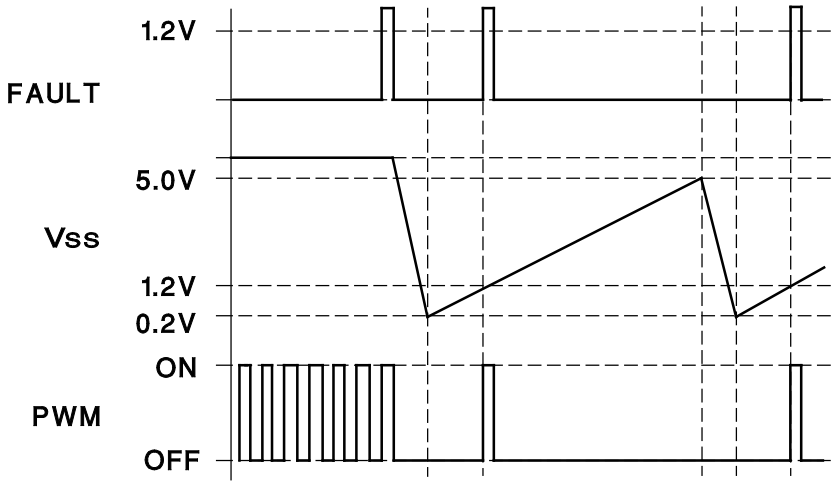


Figure 5. Soft-Start and Fault Waveforms

ACTIVE LOW OUTPUTS DURING UVLO

The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.

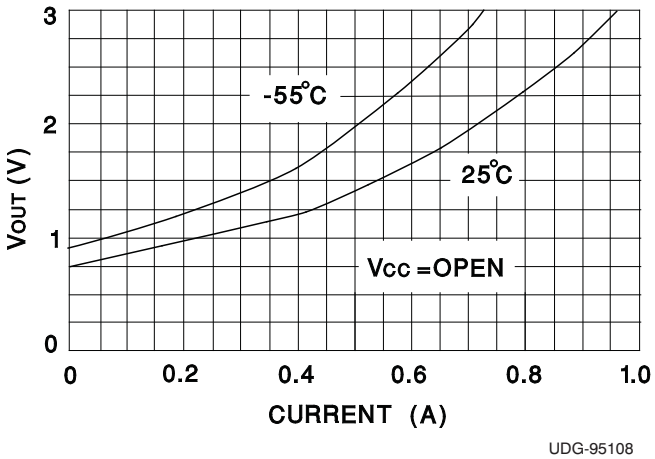


Figure 6. Output Voltage vs Output Current

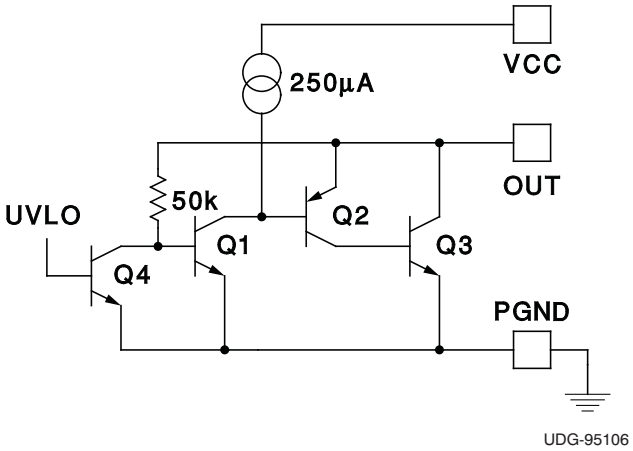


Figure 7. Output V and I During UVLO

CONTROL METHODS

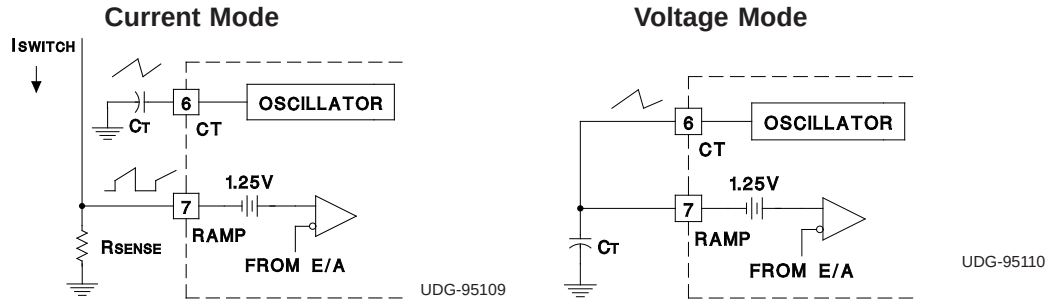


Figure 8. Control Methods

SYNCHRONIZATION

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10 ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that the CLK/LEB pin no longer accepts an incoming synchronizing signal.

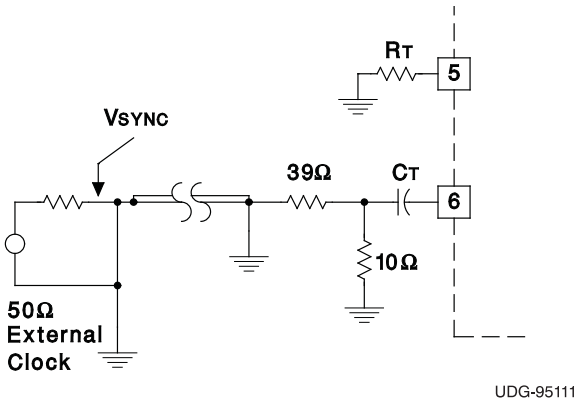


Figure 9. General Oscillator Synchronization

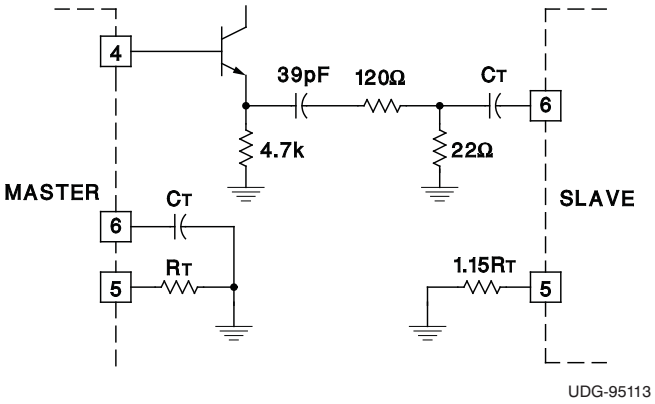


Figure 10. Two Unit Interface

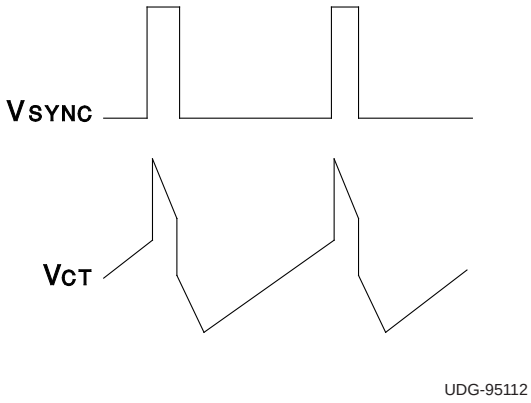


Figure 11. Operational Waveforms

HIGH CURRENT OUTPUTS

Each totem pole output of the UC1825A can deliver a 2-A peak current into a capacitive load. The output can slew a 1000-pF capacitor by 15 V in approximately 20 ns. Separate collector supply (VC) and power ground (PGND) pins help decouple the device's analog circuitry from the high-power gate drive noise. The use of 3-A Schottky diodes (1N5120, USD245, or equivalent) as shown in the Figure 13 from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. DO NOT USE standard silicon diodes.

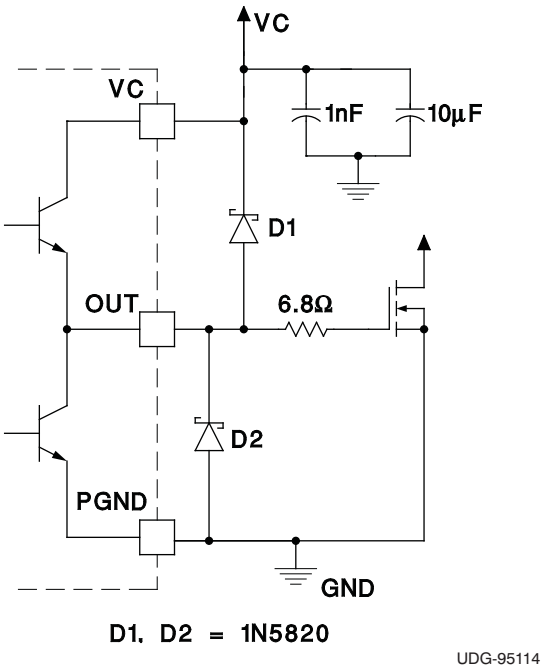


Figure 12. Power MOSFET Drive Circuit

GROUND PLANES

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1-mF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.

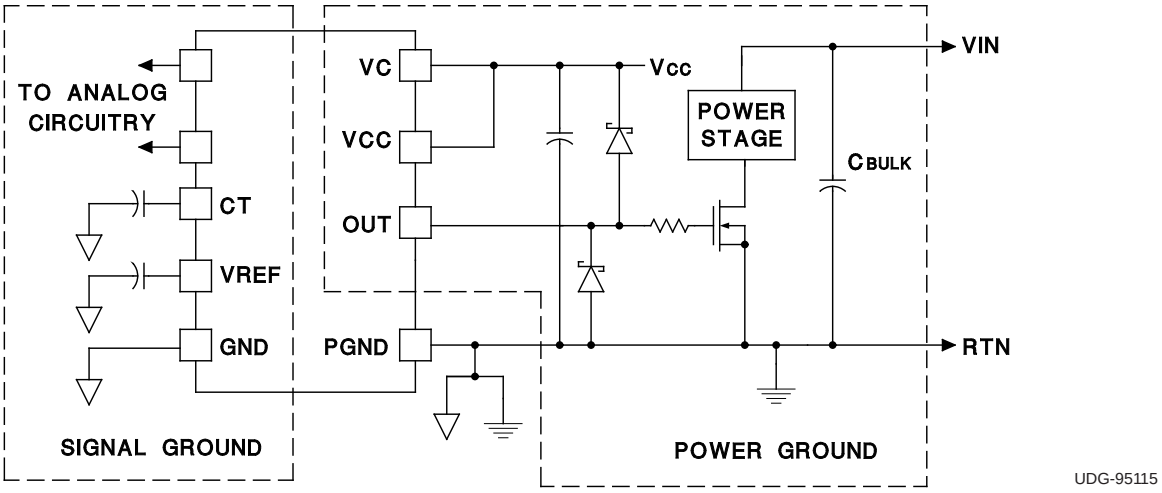


Figure 13. Ground Planes Diagram

OPEN LOOP TEST CIRCUIT

This test fixture is useful for exercising many functions of this device family and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

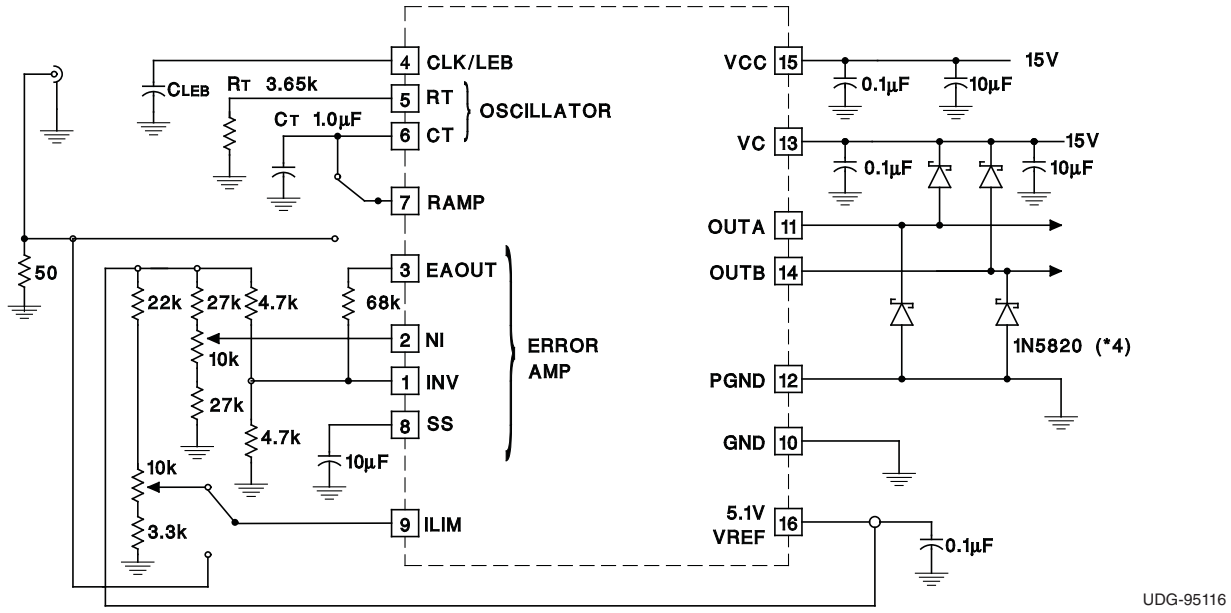


Figure 14. Open Loop Test Circuit Schematic

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-8768102V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8768102VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
5962-8768105VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

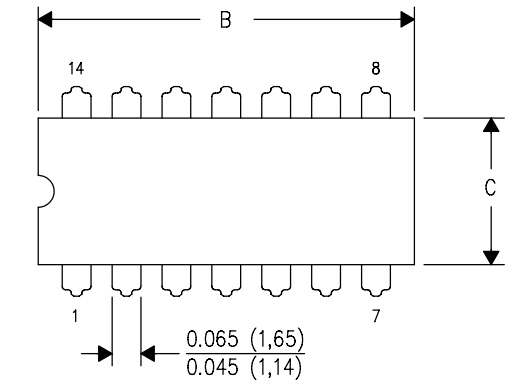
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF UC1825A-SP :
- Catalog: UC1825A

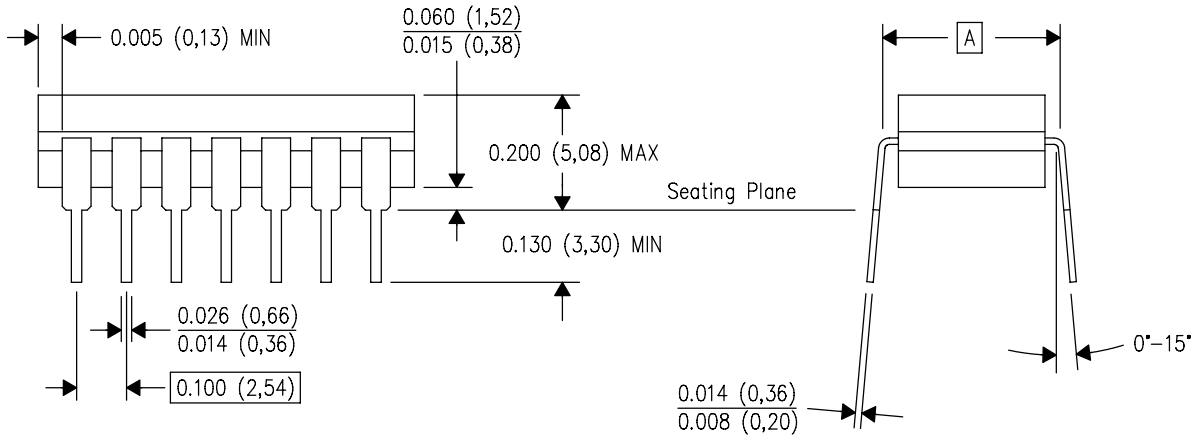
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

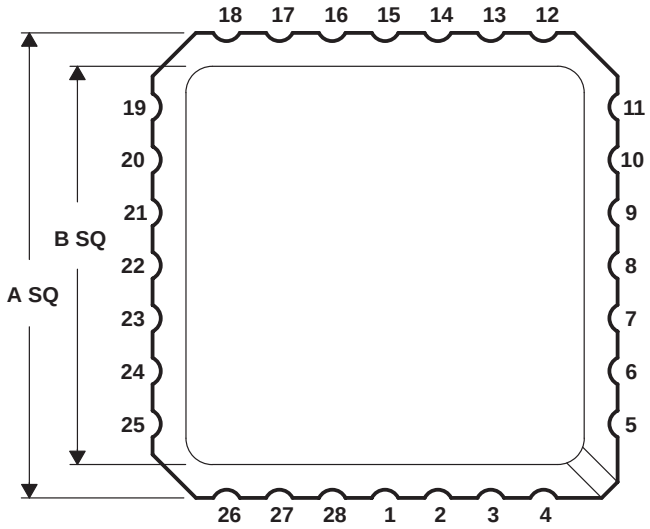


4040083/F 03/03

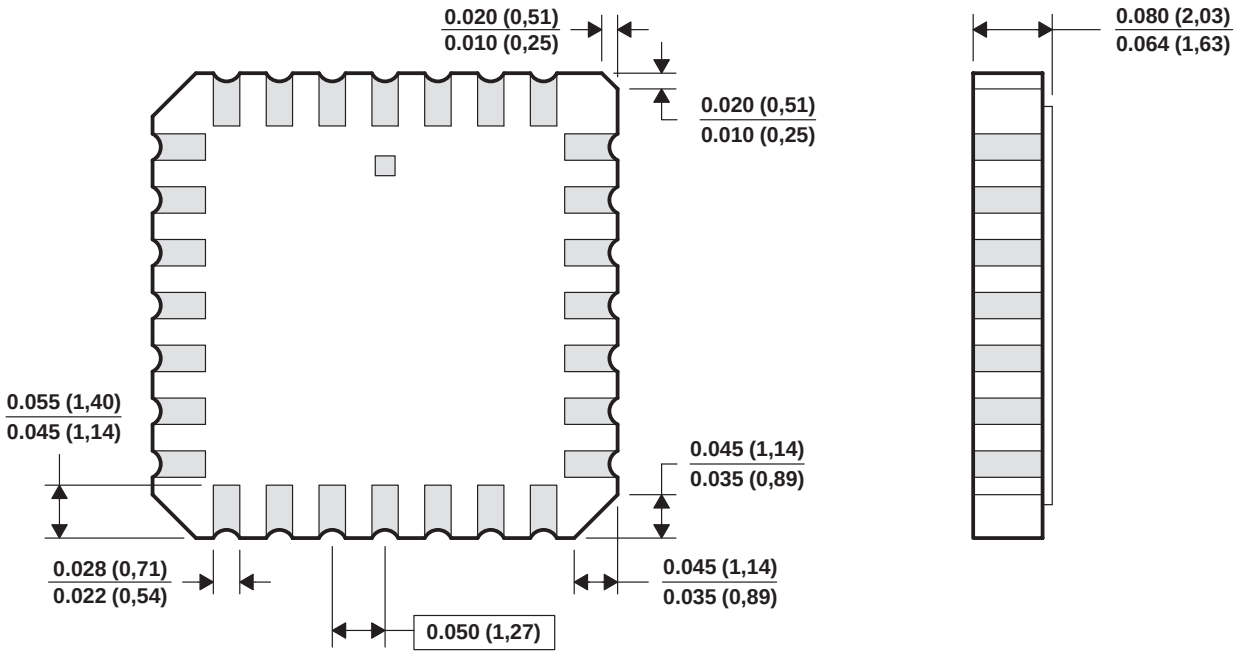
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

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