

## HAT2220R

### Silicon N Channel MOS FET High Speed Power Switching

REJ03G1572-0500

Rev.5.00

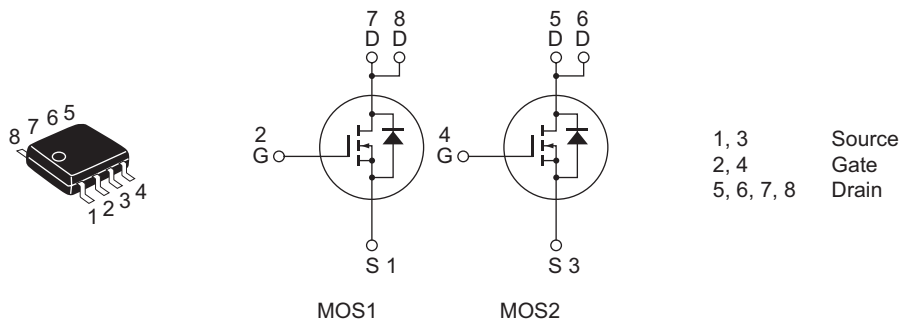
Jul 20, 2007

#### Features

- Low on-resistance
- Low drive current
- High density mounting

#### Outline

RENESAS Package code: PRSP0008DD-D  
(Package name: SOP-8 <FP-8DAV> )



#### Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	450	V
Gate to source voltage	$V_{GSS}$	±30	V
Drain current	$I_D$ <sup>Note1</sup>	0.7	A
Drain peak current	$I_{D(pulse)}$ <sup>Note2</sup>	2.1	A
Body-drain diode reverse drain current	$I_{DR}$	0.7	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	0.7	A
Channel dissipation	$P_{ch}$ <sup>Note4</sup>	2	W
Channel dissipation	$P_{ch}$ <sup>Note5</sup>	3	W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

Notes: 1.  $PW \leq 1$  s

2.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

3.  $ST_{ch} = 25$  °C,  $T_{ch} \leq 150$  °C

4. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10$  s

5. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10$  s

## Electrical Characteristics

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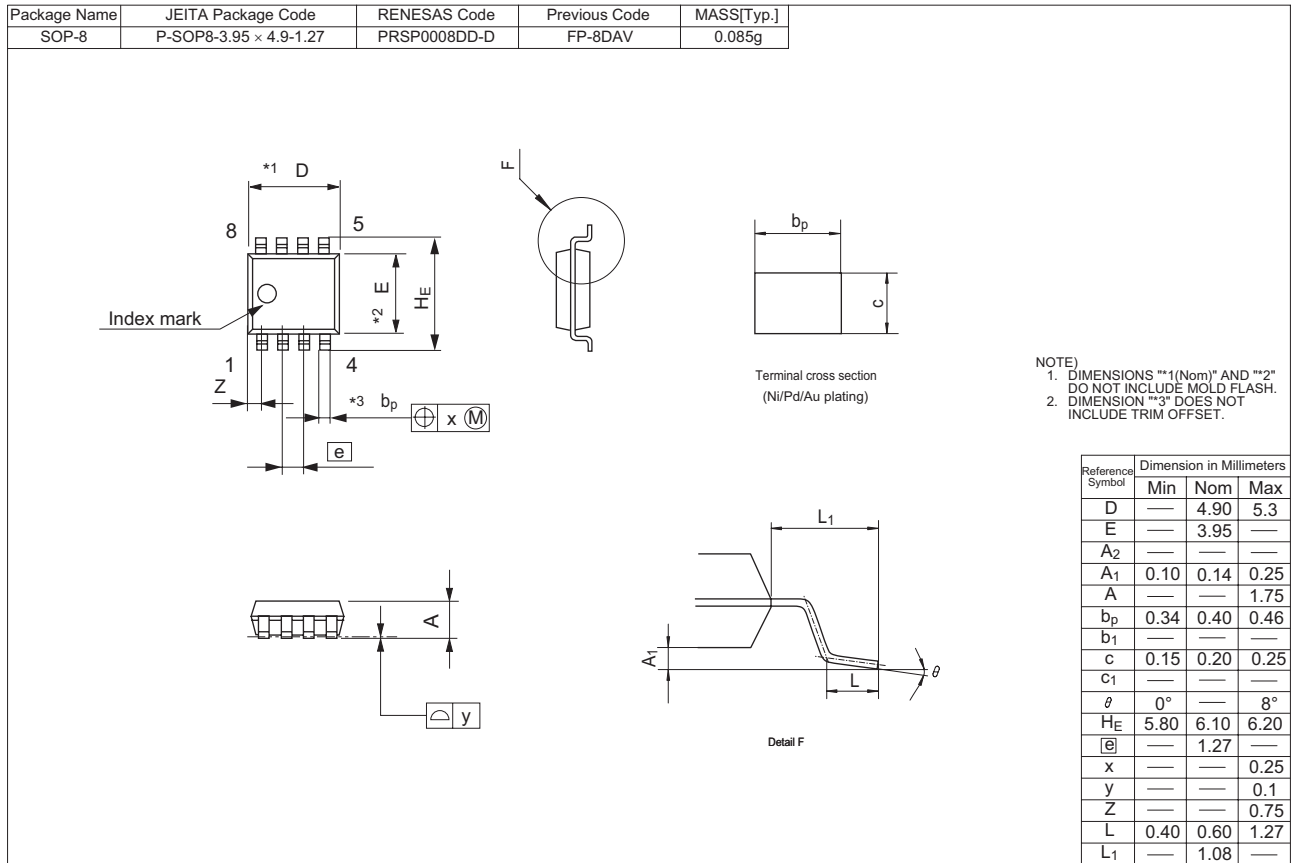
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 450 \text{ V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 30 \text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	0.55	0.95	—	S	$I_D = 0.4 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note6</sup>
Static drain to source on state resistance	$R_{DS(on)}$	—	5.5	6.5	$\Omega$	$I_D = 0.4 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note6</sup>
Input capacitance	$C_{iss}$	—	140	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	17	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	5	—	pF	
Turn-on delay time	$t_{d(on)}$	—	22	—	ns	$I_D = 0.4 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 562 \Omega$ $R_g = 10 \Omega$
Rise time	$t_r$	—	12	—	ns	
Turn-off delay time	$t_{d(off)}$	—	38	—	ns	
Fall time	$t_f$	—	47	—	ns	
Total gate charge	$Q_g$	—	4.9	—	nC	$V_{DD} = 360 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 0.7 \text{ A}$
Gate to source charge	$Q_{gs}$	—	0.6	—	nC	
Gate to drain charge	$Q_{gd}$	—	3.2	—	nC	
Body-drain diode forward voltage	$V_{DF}$	—	0.84	1.24	V	$I_F = 0.7 \text{ A}$ , $V_{GS} = 0$ <sup>Note6</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	120	—	ns	$I_F = 0.7 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 6. Pulse test

7. Since this device includes two high voltage Power MOS FET chips ( $V_{DSS} \geq 450 \text{ V}$ ), high voltage margin may occur. (Between No.6 pin and No.7 pin in the outline fig.) Therefore, please be sure to confirm about Electric discharge between No.6 pin and No.7 pin in the equivalent circuit.

Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
HAT2220R-EL-E	2500 pcs	Taping

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