



SSDI
Solid State Devices, Inc.

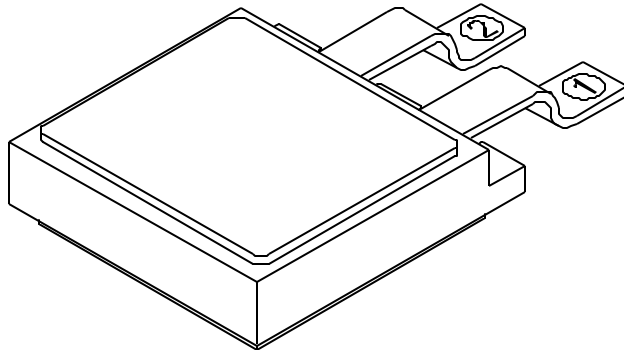
14701 Firestone Blvd * La Mirada, CA 90638

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DESIGNER'S DATA SHEET ^{1/}

CERPACK



SDR623G Thru SDR626G

20A 35nsec 300-600 V Hyper Fast Rectifier

Features:

- Hyper Fast Recovery: 35nsec Maximum ^{3/}
- High Surge Rating
- Low Reverse Leakage Current
- Low Junction Capacitance
- Hermetically Sealed Package
- Gold Eutectic Die Attach
- Ultrasonic Aluminum Wire Bonds
- TX, TXV, and S-Level Screening Available ^{2/}

Maximum Ratings		Symbol	Value	Units
Peak Repetitive Reverse Voltage	SDR623G	V_{RRM}	300	Volts
	SDR624G	V_{RWM}	400	
	SDR625G	V_R	500	
	SDR626G		600	
Average Rectified Forward Current ^{4/} (Resistive Load, 60 Hz Sine Wave, $T_A = 25^\circ\text{C}$)		I_o	20	Amps
Peak Surge Current ^{4/} (8.3 ms Pulse, Half Sine Wave, $T_A = 25^\circ\text{C}$)		I_{FSM}	200	Amps
Operating & Storage Temperature		$T_{OP} \text{ \& } T_{STG}$	-65 to +200	$^\circ\text{C}$
Maximum Total Thermal Resistance Junction to Case ^{4/}		R_{qJC}	1.0	$^\circ\text{C/W}$

Notes:

1/ For ordering information, Price, Operating Curves, and Availability- Contact Factory.

2/ Screened to MIL-PRF-19500.

3/ Recovery Conditions: $I_F = 0.5 \text{ Amp}$, $I_R = 1.0 \text{ Amp}$, rec. to .25 Amp.

4/ Both Legs Tied Together.

NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: RH0053G

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查询"SDR623G"供应商

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SDR623G

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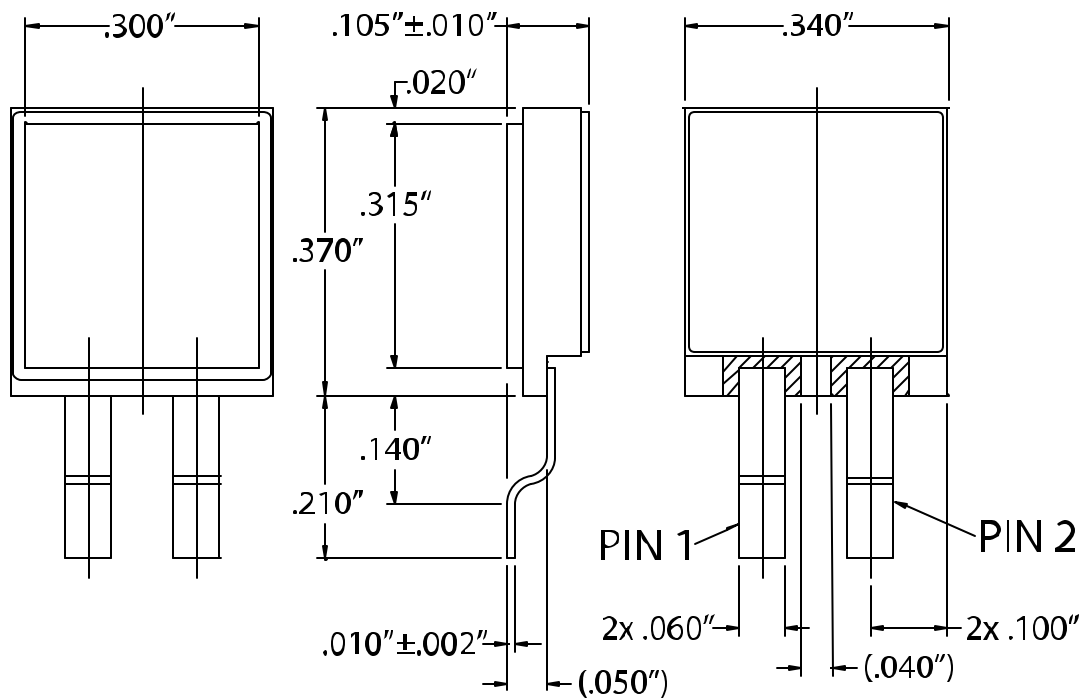
Electrical Characteristics ^{1/}		Symbol	Max	Units
Instantaneous Forward Voltage Drop (I _F = 10Adc, Pulse) (I _F = 20Adc, Pulse)	T _A = 25 °C	V _{F1}	1.40	V _{DC}
	T _A = 25 °C	V _{F2}	1.60	
Instantaneous Forward Voltage Drop (I _F = 20Adc, Pulse)	T _A = -55 °C	V _{F3}	1.70	V _{DC}
Reverse Leakage Current (100% of rated V _R , Pulse)	T _A = 25 °C	I _{R1}	50	mA
	T _A = 100 °C	I _{R2}	5	mA
Reverse Recovery Time (I _F = 0.5A, I _R = 1A, I _{RR} = 0.25A, T _A = 25°C)		t _{RR}	35	nsec
Junction Capacitance (V _R = 10V _{DC} , T _A = 25°C, f = 1MHz)		C _J	150	pF

Notes: ^{1/} Both Legs Tied Together.

PIN ASSIGNMENT			
PACKAGE	Pin 1	Pin 2	Pin 3 (Case)
CERPACK	Anode	Anode	Cathode

CERPACK

Outline:



Tolerances

Unless Specified- .XX ± .020"

.XXX ± .010"

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