LM4879 Boomer® Audio Power Amplifier Series
1.1 Watt Audio Power Amplifier

General Description

The LM4879 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4879 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for lower-power portable applications where minimal space and power consumption are primary requirements.

The LM4879 features a low-power consumption global shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the LM4879 features an internal thermal shutdown protection mechanism.

The LM4879 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4879 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- PSRR: 5V, 3V @ 217Hz — 62dB (typ)
- Power Output at 5V & 1% THD+N — 1.1W (typ)
- Power Output at 3V & 1% THD+N — 350mW (typ)
- Shutdown Current — 0.1µA (typ)

Features

- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity gain stable
- Ultra low current shutdown mode
- Fast turn on: 80ms (typ), 110ms (max) with 1.0µF capacitor
- BTL output can drive capacitive loads up to 100pF
- Advanced pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 2.2V - 5.0V operation
- Available in space-saving µSMD, LLP, and MSOP packages

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

Typical Application

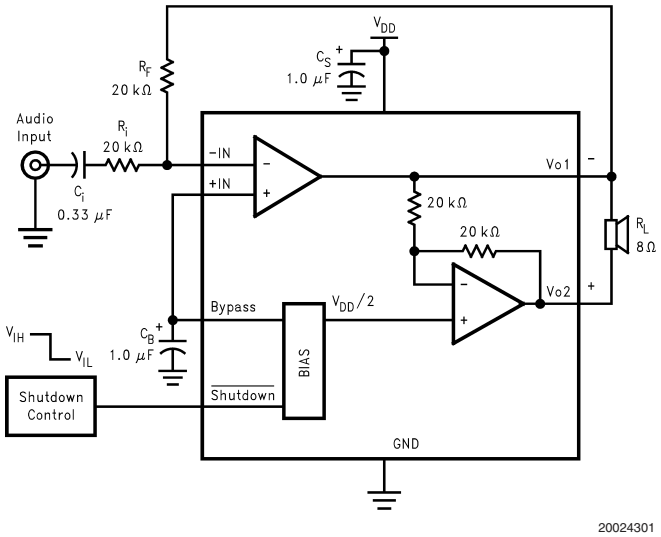

FIGURE 1. Typical Audio Amplifier Application Circuit

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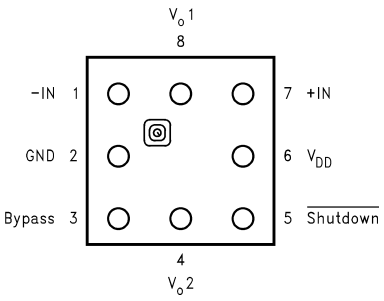
Connection Diagrams

8 Bump micro SMD



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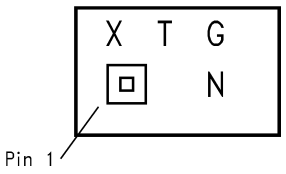
Top View
Order Number LM4879IBP, LM4879IBPX
See NS Package Number BPA08DDB

8 Bump micro SMD Marking



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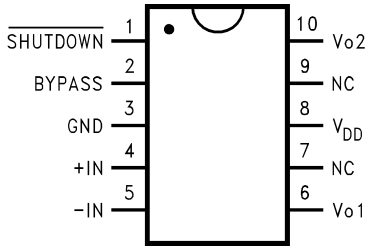
Top View
X - Date Code
T - Die Traceability
G - Boomer Family
N- LM4879IBP

Mini Small Outline (MSOP) Package



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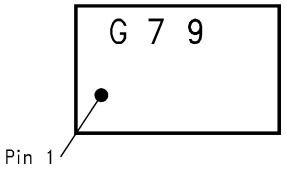
Top View
NC = No Connect
Order Number LM4879MM
See NS Package Number MUB10A

MSOP Marking



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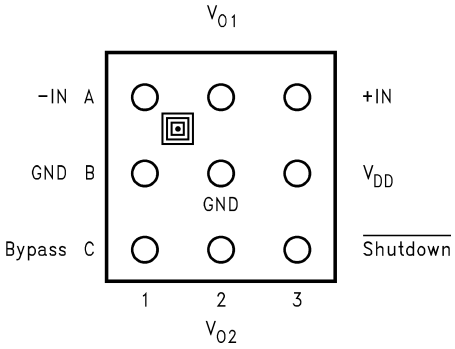
Top View
G - Boomer Family
79-LM4879MM

9 Bump micro SMD



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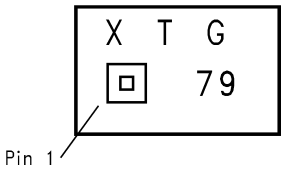
Top View
Order Number LM4879IBL, LM4879IBLX
See NS package Number BLA09AAB

9 Bump micro SMD Marking



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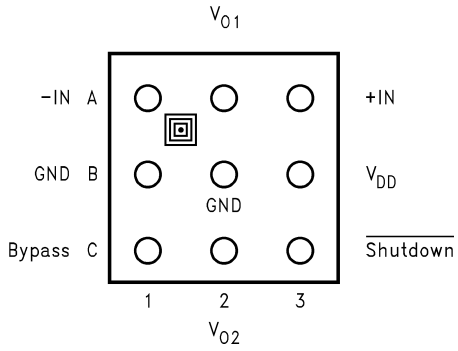
Top View
X - Date Code
T - Die Traceability
G - Boomer Family
79 - LM4879IBL

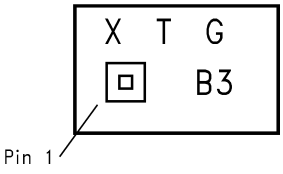
Connection Diagrams (Continued)

9 Bump micro SMD



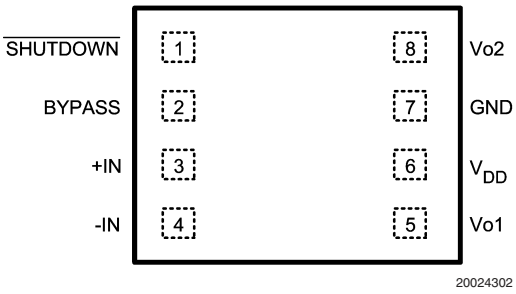
Top View
Order Number LM4879ITL, LM4879ITLX
See NS package Number TLA09AAA

9 Bump micro SMD Marking



Top View
X - Date Code
T - Die Traceability
G - Boomer Family
B3 - LM4879ITL

Leadless Leadframe Package (LLP)



Top View
Order Number LM4879SD
See NS Package Number SDC08A

LLP Marking

Top View
N - NS Logo
U - Fab Code
Z - Assembly Plant Code
XY - Date Code
TT - Die Traceability
L4879SD - LM4879SD

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 9)	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150˚C
Thermal Resistance	
θ_{JA} (BPA08DDB)	220˚C/W (Note 10)
θ_{JA} (SDC08A)	64˚C/W (Note 12)
θ_{JA} (TLA09AAA)	180˚C/W (Note 10)
θ_{JA} (BLA09AAB)	180˚C/W (Note 10)
θ_{JC} (MUB10A)	56˚C/W
θ_{JA} (MUB10A)	190˚C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40˚C \le T_A \le 85˚C$
Supply Voltage	$2.2V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4879		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, 8Ω BTL	5	10	mA (max)
I_{SD}	Shutdown Current	$V_{shutdown}$ = GND	0.1	2.0	µA (max)
V_{OS}	Output Offset Voltage		5	40	mV (max)
P_o	Output Power	THD+N = 1% (max); f = 1kHz	1.1	0.9	W (min)
THD+N	Total Harmonic Distortion+Noise	P_o = 0.4Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mVsine p-p, C_B = 1.0µF Input terminated with 10Ω to ground	68 (f = 1kHz) 62 (f = 217Hz)	55	dB (min)
V_{SDIH}	Shutdown High Input Voltage			1.4	V (min)
V_{SDIL}	Shutdown Low Input Voltage			0.4	V (max)
T_{WU}	Wake-up Time	C_B = 1.0µF	80	110	ms (max)
N_{OUT}	Output Noise	A-Weighted; Measured across 8Ω BTL Input terminated with 10Ω to ground	26		μV_{RMS}

Electrical Characteristics V_{DD} = 3.0V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4879		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, 8Ω BTL	4.5	9	mA (max)
I_{SD}	Shutdown Current	$V_{shutdown}$ = GND	0.1	2.0	µA (max)
V_{OS}	Output Offset Voltage		5	40	mV (max)
P_o	Output Power	THD+N = 1% (max); f = 1kHz	350	320	mW
THD+N	Total Harmonic Distortion+Noise	P_o = 0.15Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mVsine p-p, C_B = 1.0µF Input terminated with 10Ω to ground	68 (f = 1kHz) 62 (f = 217Hz)	55	dB (min)
V_{SDIH}	Shutdown High Input Voltage			1.4	V (min)
V_{SDIL}	Shutdown Low Input Voltage			0.4	V (max)
T_{WU}	Wake-up Time	C_B = 1.0µF	80	110	ms (max)

Electrical Characteristics V_{DD} = 3.0V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25˚C. (Continued)

Symbol	Parameter	Conditions	LM4879		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 8)	
N_{OUT}	Output Noise	A-Weighted; Measured across 8Ω BTL Input terminated with 10Ω to ground	26		μV_{RMS}

Electrical Characteristics V_{DD} = 2.6V (Notes 1, 2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4879		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, 8Ω BTL	3.5		mA
I_{SD}	Shutdown Current	$V_{shutdown}$ = GND	0.1		µA
V_{OS}	Output Offset Voltage		5		mV
P_o	Output Power	THD+N = 1% (max); f = 1kHz			
		R_L = 8Ω	250		mW
		R_L = 4Ω	350		
THD+N	Total Harmonic Distortion+Noise	P_o = 0.1Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mVsine p-p, C_B = 1.0µF Input terminated with 10Ω to ground	55 (f = 1kHz) 55 (f = 217Hz)		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4879, see power derating curves for additional information.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF–240pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: For micro SMD only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.

Note 9: If the product is in shutdown mode, and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10ma, then the part will be protected. If the part is enabled when V_{DD} is above 6V, circuit performance will be curtailed or the part may be permanently damaged.

Note 10: All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance.

Note 11: Maximum power dissipation (P_{DMAX}) in the device occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 1 shown in the Application section. It may also be obtained from the power dissipation graphs.

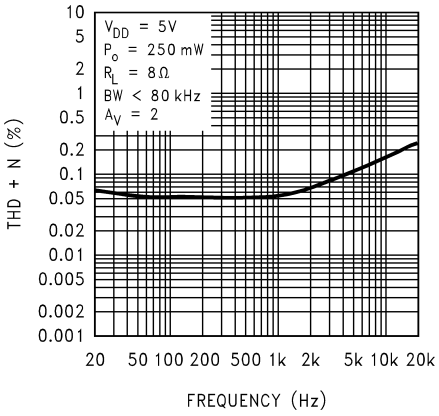
Note 12: The stated θ_{JA} is achieved when the LLP package's DAP is soldered to a $4in^2$ copper heatsink plain.

External Components Description

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, **Proper Selection of External Components**, for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Power Supply Bypassing** section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, **Proper Selection of External Components**, for information concerning proper placement and selection of C_B.

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, PWR = 250mW



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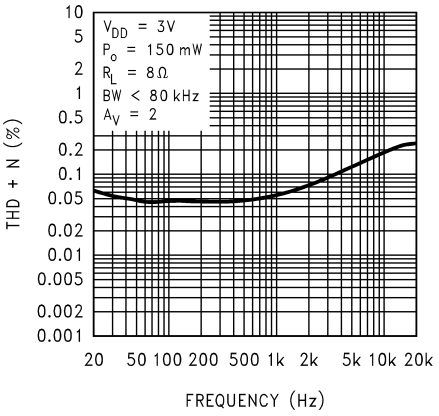
THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, PWR = 150mW



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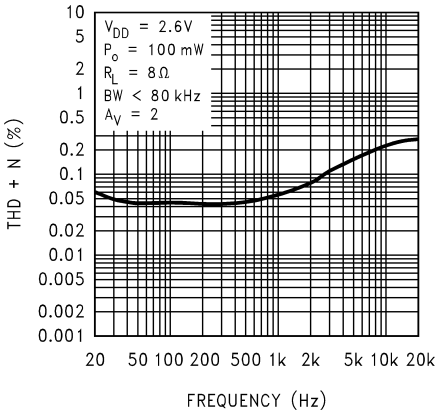
THD+N vs Frequency
V_{DD} = 2.6V, R_L = 8Ω, PWR = 100mW



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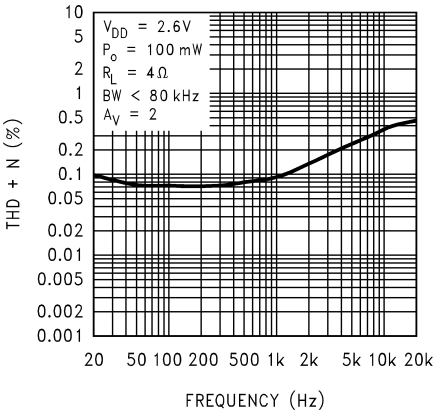
THD+N vs Frequency
V_{DD} = 2.6V, R_L = 4Ω, PWR = 100mW



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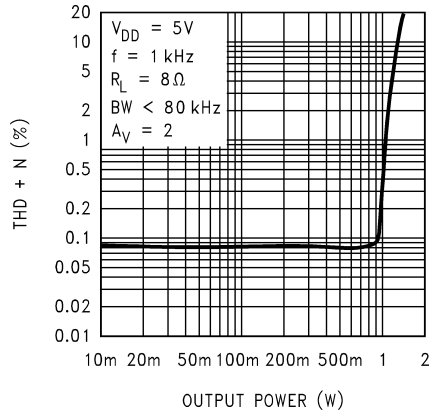
THD+N vs Power Out
V_{DD} = 5V, R_L = 8Ω, f = 1kHz



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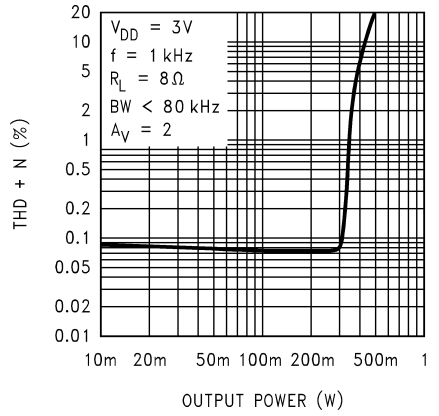
THD+N vs Power Out
V_{DD} = 3V, R_L = 8Ω, f = 1kHz



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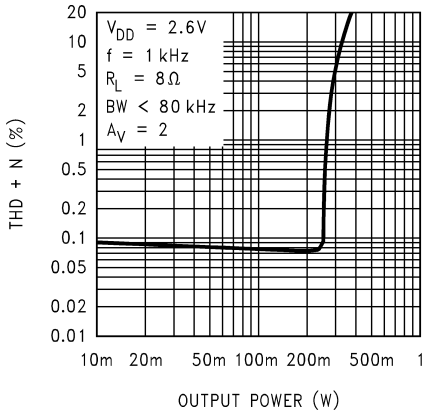
Typical Performance Characteristics (Continued)

THD+N vs Power Out
V_{DD} = 2.6V, R_L = 8Ω, f = 1kHz



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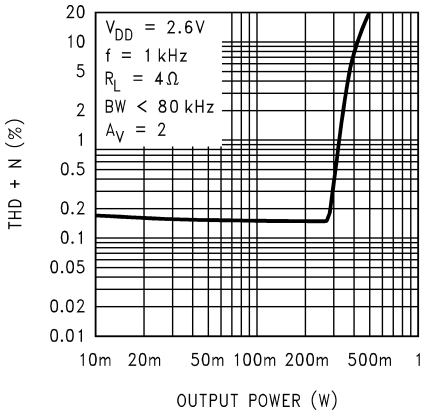
THD+N vs Power Out
V_{DD} = 2.6V, R_L = 4Ω, f = 1kHz



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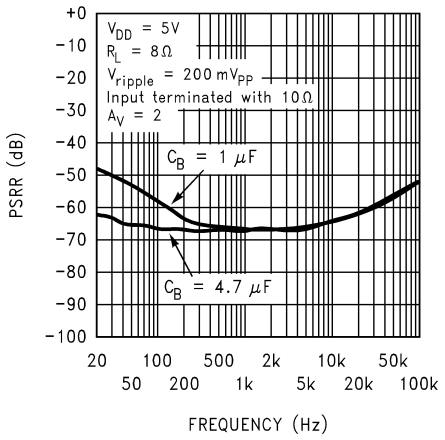
Power Supply Rejection Ratio
V_{DD} = 5V



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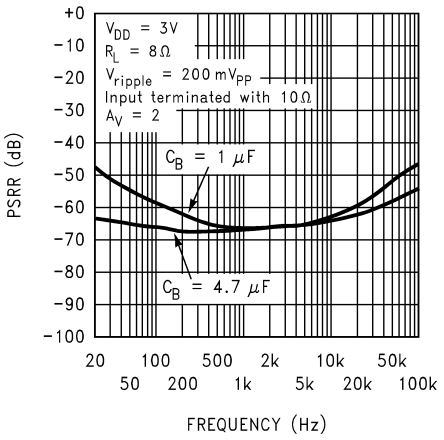
Power Supply Rejection Ratio
V_{DD} = 3V



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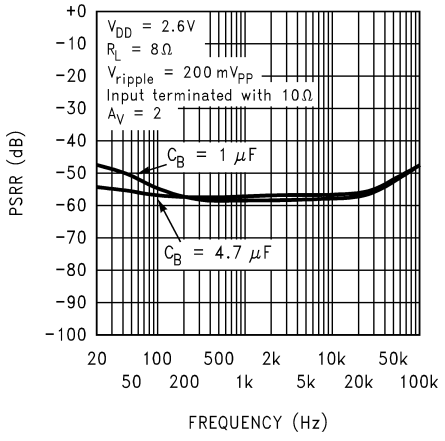
Power Supply Rejection Ratio
V_{DD} = 2.6V



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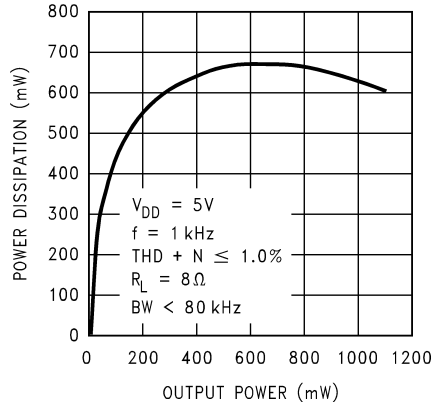
Power Dissipation vs Output Power
V_{DD} = 5V



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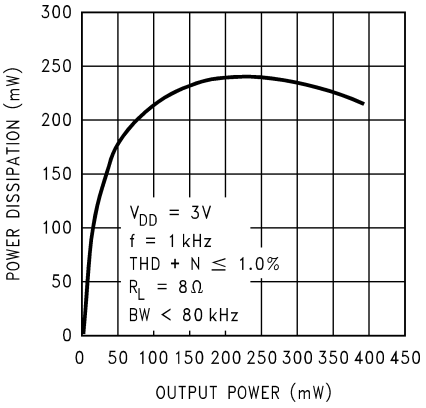
Typical Performance Characteristics (Continued)

Power Dissipation vs Output Power V_{DD} = 3V



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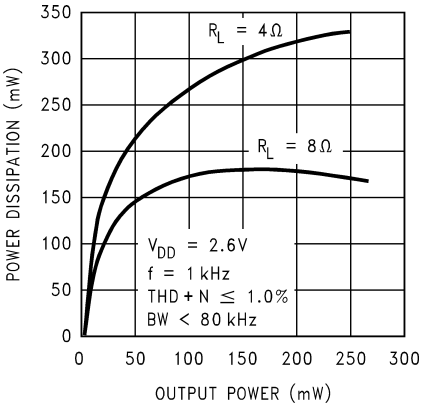
Power Dissipation vs Output Power V_{DD} = 2.6V



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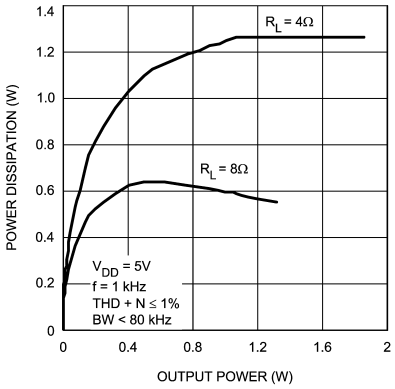
Power Dissipation vs Output Power (LLP Package) V_{DD} = 5V



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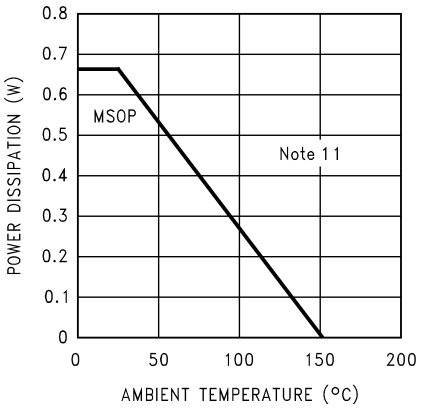
Power Derating - MSOP P_{DMAX} = 670mW V_{DD} = 5V, R_L = 8Ω



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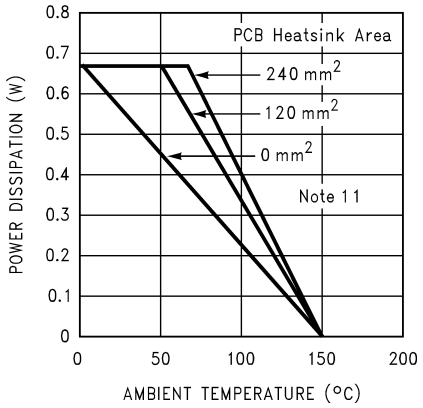
Power Derating - 8 Bump µSMD P_{DMAX} = 670mW V_{DD} = 5V, R_L = 8Ω



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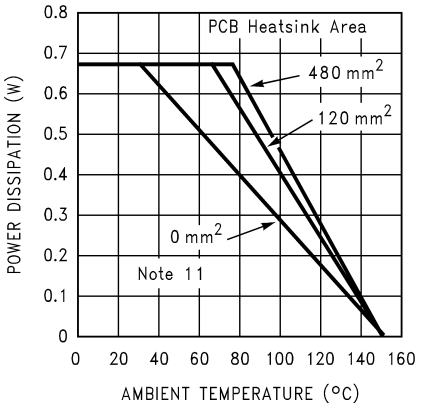
Power Derating - 9 Bump µSMD P_{DMAX} = 670mW V_{DD} = 5V, R_L = 8Ω



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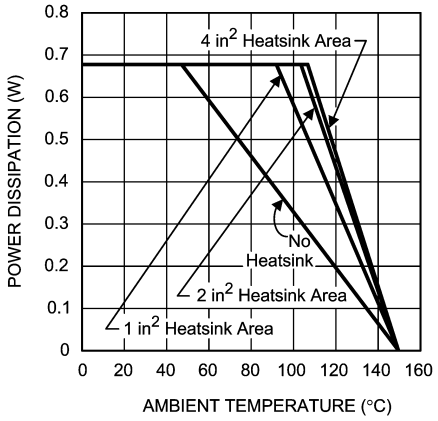
Typical Performance Characteristics (Continued)

Power Derating - LLP
P_{DMAX} = 670mV
V_{DD} = 5V, R_L = 8



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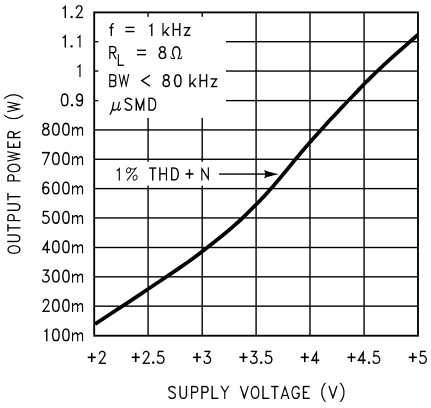
Output Power vs Supply Voltage



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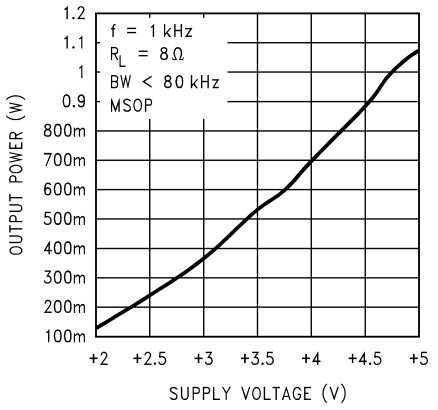
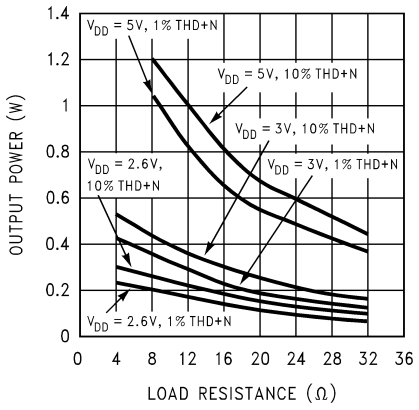
Output Power vs Supply Voltage



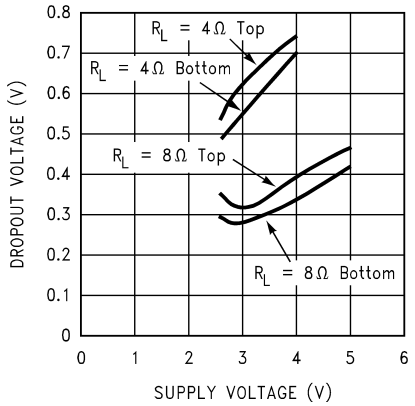
20024350

Output Power vs Load Resistance



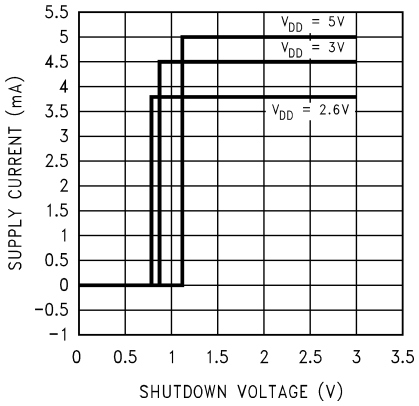
20024374

Clipping (Dropout) Voltage vs Supply Voltage



20024352

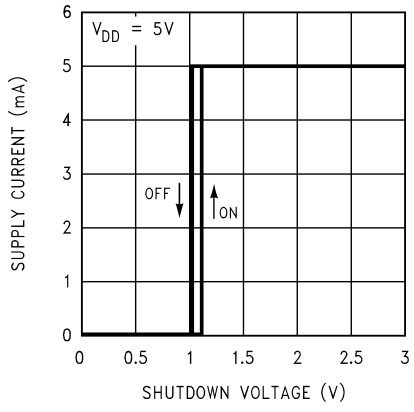
Supply Current Shutdown Voltage



20024375

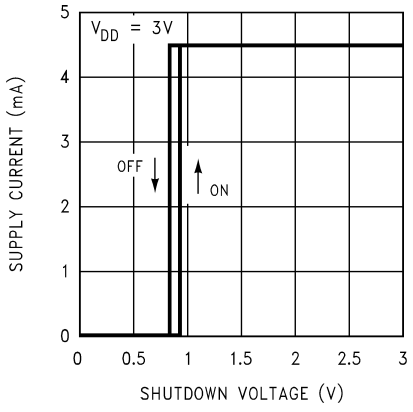
Typical Performance Characteristics (Continued)

Shutdown Hysterisis Voltage
V_{DD} = 5V



20024376

Shutdown Hysterisis Voltage
V_{DD} = 3V



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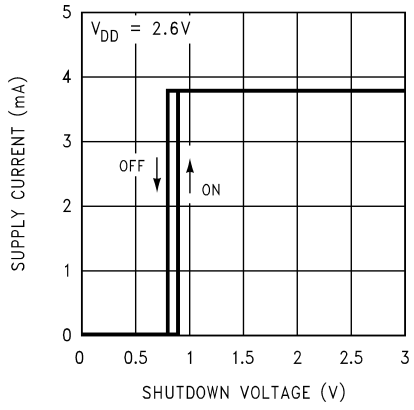
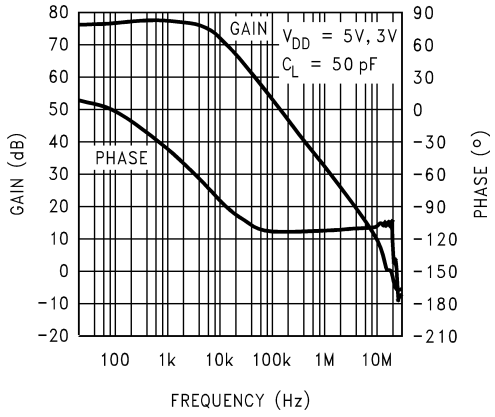
Shutdown Hysterisis Voltage
V_{DD} = 2.6V



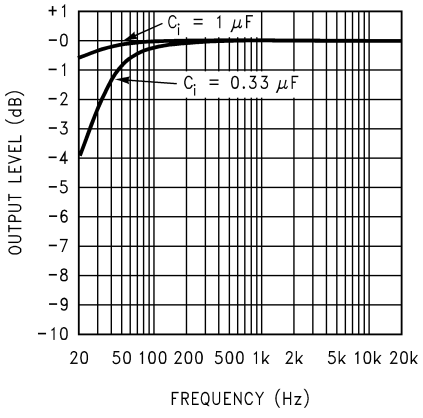
20024378

Open Loop
Frequency Response



20024354

Frequency Response
vs Input Capacitor Size



20024356

Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4879 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 20 kΩ resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180˚. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f/R_i)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in LM4879, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4879 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

It is critical that the maximum junction temperature (T_{JMAX}) of 150˚C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced from a free air value of 150˚C/W, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the LM4879. It is especially effective when connected to V_{DD}, GND, and the output pins. Refer to the application information on the LM4879 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150˚C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4879. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4879 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin. By switching the shutdown pin to ground, the LM4879 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than $0.4V_{DC}$, the idle current may be greater than the typical value of 0.1µA. (Idle current is measured with the shutdown pin tied to ground).

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground which disables the amplifier. If the switch is open, then the external pull-up resistor to V_{DD} will enable the LM4879. This scheme guarantees that the shutdown pin will not float thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4879 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4879 is unity-gain stable which gives the designer maximum system flexibility. The LM4879 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 1*. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Application Information (Continued)

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100 Hz to 150 Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the LM4879 turns on. The slower the LM4879's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0 µF along with a small value of C_i (in the range of 0.1 µF to 0.39 µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1 µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0 µF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{opeak} using Equation 2 and add the output voltage. Using this method, the minimum supply voltage would be $(V_{opeak} + (V_{OD_{TOP}} + V_{OD_{BOT}}))$, where $V_{OD_{BOT}}$ and $V_{OD_{TOP}}$ are extrapolated from the Dropout Voltage vs Supply Voltage curve in the **Typical Performance Characteristics** section.

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (2)$$

5V is a standard voltage, in most applications, chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4879 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 3.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (3)$$

$$A_{VD} = (R_f/R_i)\ 2$$

From Equation 3, the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance was 20 kΩ, and with a A_{VD} of 3, a ratio of 1.5:1 of R_f to R_i results in an allocation of R_i = 20 kΩ and R_f = 30 kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of –3 dB frequency points. Five times away from a –3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified.

f_L = 100 Hz/5 = 20 Hz

f_H = 20 kHz * 5 = 100 kHz

As stated in the **External Components** section, R_i in conjunction with C_i create a highpass filter.

$C_i \geq 1/(2\pi * 20\ k\Omega * 20\ Hz) = 0.397\ \mu F$; use 0.39 µF

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100 kHz, the resulting GBWP = 300 kHz which is much smaller than the LM4879 GBWP of 10 MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4879 can still be used without running into bandwidth limitations.

Application Information (Continued)

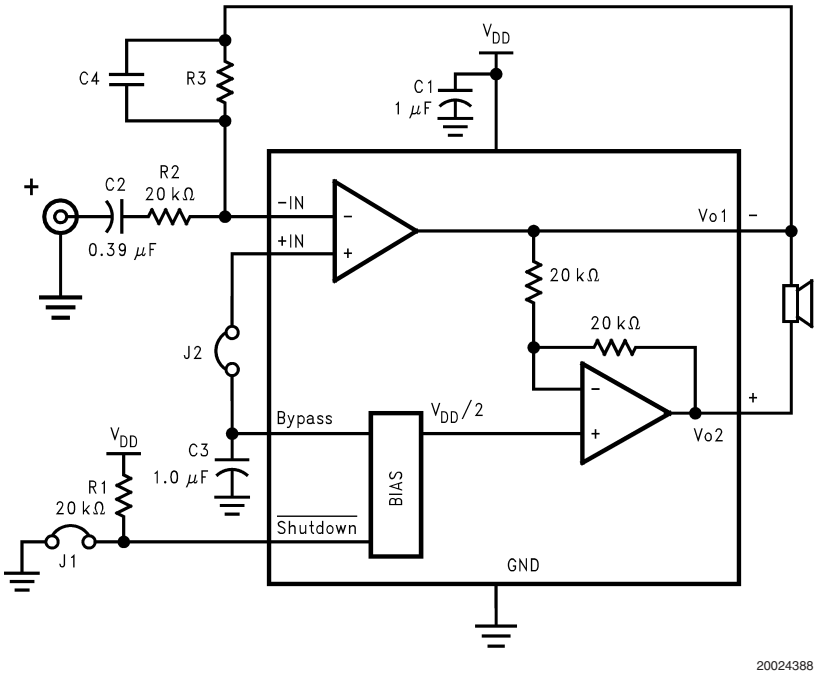


FIGURE 2. HIGHER GAIN AUDIO AMPLIFIER

The LM4879 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C4) may be needed as shown in Figure 2 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C_4 = 25pf. These components result in a -3dB point of approximately 320 kHz.

Application Information (Continued)

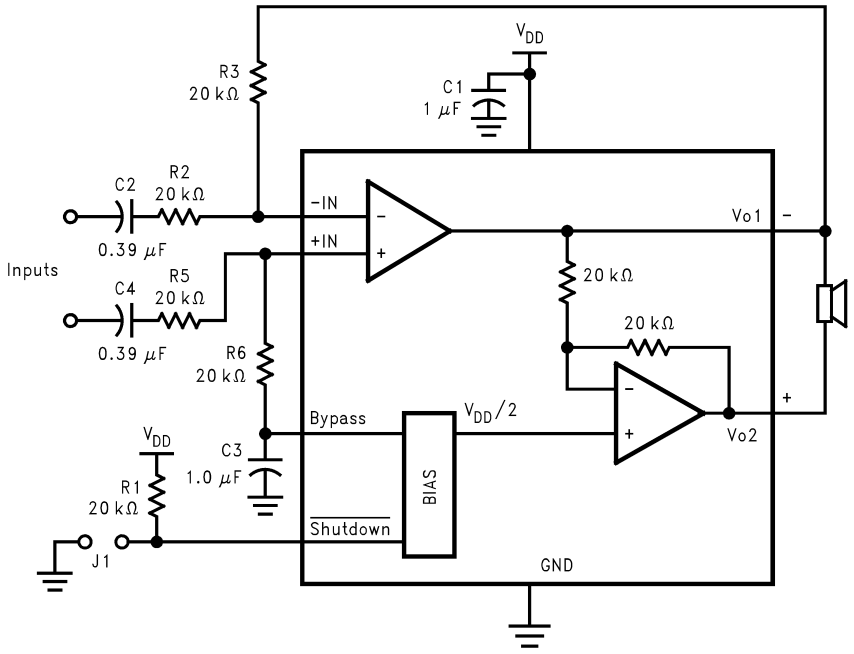


FIGURE 3. DIFFERENTIAL AMPLIFIER CONFIGURATION FOR LM4879

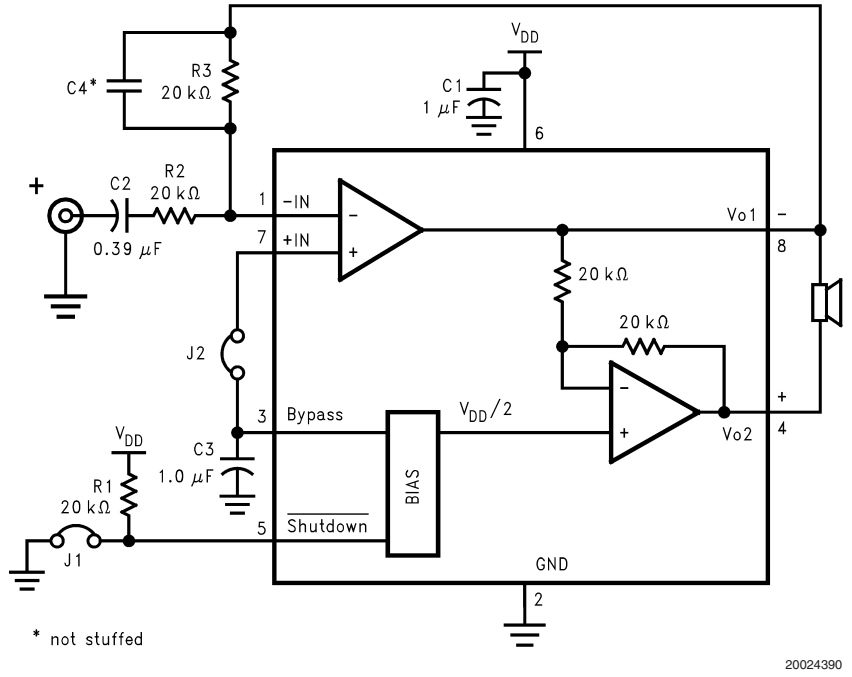


FIGURE 4. REFERENCE DESIGN BOARD and LAYOUT - micro SMD

Application Information (Continued)

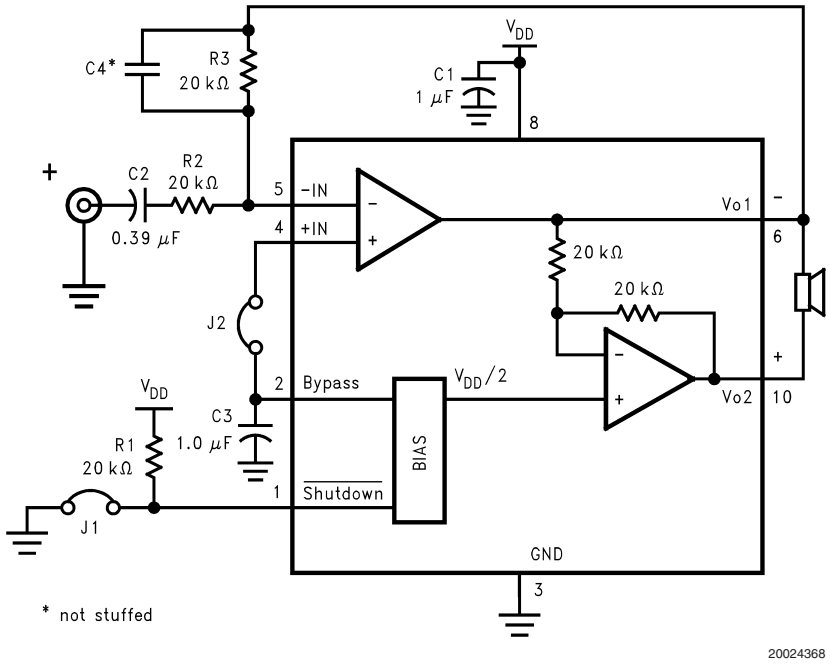
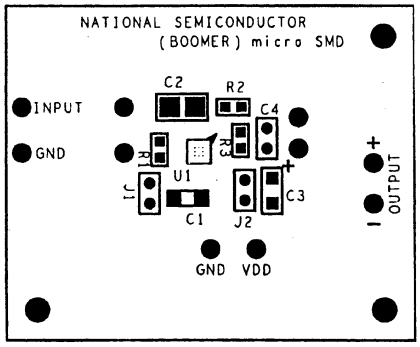


FIGURE 5. REFERENCE DESIGN BOARD and PCB LAYOUT GUIDELINES - MSOP & SO Boards

Application Information (Continued)

LM4879 micro SMD BOARD ARTWORK

Silk Screen



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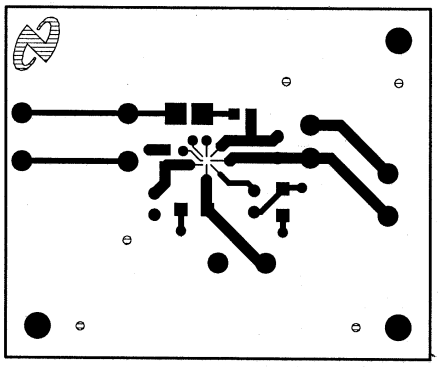
Top Layer



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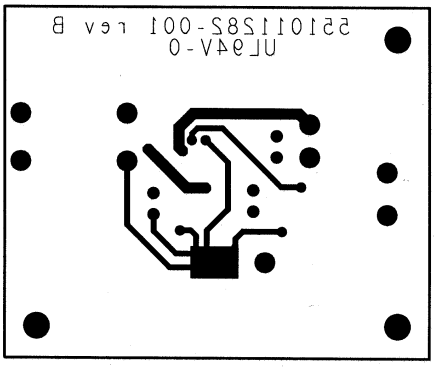
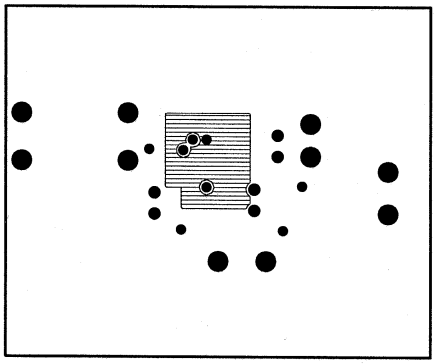
Bottom Layer



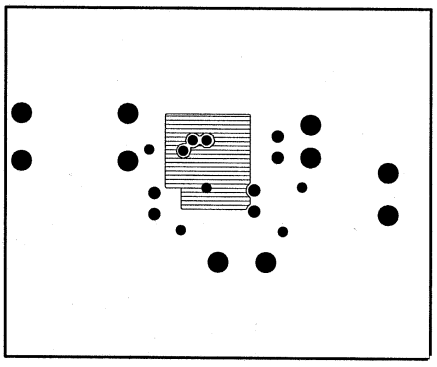
20024359

Inner Layer Ground



20024360

Inner Layer V_{DD}



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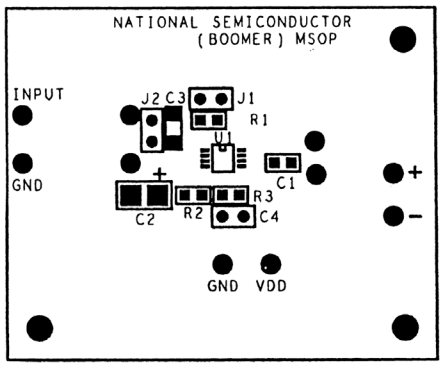
Application Information (Continued)

LM4879 MSOP DEMO BOARD ARTWORK

Silk Screen



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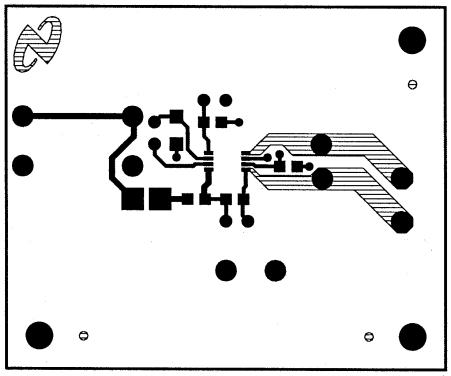

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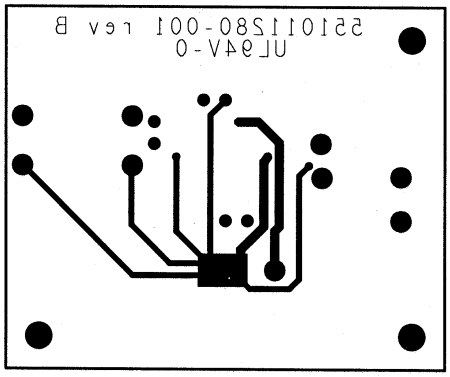
Bottom Layer



20024367

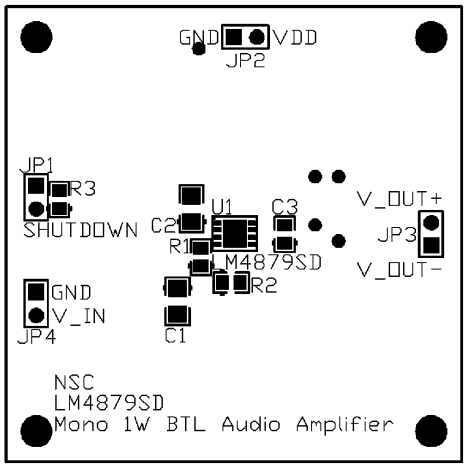
TABLE 1. Mono LM4879 Reference Design Boards Bill of Material for all 3 Demo Boards

Item	Part Number	Part Description	Qty	Ref Designator
1	551011208-001	LM4879 Mono Reference Design Board	1	
10	482911183-001	LM4879 Audio AMP	1	U1
20	151911207-001	Tant Cap 1uF 16V 10	1	C1
21	151911207-002	Cer Cap 0.39uF 50V Z5U 20% 1210	1	C2
25	152911207-001	Tant Cap 1.0uF 16V 10	1	C3
30	472911207-001	Res 20K Ohm 1/10W 5	3	R1, R2, R3
35	210007039-002	Jumper Header Vertical Mount 2X1 0.100	2	J1, J2

Application Information (Continued)

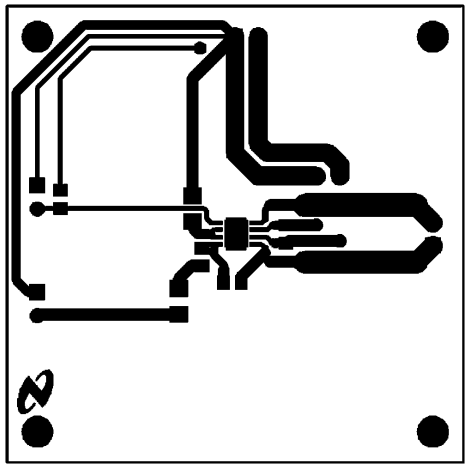
LM4879 LLP DEMO BOARD ARTWORK

Silk Screen



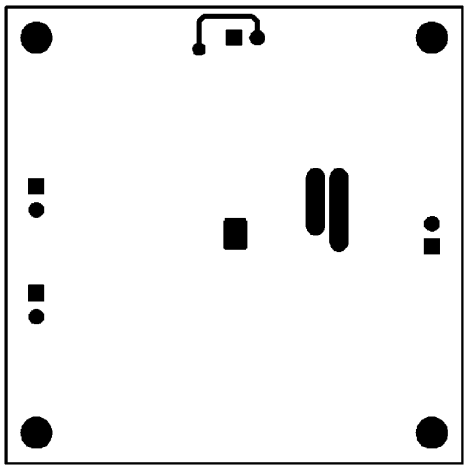
200243C2

Top Layer



200243C0

Bottom Layer



200243C1

Application Information (Continued)

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

General Mixed Signal Layout Recommendation

Power and Ground Circuits

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will take require a greater amount of design time but will not increase the final price of the board. The only extra parts required may be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

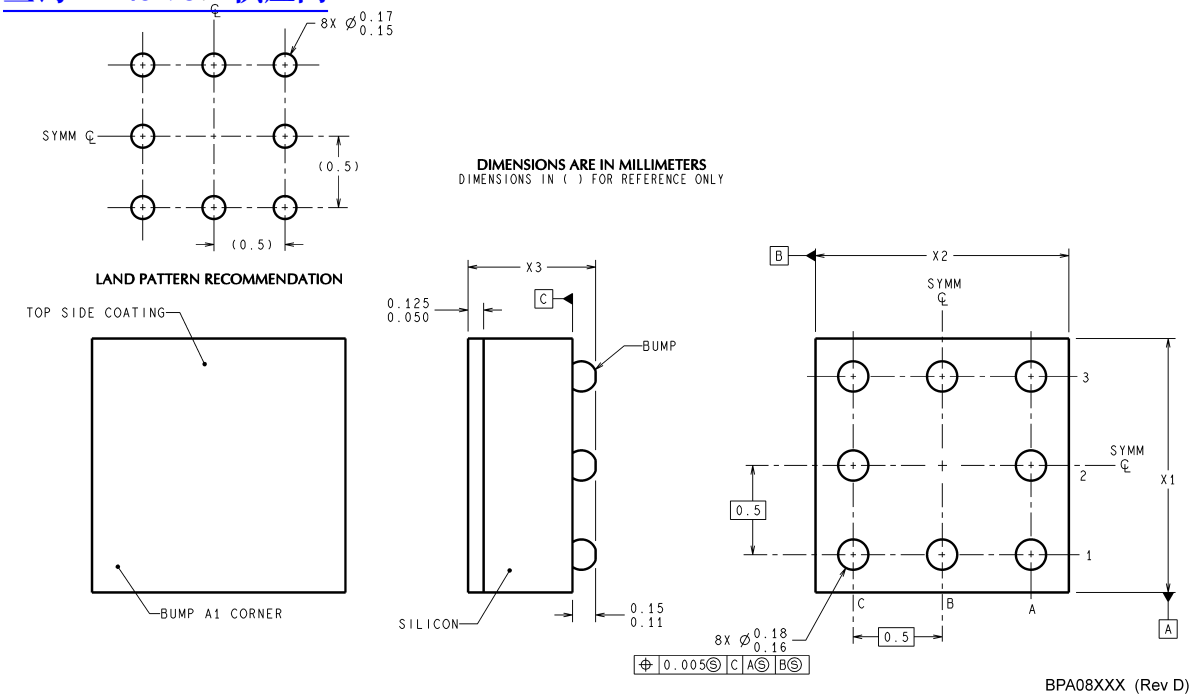
Placement of Digital and Analog Components

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Physical Dimensions inches (millimeters) unless otherwise noted



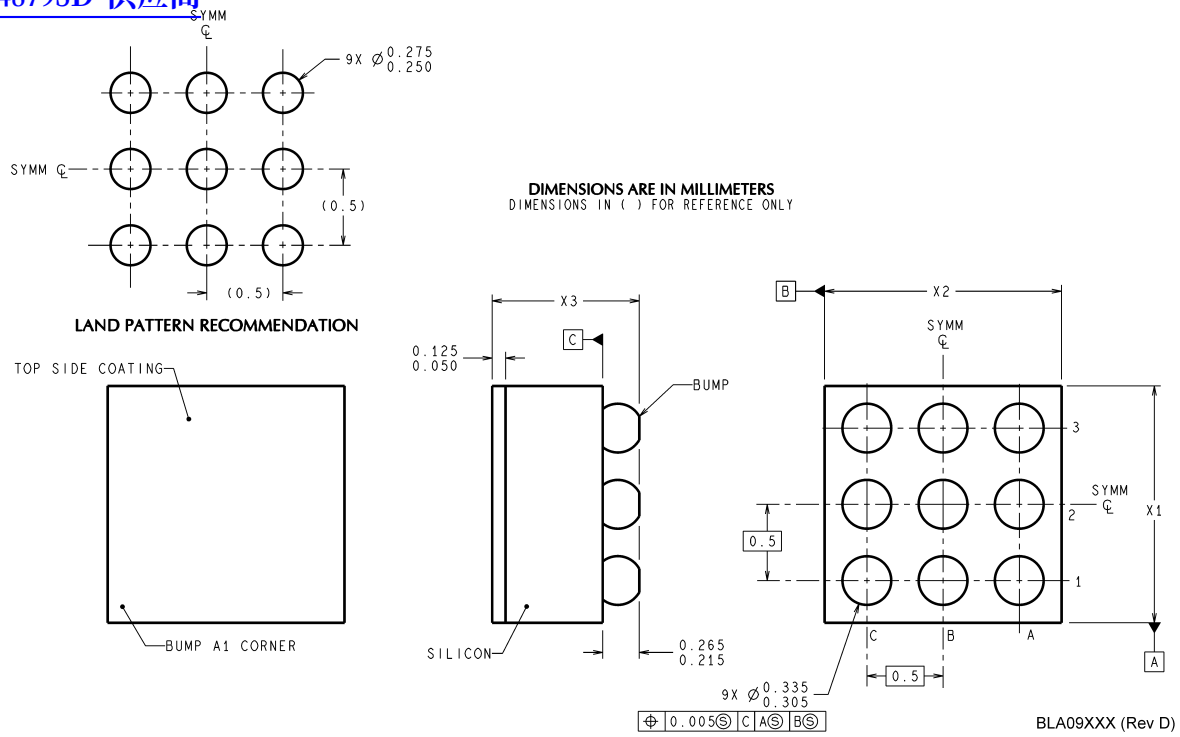
BPA08XXX (Rev D)

Note: Unless otherwise specified.

1. Epoxy coating.
2. 63Sn/37Pb eutectic bump.
3. Recommend non-solder mask defined landing pad.
4. Pin 1 is established by lower left corner with respect to text orientation pins are numbered counterclockwise.
5. Reference JEDEC registration MO-211, variation BC.

8-Bump micro SMD
Order Number LM4879IBP, LM4879IBPX
NS Package Number BPA08DDB
X1 = 1.361±0.03 X2 = 1.361±0.03 X3 = 0.850±0.10

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

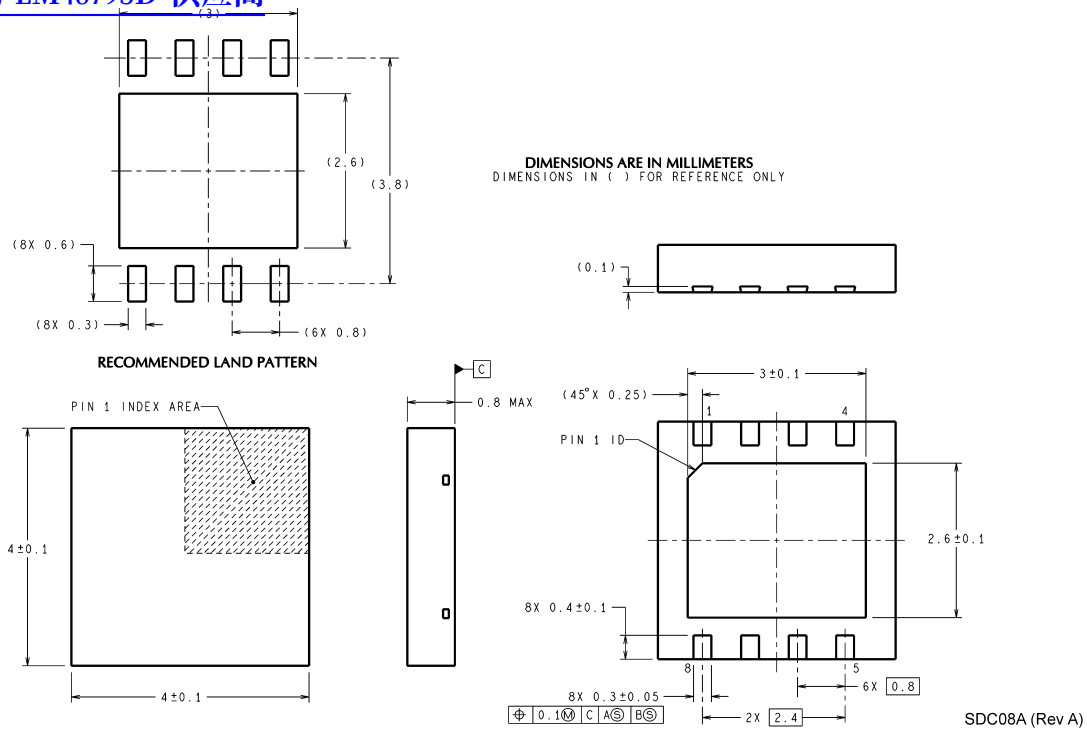


Note: Unless otherwise specified.

1. Epoxy coating.
2. 63Sn/37Pb eutectic bump.
3. Recommend non-solder mask defined landing pad.
4. Pin 1 is established by lower left corner with respect to text orientation pins are numbered counterclockwise.
5. Reference JEDEC registration MO-211, variation BC.

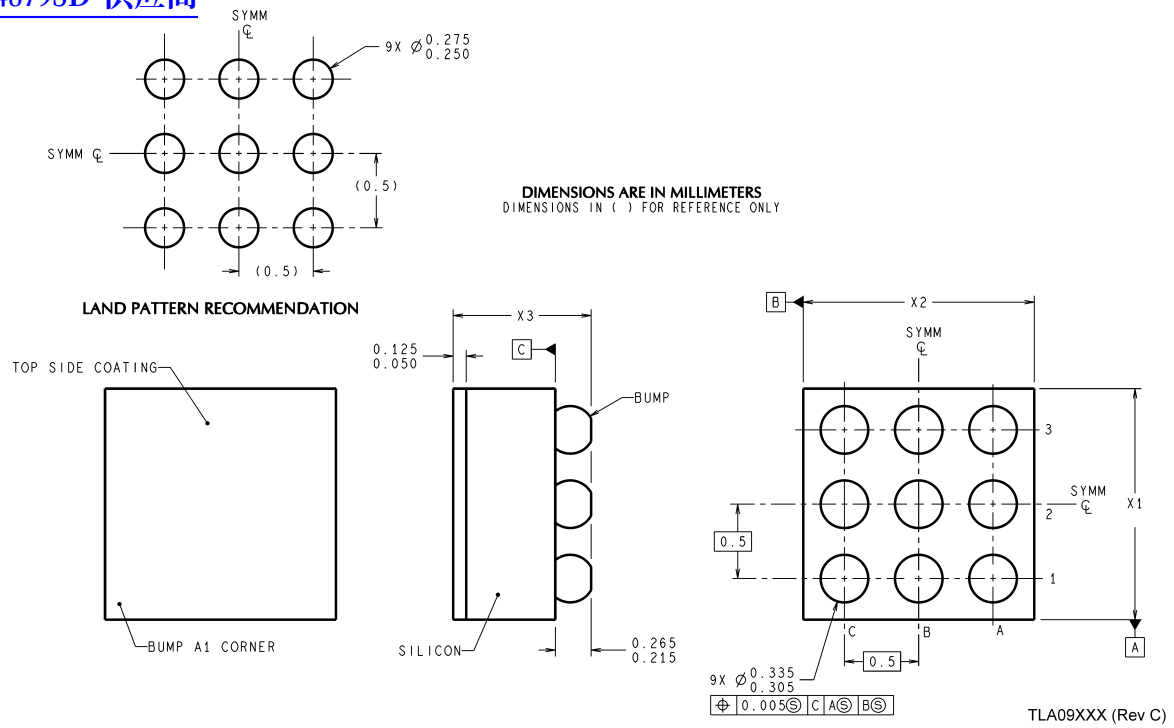
9-Bump micro SMD
Order Number LM4879IBL, LM4879IBLX
NS Package Number BLA09AAB
X1 = 1.514±0.03 X2 = 1.514±0.03 X3 = 0.945±0.10

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

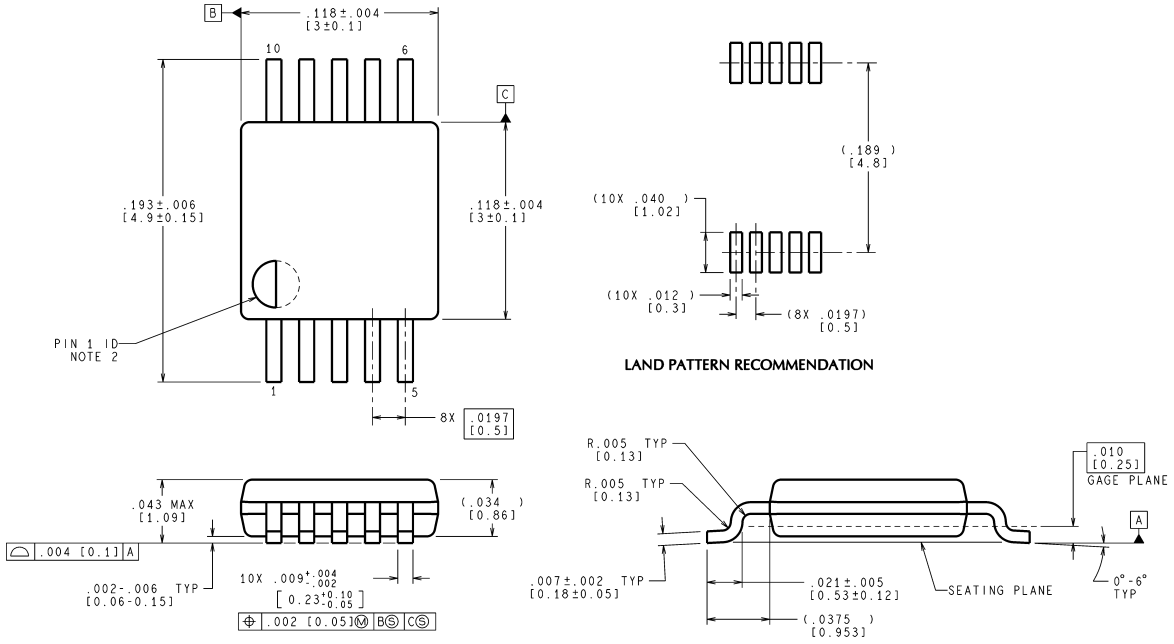


LLP
Order Number LM4879SD
NS Package Number SDC08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



9-Bump micro SMD
Order Number LM4879ITL LM4879ITLX
NS Package Number TLA09AAA
X1 = 1.514±0.03 X2 = 1.514±0.03 X3 = 0.60±0.075



MSOP
Order Number LM4879MM
NS Package Number MUB10A

Notes