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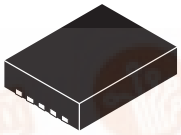

Li-Ion AND Li-Pol BATTERY GAS GAUGE IC FOR PORTABLE APPLICATIONS (bqJUNIOR)

FEATURES

- HDQ (bq27010) or I^{2}C (bq27210) Communication
- Reports Accurate *Time-to-Empty* At Both Measured and Host-Requested Load Values
- Reports Available Capacity Compensated for Discharge Rate, Temperature, and Age
- End-of-Discharge Voltage Compensated for Discharge Rate and Temperature
- Automatic Capacity Reduction with Age
- Reports Temperature, Voltage, and Current
- High Accuracy Charge and Discharge Current Integration with Automatic Offset Calibration
- Requires No User Calibration
- Programmable Input/Output Port
- Internal User EEPROM Configuration Memory
- Uploadable Coefficients Allows Host-Side Use with Multiple Pack Characteristics
- Stable Oscillator Without External Components
- Dynamic End-of-Discharge Detection Delay to Allow Use in a High-Dynamic Load Environment
- Automatic Sleep Mode When Communication Lines are Low
- Available in a Small 3 mm x 4 mm QFN Package
- Five Low-Power Operating Modes
  - Active: < 90 µA
  - Sleep: < 2.5 µA
  - Ship: < 2 µA (bq27010 only)
  - Hibernate: < 1.5 µA
  - Data Retention: < 20 nA

APPLICATIONS

- PDA
- Smart Phones
- MP3 Players
- Digital Cameras
- Internet Appliances
- Handheld Devices

DESCRIPTION

The bqJUNIOR™ series are highly accurate stand-alone single-cell Li-Ion and Li-Pol battery capacity monitoring and reporting devices targeted at space-limited, portable applications. The IC monitors a voltage drop across a small current sense resistor connected in series with the battery to determine charge and discharge activity of the battery. Compensations for battery age, temperature, self-discharge, and discharge rate are applied to the capacity measurments to provide available time-to-empty information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or learned, in the course of a discharge cycle from full to empty. Internal registers include current, capacity, time-to-empty, state-of-charge, cell temperature and voltage, status, and more.

The bqJUNIOR can operate directly from single-cell Li-Ion and Li-Pol batteries and communicates to the system over a HDQ one-wire or I^{2}C serial interface.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

bqJUNIOR is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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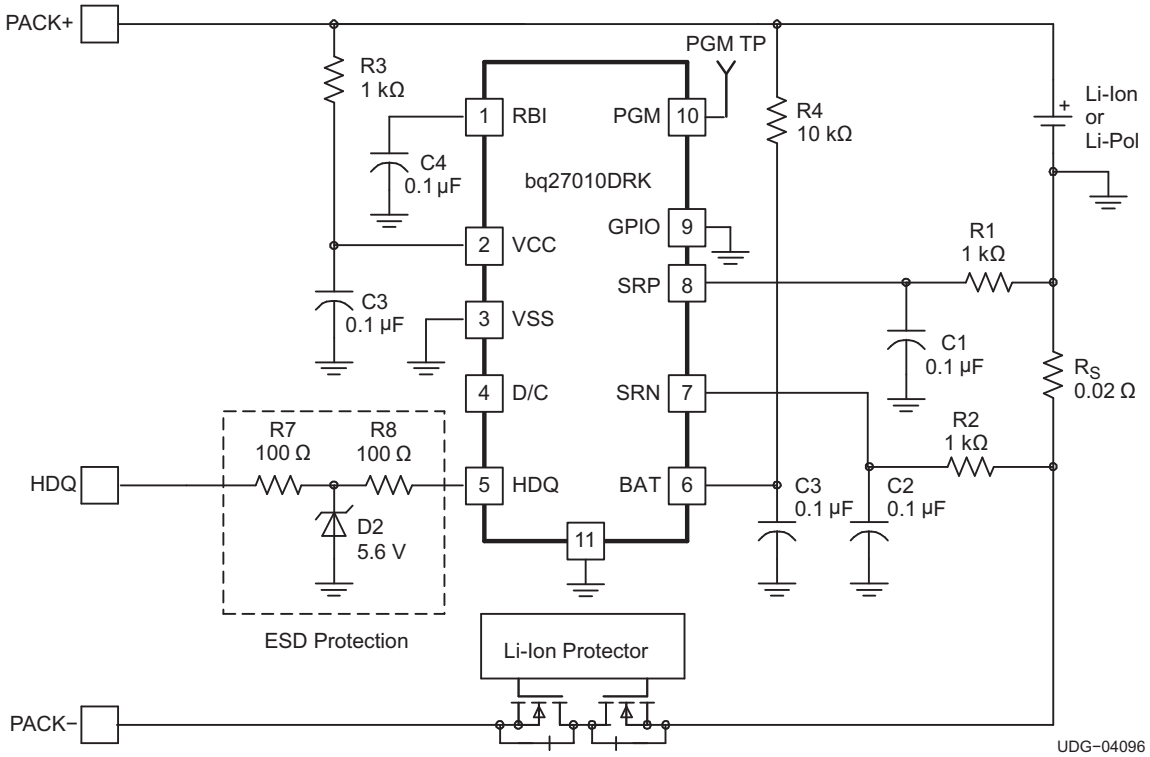
TYPICAL APPLICATION



ORDERING INFORMATION

TA	COMMUNICATION INTERFACE	PACKAGED DEVICES(1)	MARKINGS
-20°C to 70°C	HDQ	bq27010DRKR	27010
	I^2C	bq27210DRKR	27210

(1) The DRK package is available taped and reeled only. Quantities are 2,000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			bq27010 bq27210	UNITS
V_{CC}	Supply voltage	(with respect to V_{SS})	–0.3 to 7	V
V_{IN}	Input voltage	SRP, SRN, RBI, BAT (all with respect to V_{SS})	–0.3 to V_{CC}+0.3	
		HDQ, SCL, SDA, GPIO (all with respect to V_{SS})	–0.3 to 7	
		PGM (with respect to V_{SS}) during EEPROM programming	–0.3 to 22	
I_{SINK}	Output sink current	GPIO, SCL, SDA, HDQ	5	mA
T_A	Operating free-air temperature range		–20 to 70	°C
T_{stg}	Storage temperature range		–65 to 150	
T_J	Operating junction temperature range		–40 to 125	
	Lead temperature (soldering, 10 sec)		300	

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RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.6	4.5	V
T_A	Operating free-air temperature	–20	70	°C
	Input voltage, SRP and SRN with respect to V_{SS}	–100	100	mV

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
$I_{CC(VCC)}$	Active current	$V_{BAT} = V_{CC}$		52	90	µA
$I_{CC(SLP)}$	Sleep current			1.0	2.5	
$I_{CC(SHP)}$	Ship current (bq27010 only)			0.9	2.0	
$I_{CC(POR)}$	Hibernate current	$0 < V_{CC} < 1.5$ V		0.6	1.5	
	RBI current	RBI pin only, $V_{CC} < V_{CC(POR)}$		< 1	20	nA
$V_{(POR)}$	POR threshold		2.0		2.6	V
	Input impedance	BAT, SRN, SRP	10			MΩ
	Pull-down current	HDQ, SCL, SDA		2.7	4.5	µA
HDQ, SCL, SDA and GPIO						
V_{IH}	High-level input voltage	$V_{CC} < 4.2$ V	1.5			V
		$V_{CC} > 4.2$ V	1.7			
V_{IL}	Low-level input voltage				0.7	
V_{OL}	Low-level output voltage (GPIO)	$I_{OL} = 1$ mA			0.4	
	Low-level output voltage (HDQ, SCL, SDA)	$I_{OL} = 2$ mA			0.4	
VOLTAGE AND TEMPERATURE MEASUREMENT						
	Measurement range	$V_{CC} = V_{(BAT)}$	2.6		4.5	V
	Reported voltage resolution			2.7		mV
	Reported accuacy		-25		25	
	Voltage update time			2.56		s
	Reported temperature resolution			0.25		°K
	Reported temperature accuracy		-3		3	
	Temperature update time			2.56		s
TIME, CURRENT AND CAPACITY (3.0 V ≤ V_{CC} ≤ 4.2 V, 0°C ≤ T_A ≤ 50°C)						
f_{OSC}	Internal oscillator frequency		-2.2%		1.5%	
	Current gain variability		-0.5%		0.5%	
	Coulometric gain variability		-1.7%		0.5%	
	Coulomb counter input offset(1)		-15	0	15	µV
	V_{SRP}-V_{SRN} differential input		–100		100	mV
EEPROM PROGRAMMING (V_{CC} ≥ 3.0 V, -20°C ≤ T_A ≤ 35°C)(2)						
	Programming voltage rise time		0.5		1.5	ms
	Programming voltage high time		10		100	ms
	Programming voltage fall time		0.5		1.5	ms
	Programming voltage	Applied to PGM pin	20		22	V
	EEPROM programming current	$V_{PROGRAM} = 21$ V			15	mA

(1) Excludes contributions to the offset due to PCB layout or other factors external to the bq27010/bq27210.
(2) Maximum number of programming cycles on the EEPROM is 10 and data retention time is 10 years at $T_A = 85$°C.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STANDARD HDQ SERIAL COMMUNICATION TIMING (bq27010 only)						
$t_{(B)}$	Break timing		190			µs
$t_{(BR)}$	Break recovery		40			
$t_{(CYCH)}$	Host bit window		190			
$t_{(HW1)}$	Host sends 1		0.5		50	
$t_{(HW0)}$	Host sends 0		86		145	
$t_{(RSPS)}$	bqJUNIOR to host response		190		320	
$t_{(CYCD)}$	bqJUNIOR bit window		190		250	
$t_{(DW1)}$	bqJUNIOR sends 1		32		50	
$t_{(DW0)}$	bqJUNIOR sends 0		80		145	
STANDARD I^2C SERIAL COMMUNICATION TIMING (bq27210 only - Product Preview Data)						
t_r	SCL/SDA rise time				1	µs
t_f	SCL/SDA fall time				300	ns
$t_{w(H)}$	SCL pulse width (high)		4			µs
$t_{w(L)}$	SCL pulse width (low)		4.7			
$t_{su(STA)}$	Setup for repeated start		4.7			
$t_{d(STA)}$	Start to first falling edge of SCL		4			
$t_{su(DAT)}$	Data setup time		250			ns
$t_{h(DAT)}$	Data hold time		300			
$t_{su(STOP)}$	Setup time for stop		4			µs
$t_{(BUF)}$	Bus free time between stop and start		4.7			
$f_{(SCL)}$	Clock frequency				100	kHz
$t_{(BUSERR)}$	Bus error timeout		17.3		21.2	s

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TIMING DIAGRAMS

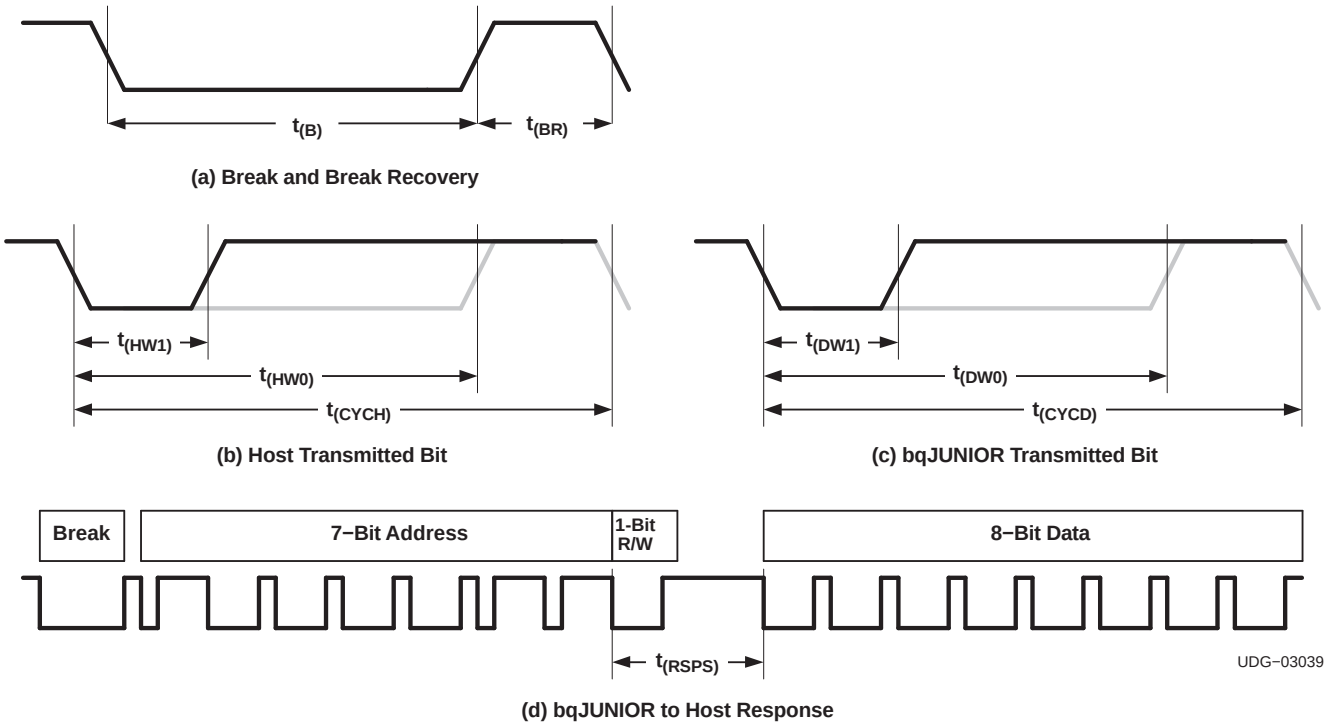

Figure 1. HDQ Bit Timing Diagram

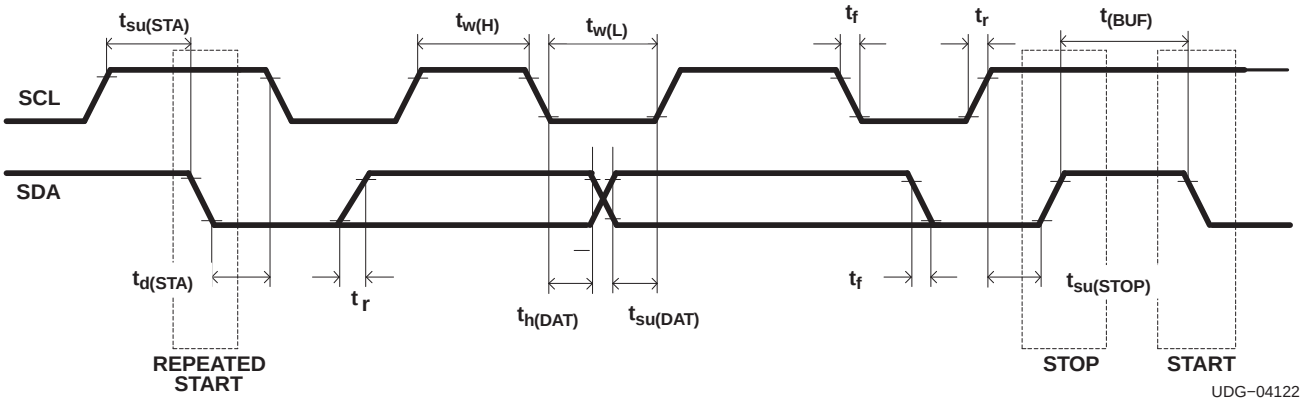

Figure 2. I²C Timing Diagram

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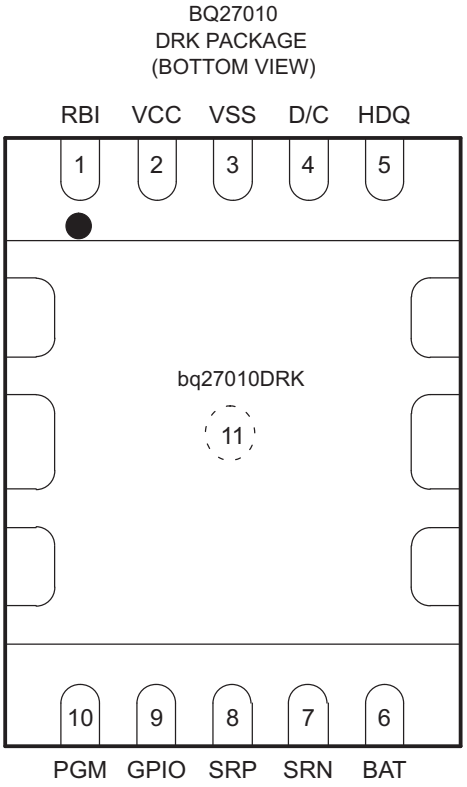
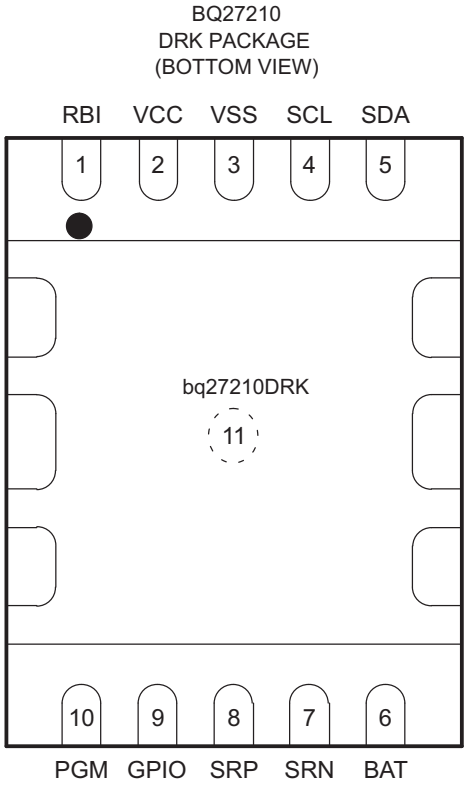
TIMING DIAGRAMS (continued)





DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	bq27010	bq27210 (Preview)		
BAT	6	6	I	Battery voltage sense input
D/C	4	-	-	Do not connect. Must be left floating or tied to V_{SS}
GPIO	9	9	I/O	General purpose input/output
HDQ	5	-	I/O	Single wire HDQ serial interface
PGM	10	10	I	EEPROM programming voltage input
RBI	1	1	I	Register back-up input
SCL	-	4	I	Serial clock input (I^2C)
SDA	-	5	I/O	Serial data input (I^2C)
SRN	7	7	I	Current sense input (negative)
SRP	8	8	I	Current sense input (positive)
VCC	2	2	I	V_{CC} supply input
VSS	3	3	-	Ground input
VSS	11	11	-	Ground shield

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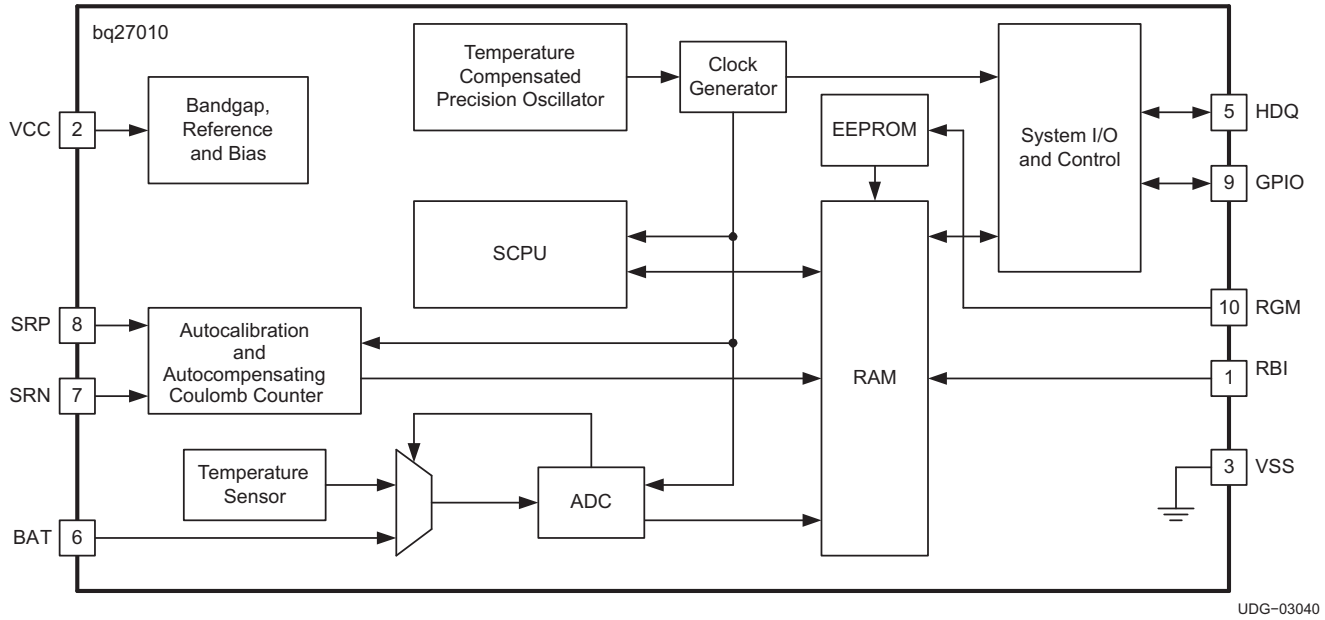
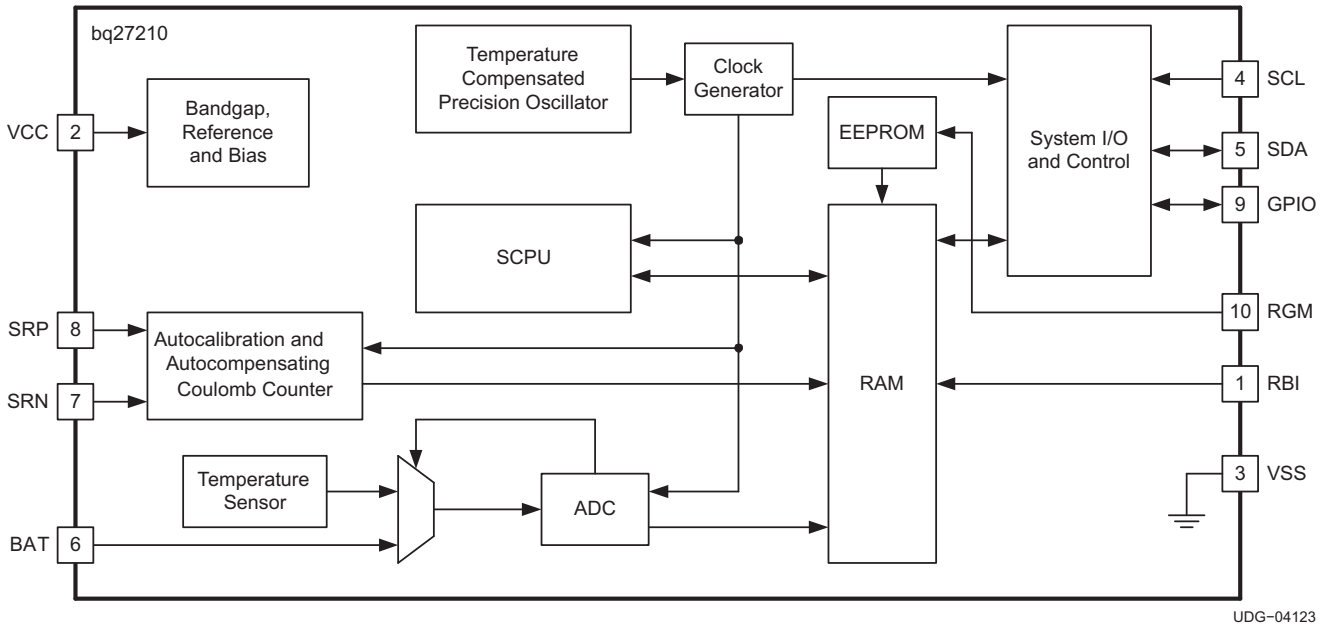
FUNCTIONAL BLOCK DIAGRAMS





FUNCTIONAL DESCRIPTION

The bqJUNIOR determines battery capacity by monitoring the amount of charge input to or removed from a Li-Ion or Li-Pol battery. The bqJUNIOR measures discharge and charge currents, monitors the battery for low voltage thresholds, and compensates for self-discharge, aging, temperature, and discharge rate. Current is measured across a small value series resistor between the negative terminal of the battery and the pack ground (see R_S in Figure 3). Available capacity is reported with a resolution of 3.57 µVh. Time-To-Empty reporting in minutes at standby, actual, and at-rate currents allows the requirements for host-based calculations to be greatly reduced or eliminated; reading a single register pair provides useful and meaningful information to the end user of the application.

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FUNCTIONAL DESCRIPTION (continued)

Figure 3 shows a typical application circuit. Differential sense of the voltage across the current sense resistor, R_S, improves device performance, leading to an improvement in reported time-to-empty accuracy. An internal 3-µA pull-down on the HDQ or SDA and SCL lines ensures that the device detects a logic *0* on the communication lines and allows the device to automatically enter the low-power sleep mode when the system power is switched off or the pack is removed. A 100 kΩ pullup to V_{CC} can be added to the communication lines if this feature needs to be disabled. The bqJUNIOR can operate directly from a single Li-Ion or Li-Pol cell.

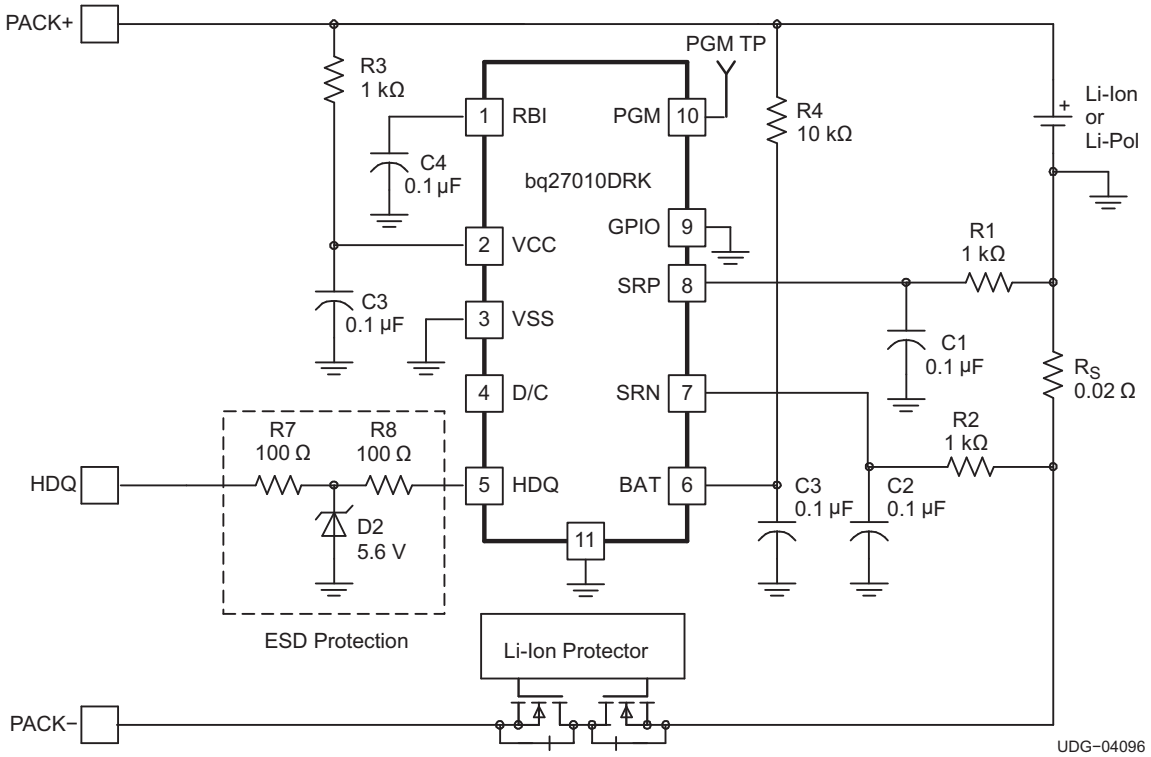

Figure 3. Typical Application Circuit (bq27010)

Measurements

As shown in the functional block diagram, the bqJUNIOR uses a dedicated fully differential Delta-Sigma Coulomb Counter (DSCC) for charge and discharge current and coulometric measurements and an analog-to-digital converter (ADC) for battery voltage and temperature measurements. Both DSCC and ADC are automatically compensated for offset. No user calibration or compensation is required. An EEPROM offset value can be programmed to compensate for contributions to the DSCC offset due to the PCB layout.

Charge and Discharge Coulometric and Current Measurements

The bqJUNIOR uses a DSCC to perform a continuous integration of the voltage waveform across a small value sense resistor in the negative lead of the battery, as shown in Figure 3. The integration of the voltage across the sense resistor is the charge added or removed from the battery. Because the DSCC does a direct integration of the waveform, the shape of the current waveform through the sense resistor does not have any effect on the coulometric measurement accuracy. The low-pass filter that feeds the sense resistor voltage to the bqJUNIOR SRP and SRN inputs filters out system noise and does not affect the coulometric measurement accuracy, because the low-pass filter does not change the integrated value of the waveform. The bqJUNIOR also uses the DSCC to measure current. The reported current is determined by the average voltage across the sense resistor over a 5.12 second interval.

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FUNCTIONAL DESCRIPTION (continued)

Offset Calibration

The offset voltage of the DSCC measurement must be very low to be able to measure small signal levels accurately. The bqJUNIOR provides an auto-calibration feature to cancel the internal voltage offset error across SRP and SRN for maximum charge measurement accuracy. **NO CALIBRATION IS REQUIRED**. External voltage offset error caused by the PCB layout cannot be automatically calibrated out by the gauge, but the external offset can be determined using a built-in user offset measurement command and can be programmed into the EEPROM for inclusion in the offset compensation performed by the gauge. See the *Layout Considerations* section for details on minimizing PCB induced offset across the SRP and SRN pins.

The bqJUNIOR auto-calibration of the DSCC offset is performed from time-to-time as operating conditions change, to keep the measurement error small. A Calibration-In-Progress (CALIP) flag is set in FLAGS to indicate when the operation occurs. Capacity, voltage, and temperature is updated during the 5.12 second offset calibration time, but other parameters are not updated until the calibration has completed. When there is a full reset, the gauge makes an initial quick offset calibration and delays the 5.12 second full offset calibration for at least 40 seconds. This is done to prevent the full 5.12 second calibration operation from interfering with module test functions that need to be performed immediately after power application during manufacturing test. The quick offset calibration after a full reset is a 1.28 second offset measurment used as a delay, followed by a 1.28 second offset measurement that is used as the initial offset value. The 1.28 second delay allows V_{CC} to settle before the initial offset measurement. If manufacturing test does not need the additional V_{CC} settling time or can use a slightly worse initial offset measurement, the tester may write bit *0* of CTRL (address 0x00) to *1* during the first 1.28 seconds after the reset and the first offset sample will be used, cutting the initial quick offset calibration time in half.

Digital Magnitude Filter

The Digital Magnitude Filter (DMF) threshold can be set in EEPROM to indicate a threshold below which any charge or discharge accumulation is ignored. This allows setting a threshold above the maximum DSCC offset expected from the IC and PCB combination, so that when no charge or discharge current is present, the measured capacity change by the bqJUNIOR is zero. Note that even a small offset can add up to a large error over a long period. In addition to setting the threshold above the largest offset expected, the DMF should be set below the minimum signal level to be measured. The sense resistor value should be large enough to allow the minimum current level to provide a signal level substantially higher than the maximum offset voltage. Conversely, the sense resistor must be small enough to meet the system requirement for insertion loss as well as keep the maximum voltage across the sense resistor below the 100 mV maximum that the DSCC can accurately measure.

The DMF threshold is programmed in EEPROM in increments of 4.9 µV. Programming a zero in the DMF value will disable the DMF function and all non-zero DSCC measurements are counted.

Voltage

The bqJUNIOR monitors the battery voltage through the BAT pin and reports an offset corrected value through the internal registers. The bqJUNIOR also monitors the voltage for the end-of-discharge (EDV) thresholds. The EDV threshold levels are used to determine when the battery has been discharged to 6.25% or *empty* and synchronizes the reported capacity to these levels when the programmed EDV thresholds are detected.

Temperature

The bqJUNIOR uses an integrated temperature sensor to monitor the pack temperature and is reported through the internal registers. The temperature measurement is used to adjust compensated available capacity and self-discharge capacity loss.

RBI Input

The Register Backup Current (RBI) input pin is used with an external capacitor to provide backup potential to the internal registers when V_{CC} drops below $V_{(POR)}$. V_{CC} is output on RBI through an internal FET switch when V_{CC} is above $V_{(POR)}$, charging the capacitor. If V_{CC} drops below $V_{(POR)}$, the FET switch from V_{CC} is opened and the capacitor can supply the small data retention current to the internal registers to retain the data content while V_{CC} is absent. Register data will be maintained as long as the RBI voltage remains above 1.3 V.

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FUNCTIONAL DESCRIPTION (continued)

Register Initialization and Data Integrity Checks

Checksums of critical internal register data are continually checked during operation of the bqJUNIOR. A failed checksum comparison will force a hardware reset. After a reset, the bqJUNIOR examines a checksum containing LMD, CYCL, CYCT, and other critical data. If the checksum is incorrect, NAC, CYCL, and CYCT are cleared, LMD and other parameters are initialized from EEPROM, the CI bit in FLAGS is set, and the INIT bit in MODE is set. This process constitutes a full reset. If the checksum is correct, NAC, LMD, CYCL, and CYCT are retained. In addition, a second checksum containing all user-updateable EEPROM coefficients is checked. If the second checksum is incorrect, the values are all initialized from the EEPROM, the CI bit in FLAGS is set, and the INIT bit in MODE is set. The INIT bit is used to inform the host that it may need to reinitialize these values if the default values are not satisfactory. If the second checksum is correct, the INIT bit in MODE will not be set, the CI bit in FLAGS will remain unchanged, and the register data that may have been updated by the host will be retained. This process constitutes a partial reset. It is the host responsibility to clear the INIT bit in MODE after any updates by the host are completed. See CTRL description for more on host updates. Other register values not specifically retained are reinitialized on all resets.

GPIO

The GPIO pin can be used as an input or an output. The initial state can be established by programming bit 7 in the PKCFG EEPROM location. The input/output state can be changed at any time by changing the value in bit 7 of MODE. If unused, the GPIO pin should be tied to V_{SS}.

Layout Considerations

The auto-calibrating DSCC approach effectively cancels the internal offset voltage within the bqJUNIOR, but any external offset caused by PCB layout must be programmed in the EEPROM to be cancelled. The magnitude and variability of the external offset makes it critical to pay special attention to the PCB layout. To obtain optimal performance, the decoupling capacitor from V_{CC} to V_{SS} and the filter capacitors from SRP and SRN to V_{SS} should be placed as closely as possible to the bqJUNIOR, with short trace runs to both signal and V_{SS} pins. All low-current V_{SS} connections should be kept separate from the high-current discharge path from the battery and should tie into the high-current trace at a point directly next to the sense resistor. This should be a trace connection to the edge or inside of the sense resistor connection, so that no part of the V_{SS} interconnections carry any load current and no portion of the high-current PCB trace is included in the effective sense resistor (i.e. Kelvin connection).

Gas Gauge Operation

Figure 4 illustrates an operational overview of the gas gauge function.

The bqJUNIOR reports uncompensated nominal available capacity (NAC), uncompensated last measured discharge (LMD), compensated available capacity (CAC), and full charge compensated available capacity (FCAC). The compensated CAC and FCAC values are reduced from their respective uncompensated NAC and LMD values by an amount that varies with discharge rate, temperature, and cycle count (age). CAC and FCAC will equal their respective uncompensated NAC and LMD values at light loads and when charging.

The bqJUNIOR learns the capacity of the battery during actual use conditions and will update LMD when a valid learning cycle occurs. The bqJUNIOR learns the capacity of the battery by measuring the capacity removed from the battery when it is discharged from full (NAC = LMD) to the first end-of-discharge (EDV1) voltage threshold without any learning cycle disqualifying event. The EDV1 threshold should be programmed to a value determined from battery characterization that affords 6.25% of design capacity (DC) remaining before the battery reaches zero capacity. The measured discharge capacity plus 6.25% of DC is the measured full capacity during actual use (compensated) conditions. LMD will be updated with the measured discharge plus 6.25% of DC plus the capacity compensation value due to discharge rate, temperature, and age. Thus the compensated FCAC value, with the capacity compensation subtracted from it, will match the measured discharge capacity plus the 6.25% of DC unmeasured discharge capacity. The final end-of-discharge (EDVF) threshold is a fixed value and should be set at a voltage that the system sees as the zero-capacity battery voltage. The bqJUNIOR does not learn the capacity between the EDV1 and EDVF thresholds, so the EDV1 threshold should be based on actual battery characterization. The EDV1 threshold can be compensated with discharge rate and temperature to maintain the 6.25% remaining capacity with different use profiles.

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FUNCTIONAL DESCRIPTION (continued)

When the battery is charged to full (NAC = LMD), the valid discharge flag (VDQ) bit in FLAGS will be set. It will remain set during the subsequent discharge until the learning discharge cycle completes or an event occurs that disqualifies the learning cycle. When the battery is discharged to the condition where VOLT ≤ EDV1 threshold, the learning cycle will terminate and LMD will be updated if VDQ is still set. The bqJUNIOR EDV detection is designed to prevent premature detection of the EDV threshold due to dynamic load variations. EDV detection has a dynamically adjusted delay of up to 21.5 seconds with CSOC ≥ 6% and down to 3 seconds when CSOC = 0%. To prevent a severe reduction in LMD due to some abnormal situation, the new LMD value is restricted to a learn-down maximum of DC/8 during any single learning cycle. When the learning cycle completes, LMD is updated and the capacity inaccurate (CI) bit in FLAGS is cleared. The CI bit will remain cleared unless there is a full reset (reset with RAM corruption detected) or the cycle count since the last learning cycle (CYCL) reaches a count of 32.

A learning cycle can be disqualified by any of the following conditions:

1. Cold temperature: Temperature < 0°C when the EDV1 threshold voltage is reached.
2. Light load: A capacity learning cycle is disqualified if average current is less than or equal to 2 times the initial standby load when the EDV1 threshold voltage is reached.
3. Excessive charging: Cumulative Charge > 255 NAC counts (910 µVh) during a learning discharge cycle (alternating discharge/charge/discharge before EDV1 is set).
4. Reset: VDQ is cleared on all resets.
5. Excessive self-discharge: NAC reduction from self-discharge estimate (0.195%) performed 64 times.
6. Self-discharge at termination of learning cycle. If self-discharge estimate causes CAC ≤ DC/16, VDQ is cleared.

NAC is adjusted by charge and discharge coulometric measurements except when battery full or empty conditions are detected. NAC = LMD is forced when IMIN = 1 (full detection) unless Temperature ≤ TCOMP[2:0]*2 (°C). During a discharge with VDQ = 1, CAC is not allowed to drop below DC/16 until EDV1 = 1. If EDV1 = 1 occurs when CAC > DC/16, CAC = DC/16 will be forced. CAC = 0 is forced if EDVF = 1.

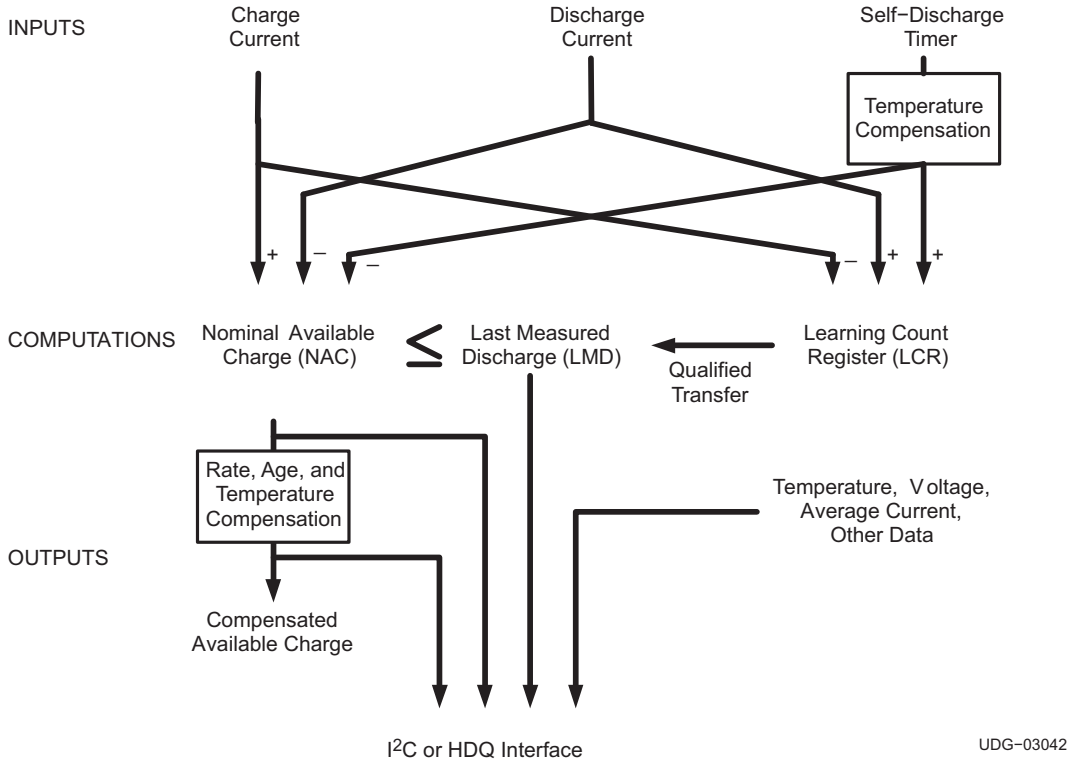

Figure 4. Operational Overview

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FUNCTIONAL DESCRIPTION (continued)

Register Interface

The bqJUNIOR stores all calculated information in RAM, which is backed up by the voltage on the RBI input. EEPROM registers store permanent user data. The memory map for bq27010/bq27210 is shown in Table 1.

Table 1. bq27010/bq27210 Memory Map

ADDRESS	NAME	FUNCTION	UNITS	ACCESS
		EEPROM Registers		
0x7F	TCOMP	Temperature Compensation Constants, OR, ID#1		R/W
0x7E	DCOMP	Discharge Rate Compensation Constants, OR, ID#2		R/W
0x7D	GAF/DEDV	Gain Age Factor / EDVI Rate Compensation		R/W
0x7C	PKCFG	Pack Configuration Values		R/W
0x7B	TAPER	LMD Aging Enable, Charge Termination Taper Current	228 µV(1)	R/W
0x7A	DMFSD	Digital Magnitude Filter and Self-Discharge Rate Constants		R/W
0x79	ISLC/EDVT	Initial Standby Load Current / EDVI Temperature Compensation		R/W
0x78	SEDV1	Scaled EDV1 Threshold		R/W
0x77	SEDVF	Scaled EDVF Threshold		R/W
0x76	ILMD	Initial Last Measured Discharge High Byte	914 µVh(1)	R/W
0x6F - 0x75	-	RESERVED		R
0x6E	EE_EN	EEPROM Program Enable		R/W
0x2D - 0x6D	-	RESERVED		R
		RAM Registers		
0x2C	CSOC	Compensated State-of-Charge	%	R
0x2B - 0x2A	CYCT	Cycle Count Total High - Low Byte	Cycles	R
0x29 - 0x28	CYCL	Cycle Count Since Learning Cycle High - Low Byte	Cycles	R
0x27 - 0x26	TTECP	Time-to-Empty At Constant Power High - Low Byte	Minutes	R
0x25 - 0x22	RSVD	Reserved		R
0x21 - 0x20	CEDV	Compensated EDV Threshold High - Low Byte	mV	R
0x1F - 0x1E	RSVD	Reserved		R
0x1D - 0x1C	STTE	Standby Time-to-Empty High - Low Byte	Minutes	R
0x1B - 0x1A	SI	Standby Current High - Low Byte	3.57 µV(1)	R
0x19 - 0x18	TTF	Time-to-Full High - Low Byte	Minutes	R
0x17 - 0x16	TTE	Time-to-Empty High - Low Byte	Minutes	R
0x15 - 0x14	AI	Average Current High - Low Byte	3.57 µV(1)	R
0x13 - 0x12	FCAC	Full Compensated Available Capacity High - Low Byte	3.57 µVh(1)	R
0x11 - 0x10	CAC	Compensated Available Capacity High - Low Byte	3.57 µVh(1)	R
0x0F - 0x0E	LMD	Last Measured Discharge High - Low Byte	3.57 µVh(1)	R
0x0D - 0x0C	NAC	Nominal Available Capacity High - Low Byte	3.57 µVh(1)	R
0x0B	RSOC	Relative State-of-Charge	%	R
0x0A	FLAGS	Status Flags		R
0x09 - 0x08	VOLT	Reported Voltage High - Low Byte	mV	R
0x07 - 0x06	TEMP	Reported Temperature High - Low Byte	0.25 °K	R
0x05 - 0x04	ARTTE	At-Rate Time-to-Empty High - Low Byte	Minutes	R
0x03 - 0x02	AR	At-Rate High - Low Byte	3.57 µV(1)	R/W
0x01	MODE	Device Mode Register		R/W
0x00	CTRL	Device Control Register		R/W

(1) Divide by Rs in milliohms to convert µV to mA or µVh to mAh.

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APPLICATION INFORMATION

Control and MODE Registers (CTRL/MODE) — Address 0x00/0x01

The device control register is used by the host system to request special operations by the bqJUNIOR. The highest priority command set in the MODE register is performed when the host writes data 0xA9, 0x56, or 0xC5 as indicated to the control register. The CTRL register and MODE bits 5, 4, 3, 1, and 0 are cleared when the command is accepted. The host must set the appropriate command bit in MODE before sending the command key to CTRL.

Mode Register (MODE) — Address 0x01

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMMAND KEY = 0xA9	GPIEN	GPSTAT	WRTNAC	DONE	PRST	INIT	FRST	SHIP (1)
COMMAND KEY = 0x56	GPIEN	GPSTAT	CEO	CIO	WNACCI	INIT	WRTCYC	WRTLMD
COMMAND KEY = 0xC5	GPIEN	GPSTAT	UPDC	UPEDVI	UPDMF	INIT	UPCFG	UPCOMP

(1) bq27010 only

GPIEN GPIEN sets the state of the GPIO pin. A *1* configures the GPIO pin as input, while a *0* configures the GPIO pin as an open-drain output. This bit is initialized to the value of bit 7 of the PKCFG register in the EEPROM. The user should keep this bit set or cleared as desired when other bits in this register are written.

GPSTAT GPSTAT sets the state of the open drain output of the GPIO pin (GPIEN = 0). A *1* turns off the open drain output, while a *0* turns the output on. This bit is set to *1* on POR. When the GPIO pin is an input (GPIEN=1), this bit returns the logic state of the GPIO pin. The user should keep this bit set or cleared as desired when other bits in this register are written.

WRTNAC WRTNAC is used to transfer data from the AR registers to NAC. Other registers are updated as appropriate. This command is useful during the pack manufacture and test to initialize the gauge to match the estimated battery capacity.

DONE DONE is used to write NAC equal to LMD. Useful if the host uses a charge termination method that does not allow the monitor to detect the taper current. The host system could use this command when the charging is complete to force update of internal registers to a full battery condition.

PRST Partial reset. This command requests a reset of all RAM registers except NAC, LMD, and the CI bit in FLAGS. This command is intended for manufacturing use.

INIT The INIT status bit is set to *1* by the bqJUNIOR if there is a full reset or if data corruption is detected in the internal memory containing EEPROM coefficients. Either of these events will cause the bqJUNIOR to update internal memory values. If NAC, LMD, CYCT, or EEPROM-initialized coefficients need to be modified from their original values, the host should first update the values and then clear the INIT bit. The INIT bit is not cleared by the bqJUNIOR.

FRST Full reset. This command bit requests a full reset. A full reset reinitializes all RAM registers, including the NAC, LMD, and FLAGS registers. This command is intended for manufacturing use.

SHIP This command bit requests that the device (bq27010 only) should be put in ship mode. See the *Power Mode* section for a description of the ship mode. This command is intended for manufacturing use.

CEO This command bit requests that the external offset value is measured. Care should be taken to insure that no charge or discharge current flows during the time this measurement is made. The external offset value is the total offset of the DSCC plus any external PCB affects. The result can be read in 0x5f-5e. The result is a signed number with an LSB value of 1.225 µV. The command takes approximately 5.5 seconds to make the measurement. This command is intended for manufacturing use. The CIO offset value may be subtracted from the CEO offset value to determine the external board offset. This value can be programmed into PKCFG[4:2] in the EEPROM for automatic compensation of this external offset value.

CIO This command bit requests that the internal offset value is measured. The internal offset value is

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the offset of the DSCC with an internal short applied from SRP to SRN. The result can be read in 0x5f-5e. The result is a signed number with an LSB value of 1.225 µV. The command takes approximately 5.5 seconds to make the measurement. This command is intended for manufacturing use, along with the CEO command, to determine the external board offset..

WNACCI WNACCI is used to transfer data from the AR registers to NAC. It is identical to the WRTNAC command, but the CI bit in FLAGS is also cleared

The following commands are intended for use by a host-side gauge if the battery pack is changed and the host can determine that the new pack requires different values loaded into the gauge. They can also be used with a pack-side gauge if the default EEPROM values in the bqJUNIOR do not match the required values. If the host only desires to change one of the bytes, the value for the unchanging byte will still have to be read and placed in the appropriate AR byte, as both bytes will be updated when the command is issued. The EEPROM values used by the bq27x010 firmware are located in addresses 0x46 to 0x4F. These addresses are a mirror of the EEPROM values programmed in addresses 0x76 to 0x7F after a full reset, unless DCOMP and/or TCOMP default values are selected by PKCFG[1:0]. Update commands for the EEPROM coefficients will update the appropriate value in the 0x46 to 0x4F address space, but will not affect the value in the 0x76 to 0x7F addresses.

WRTCYC WRTCYC is used to transfer data from the AR registers to CYCT.

WRTLMD WRTLMD is used to transfer data from the AR registers to LMD.

UPDC UPDC is used to simultaneously update the ILMD value (DC) from the ARL register and to update the EDVF value from the ARH register.

UPEDV1 UPEDV1 is used to simultaneously update the EDV1 value from the ARL register and to update the ISLC/EDVT value from the ARH register.

UPDMF UPDMF is used to simultaneously update the DMFSD value from the ARL register and to update the TAPER value from the ARH register.

UPCFG UPCFG is used to simultaneously update the PKCFG value from the ARL register and to update the GAF/DEDV value from the ARH register.

UPCOMP UPCOMP is used to simultaneously update the DCOMP value from the ARL register and to update the TCOMP value from the ARH register.

At-Rate Registers (ARL/ARH) — Address 0x02/0x03

The host can write the current in units of 3.57 µV per bit to this register for predictive calculation time-to-empty. The part uses this value to predict the time-to-empty at any desired current; it does not affect the time-to-empty calculation based on the actual current. The value in AR is always assumed to be a discharge current.

This register is also used during pack manufacturing to input a nominal available-charge value to set NAC to the approximate initial pack capacity value, and to update other values as described in the CTRL register description.

At Rate Time-to-Empty Registers (ARTTEL/ARTTEH) — Address 0x04/0x05

This is predicted time-to-empty in minutes at user-entered discharge rate. The discharge current used in the calculation is entered by the host system in the AR registers. The at-rate capacity (ARCAP) value used can be larger or smaller than CAC. It is computed using the same compensation formulas as CAC, except the discharge compensation is computed using AR, instead of AI, for the discharge rate. The equation used to compute at-rate time-to-empty is:

ARTTE = 60 * ARCAP / AR

The host system has read-only access to this register pair.

Reported Temperature Registers (TEMPL/TEMPH) — Address 0x06/0x07

The TEMPH and the TEMPL registers contain the reported die temperature. The temperature is expressed in units of 0.25 °K and is updated every 2.56 seconds. The equation to calculate reported pack temperature is:

Temperature = 0.25 * (256 * TEMPH + TEMPL)

The host system has read-only access to this register pair.

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Reported Battery Voltage Registers (VOLTL/VOLTH) — Address 0x08/0x09

The VOLTH and the VOLTL low-byte registers contain the reported battery voltage measured on the BAT pin. Voltage is expressed in mV with an LSB resolution of 1 mV. Reported voltage cannot exceed 5000 mV. The host system has read-only access to this register pair. Voltage is updated every 2.56 seconds.

Status Flag Register (FLAGS) — Address 0x0A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	CHGS	NOACT	IMIN	CI	CALIP	VDQ	EDV1	EDVF
POR STATUS	0	0	0	1	0	0	0	0

CHGS Charge State flag. A *1* in the CHGS indicates a charge current ($V_{SRP} > V_{SRN}$). A *0* indicates a lack of charge activity. This bit should be read when the host system reads the Average Current register pair to determine the sign of the average current magnitude. This bit is cleared to *0* on all resets.

NOACT No Activity flag. A *1* indicates that the voltage across R_S is less than the digital magnitude filter. See the *Digital Magnitude Filter* section for more information. This bit is cleared to *0* on all resets.

IMIN Li-ion taper current detection flag. A *1* indicates that the charge current has tapered to less than the value set in EEPROM and that the battery voltage is greater than or equal to the value selected by the QV0 and QV1 bits in the PKCFG register (see EEPROM Data Register description for more details). Taper current detection is disqualified if AI < 8 (28.6 µV across sense resistor). The taper detection conditions must be maintained for 4 successive average current measurements (20-25 s) to qualify as a valid taper current detection. This bit is cleared to *0* on all resets.

CI Capacity Inaccurate flag. A *1* indicates that the firmware has not been through a valid learning cycle and is basing all calculations on initial design values programmed into EEPROM or that there have been at least 32 cycle-count increments since the last learning cycle. This bit is cleared only on a LMD update following a learning cycle. This bit is set to *1* on a full reset. The previous value is retained if no RAM corruption is detected after a reset.

CALIP Calibration-In-Progress flag. This flag is set whenever an automatic or commanded offset calibration measurement is being made. This bit is set to *0* on all resets.

VDQ Valid Discharge flag. A *1* indicates that the bqJUNIOR has met all necessary requirements for the firmware to learn the battery capacity. This bit clears to *0* on a LMD update or condition that disqualifies a learning cycle. This bit is cleared to *0* on all resets.

EDV1 First End-of-Discharge-Voltage flag. A *1* indicates that the voltage on the BAT pin is less than or equal to the EDV1 threshold voltage. LMD updates immediately if the VDQ bit is set when this bit transitions from *0* to 1. This bit is cleared when charging and on all resets.

EDVF Final End-of-Discharge-Voltage flag. A *1* indicates that the voltage on the BAT pin is less than or equal to the EDVF threshold voltage. This bit is cleared when charging and on all resets.

The host system has read-only access to this register.

Relative State-of-Charge (RSOC) — Address 0x0B

RSOC reports the nominal available capacity as a percentage of the last measured discharge value (LMD). The equation is:

RSOC (%) = 100 * NAC/LMD

The host system has read-only access to this register.

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Nominal Available Capacity Registers (NACL/NACH) — Address 0x0C/0x0D

This register pair reports the light-load, or uncompensated, capacity available from the battery. NAC increments during charge ($V_{SRP} > V_{SRN}$) if Voltage > EDVF threshold and decrements during discharge ($V_{SRP} < V_{SRN}$). The NAC registers are cleared by a reset if RAM corruption is detected. The register value is retained after a reset if RAM corruption is not detected. The host system has read-only access to this register pair. NAC is reported in units of 3.57 µVh per count.

Last Measured Discharge Registers (LMDL/LMDH) – Address 0x0E/0x0F

This register pair reports the light load, or uncompensated, capacity available from the battery when fully charged. This value is updated after a valid learning cycle, which occurs when the battery is discharged from fully charged (NAC = LMD) until the EDV1 voltage threshold is detected (EDV1 = 1) without any learning cycle disqualifying event (VDQ = 1 during entire discharge). LMD will be updated with the measured capacity removed from the battery during the discharge until the EDV1 threshold is reached plus 6.25% of design capacity (the unmeasured capacity from EDV1 until the EDVF zero capacity threshold voltage) plus the computed capacity compensation reduction due to discharge rate, temperature, and age. The host system has read-only access to this register pair. LMD is reported in units of 3.57 µVh per count.

Compensated Available Capacity (CACL/CACH) – Address 0x10/0x11

This register pair reports the available capacity in the battery at the present discharge rate, temperature, and age. CAC is equal to NAC minus the capacity compensation reduction based on the compensation coefficients programmed in DCOMP (discharge compensation coefficients), TCOMP (temperature compensation coefficients), and GAF/DEDV (gain age compensation coefficient). All compensations are impedance-based and CAC will equal NAC at very low currents. However, CAC is not allowed to increase as long as there is no charging current. If the discharge load is reduced, CAC may stop decrementing even though NAC continues to decrement. When NAC drops sufficiently that the NAC minus CAC difference is equal to the discharge compensation at the reduced load current, CAC will again start decrementing. CAC will equal NAC when charging. The host system has read-only access to this register pair. CAC is reported in units of 3.57 µVh per count.

Fully-Charged Compensated Available Capacity (FCACL/FCACH) – Address 0x12/0x13

This register pair reports the fully-charged capacity of the battery at the present discharge rate, temperature, and age. FCAC is equal to LMD minus the capacity compensation reduction based on the compensation coefficients programmed in DCOMP (discharge compensation coefficients), TCOMP (temperature compensation coefficients), and GAF/DEDV (gain age compensation coefficient). All compensations are impedance-based and FCAC will converge to LMD as the measured discharge current approaches zero. FCAC will equal LMD when charging. The host system has read-only access to this register pair. FCAC is reported in units of 3.57 µVh per count.

Average Current Registers (AIL/AIH) — Address 0x14/0x15

This register pair reports the magnitude of the average current through the sense resistor. The value is reported with a resolution of 3.57 µV per count. Use the following equation to convert the value to mA, where R_S is the sense resistor value in milliohms:

Average Current = (256 * AIH + AIL) * 3.57 / R_S

The current reported is an average over the last 5.12 seconds. The host system has read-only access to this register pair.

Time-to-Empty Registers (TTEL/TTEH) — Address 0x16/0x17

This register pair reports calculated time-to-empty at the measured discharge rate. This value is based on the temperature and discharge rate compensated available charge and the average current. The equation to calculate TTE is:

TTE = 60 * CAC / AI

TTE is reported in minutes. The host system has read-only access to this register pair.

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Time-to-Full Registers (TTFL/TTFH) — Address 0x18/0x19

This register pair reports calculated time-to-full at the measured charge rate. The time computed at the average current charge rate is extended by 50% to estimate the effect of the current taper. TTF is reported in minutes. The equation for TTF is:

TTF = 60 * 1.50 * (LMD-NAC) / AI

The host system has read-only access to this register pair.

Standby Current Registers (SIL/SIH) — Address 0x1A/0x1B

This register pair reports measured standby current through the sense resistor. The standby current is an adaptive measurement. Initially, the register pair reports the standby current programmed in EEPROM and after spending some time in standby, the register pair reports the measured standby current. The register value is updated every 5.12 seconds when the measured current is above the DMF threshold and is less than or equal to 2x the initial programmed standby current value. Each new SI value is computed as follows:

SI_{NEW} = (15/16) * SI_{OLD} + (1/16) * AI

This filter function allows the reported standby current to shift towards the actual measured current with a time constant of approximately 67 seconds. The value is reported with a resolution of 3.57 µV per bit. Use the following equation to convert the value to mA, where R_S is the sense resistor value in milliohms:

Standby Load Current = (256 * SIH + SIL) * (3.57 / R_S)

The host system has read-only access to this register pair.

Standby Time-to-Empty Registers (STTEL/STTEH) — Address 0x1C/0x1D

This register pair reports calculated time-to-empty at the measured standby current value. This value is based on the nominal available charge and the standby current. STTE is reported in minutes. STTE is calculated by:

STTE = 60 * NAC/SI

The host system has read-only access to this register pair.

Compensated End-of-Discharge Registers (CEDVL/CEDVH) – Address 0x20/0x21

The EDV1 threshold can be compensated for discharge rate and temperature. The compensated, or computed, EDV1 threshold is displayed in this register pair. The CEDV display is only updated during discharge. There is a floor set for the EDV1 threshold. The EDV1 threshold will be the greater of the computed CEDV threshold and EDVF + 32 mV. CEDV is displayed in millivolts. The host system has read-only access to this register pair.

Time-to-Empty at Constant Power Registers (TTECPL/TTECPH) – Address 0x26/0x27

TTECP is the time-to-empty in minutes with a constant-power load. TTECP is equal to the TTE constant-current value scaled to reflect a future drop in battery voltage that would cause the load current to increase. The calculation assumes a linear voltage drop down to EDVF, yielding a conservative (smaller) run-time than expected.

TTECP = TTE * (VOLT + EDVF) / (2 * VOLT)

The host system has read-only access to this register pair.

Cycle Count Since Learning Cycle Registers (CYCLL/CYCLH) — Address 0x28/0x29

CYCL is the cycle count since the last learning cycle. Each count indicates an increment of CYCT since there was a learning cycle. This register is cleared every time there is a learning cycle. When this count reaches 32, it forces the CI flag in FLAGS to a 1. The host system has read-only access to this register pair.

Cycle Count Total Registers (CYCTL/CYCTH) — Address 0x2A/0x2B

CYCT is the cycle count since a full reset. A full reset clears this register. Each count indicates a cumulative discharge equal to the Design Capacity (256 * ILMD). The host system has read-only access to this register pair.

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Compensated State-of-Charge (CSOC) — Address 0x2C

CSOC reports the compensated available capacity as a percentage of the last measured discharge value (LMD). The equation is:

CSOC (%) = 100 * CAC / LMD

The host system has read-only access to this register.

Reserved Registers

Addresses 0x1E, 0x1F, 0x22-0x25, 0x2D-0x6D and 0x6F-0x75 are reserved and cannot be written by the host.

EEPROM Enable Register (EE_EN) — Address 0x6E

This register is used to enable host writes to EEPROM data locations (addresses 0x76 — 0x7F). The host must write data 0xDD to this register to enable EEPROM programming. See the *Programming the EEPROM* section for further information on programming the EEPROM bytes. Care should be taken to insure that no value except 0xDD is written to this location. All bqJUNIOR measurements and computations will be inhibited until 0x00 is written back to address 0x6E.

EEPROM Data Registers (EE_DATA) — Address 0x76 — 0x7F

The EEPROM data registers contain information vital to the performance of the device. These registers are to be programmed during pack manufacturing to allow flexibility in the design values of the battery to be monitored. The EEPROM data registers are listed in Table 2. Detailed descriptions of what should be programmed follow. See the *Programming the EEPROM* section for detailed information on writing the values to EEPROM.

Table 2. bq27010/bq27210 EEPROM Memory Map

Address	Name	Function
0x7F	TCOMP	Temperature compensation constants, OR, ID#1
0x7E	DCOMP	Discharge rate compensation constants, OR, ID#2
0x7D	GAF/DEDV	Gain Age Factor / EDVI rate compensation
0x7C	PKCFG	Pack configuration values
0x7B	TAPER	Aging estimate enable [7], charge termination taper current [6:0]
0x7A	DMFSD	Digital magnitude filter and self-discharge rate constants
0x79	ISLC/EDVT	Initial standby load current / EDVI temperature compensation
0x78	SEDV1	Scaled EDV1 threshold
0x77	SEDVF	Scaled EDVF threshold
0x76	ILMD	Initial last measured discharge high byte

Initial Last Measured Discharge High Byte (ILMD) — Address 0x76

This register contains the scaled design capacity of the battery to be monitored. ILMD is programmed in units of 914 µVh per bit. The equation to calculate the initial LMD is:

ILMD = Design Capacity (mAh) * R_S (mΩ) / (256 * 3.57)

where R_S is the value of the sense resistor used in the system. This value is used to initialize the high byte of LMD on a full reset. The low byte of LMD is initialized to 0.

Scaled EDVF Threshold (SEDVF) — Address 0x77

This register contains the scaled value of the threshold for zero battery capacity. To calculate the value to program, use the following equation:

SEDVF = Design EDVF (mV) / 8 – 256

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Scaled EDV1 Threshold (SEDV1) — Address 0x78

This register contains the scaled value of the voltage when the battery has 6.25% remaining capacity at a very light load. DEDV and EDVT coefficients can be programmed to reduce the EDVI threshold at heavier loads and at cold temperatures. When the battery reaches this threshold during a valid discharge, the device learns the full battery capacity, including the remaining unmeasured 6.25%. See the *bqJUNIOR Capacity Learning* section for more information on the learning cycles of the device. To calculate the value to program, use the following equation:

SEDV1 = Design EDV1 (mV) / 8 – 256

Initial Standby Load Current and EDV1 Temperature Compensation (ISLC/EDVT) – Address 0x79

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Name	0	ISLC[2]	ISLC[1]	ISLC[0]	EDVT[3]	EDVT[2]	EDVT[1]	EDVT[0]

The most significant nibble in this register contains the initial standby load current (ISLC) that is transferred to SI on all resets. The gauge will use this initial value, but will learn the actual system standby current by averaging in measured discharge currents above the DMF threshold and less than or equal to 2 times the ISLC value. ISLC is programmed in units of 57.1 μV per bit.

A capacity learning cycle is disqualified if average current is less than or equal to 2 times the ISLC programmed value.

The equation for programming ISLC is:

ISLC = Design Standby Current (mA) * R_S (mΩ) / 57.1 μV, where R_S is the sense resistor value.

The least significant nibble in this register contains the EDV1 temperature compensation (EDVT) coefficient. The temperature compensation is impedance-based, so the resulting compensation is proportional to load current. EDVT is programmed to increase the EDV1 rate compensation (programmed in the DEDV coefficient) by 0.78% per count for each degree than temperature is below the T_{off} threshold programmed in TCOMP. See the GAF/DEDV section for the complete EDV1 compensation equation.

Digital Magnitude Filter and Self-Discharge Values (DMFSD) — Address 0x7A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DMF[3]	DMF[2]	DMF[1]	DMF[0]	SD[3]	SD[2]	SD[1]	SD[0]

DMF[3:0] Sets the digital magnitude filter threshold. See the *bqJUNIOR Digital Magnitude Filter* section for more information on the function of the DMF. The value to be programmed is: DMF[3:0] = Design Threshold / 4.9

SD[3:0] Sets the self-discharge rate % per day value at 25°C. The value to be programmed is: SD[3:0] = 1.61 / Design SD

NAC is reduced with an estimated self-discharge correction to adjust for the expected self-discharge of the battery. This estimation is performed only when the battery is not being charged. The rate programmed in EEPROM for DMFSD determines the self-discharge when 20°C ≤ TEMP < 30°C. The self-discharge estimation is doubled for each 10°C decade hotter than the 20-30°C decade, up to a maximum of 16 times the programmed rate for TEMP ≥ 60°C and is halved for each 10°C decade colder than the 20-30°C decade, down to a minimum of 1/4th the programmed rate for TEMP < 0°C. The self-discharge estimation is performed by reducing NAC by NAC / 512 at a time interval that achieves the desired estimation. If DMFSD is programmed with 8 decimal, the self-discharge rate is 0.195% per day in the 20-30°C decade. This is accomplished by reducing NAC by NAC / 512 (100 / 512 = 0.195%) a single time every 23.3 hours (0.195 * 24 / 23.3 = 0.2). If temperature rises by 10°C, the 0.195% NAC reduction is made every 11.65 hours for a 0.4% per day reduction. If TAPER[7] = 1, capacity aging is enabled, and there is an LMD reduction of 0.1% (Design Capacity / 1024) every time there are 8 NAC self-discharge estimate reductions without charging the battery to full.

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Taper Current (TAPER) — Address 0x7B

This register contains the enable bit for the capacity aging estimate and the charge taper current value. The taper current value, in addition to battery voltage, is used to determine when the battery has reached a full charge state. The equation for programming the taper current is:

TAPER[6-0] = Design Taper Current (mA) * R_S(mΩ) / 228 µV

where R_S is the value of the sense resistor used in the system.

TAPER[7] should be set to *1* to enable the automatic aging of the LMD full capacity value when there are no learning cycles. If this feature is enabled, LMD is reduced by Design Capacity / 1024 every time CYCL increments by 2 and every time that a cumulative NAC self-discharge estimate reduction of 1.56% has been made without charging the battery to full. If TAPER[7] is set to 0, there is no LMD reduction with cycle count or self-discharge.

Pack Configuration (PKCFG) — Address 0x7C

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	GPIEN	QV1	QV0	BOFF(2)	BOFF(1)	BOFF(0)	DCFIX	TCFIX

GPIEN Allows the pack manufacturer to set the state of the GPIO pin on initial power up. If the bit is 0, the GPIEN bit is cleared on reset and the GPIO pin acts as a high-impedance output. If the bit is 1, the GPIEN bit is set on reset and the GPIO pin acts as an input. The state of the GPIO pin can then be read through the GPSTAT bit in the MODE register. If PKCFG is updated using the UPCFG host command (see Device Control section), the updated PKCFG value will not reinitialize GPIEN in the MODE register.

QV1 & QV0 These bits set the minimum qualification voltage for charge termination. The termination voltage thresholds are set as listed in Table 3.

Table 3. Charge Termination Voltage Settings

QV1	QV0	Voltage (mV)
0	0	3968
0	1	4016
1	0	4064
1	1	4112

BOFF These bits are used to store a typical board offset value for the gauge. This value is added to the internal offset measurement and the total applied as an offset correction for the charge and discharge coulometric measurements made by the DSCC. This is a 2s-complement signed number with a value of 2.45 µV per bit.

Table 4. Board Offset Voltage Settings

Board Offset	BOFF(2)	BOFF(1)	BOFF(0)
7.35 µV	0	1	1
4.9 µV	0	1	0
2.45 µV	0	0	1
0	0	0	0
-2.45 µV	1	1	1
-4.9 µV	1	1	0
-7.35 µV	1	0	1
-9.8 µV	1	0	0

DCFIX Fixed discharge compensation. Normal discharge rate compensation (DCOMP register) is used if this bit is set to 0. If this bit is set to 1, the device assumes a fixed value of 0x6C for DCOMP, giving a discharge rate compensation gain (DCGN) of 5.08% with a compensation offset threshold of C/2. Setting the bit to *1* frees the EEPROM location of 0x7E for use as a programmable identification byte.

TCFIX Fixed temperature compensation. Normal temperature compensation (TCOMP register) is used if this bit is set to 0. If this bit is set to 1, the device assumes a fixed value of 0x46 for TCOMP, which will increase DCGN by 25% per °C below 12°C. Setting this bit to *1* frees the EEPROM location of 0x7F for use as a programmable identification byte.

Gain Age Factor and EDV1 Discharge Rate Compensation (GAF/DEDV) – Address 0x7D

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	GAF[1]	GAF[0]	DEDV[5]	DEDV[4]	DEDV[3]	DEDV[2]	DEDV[1]	DEDV[0]

The two most significant bits in address 0x7d set the gain age factor (GAF). This factor adjusts the discharge rate compensation with age. The GAF will cause a linear increase in the discharge rate and temperature compensation with cycle count. GAF = 3 will cause DCGN to increase by same amount as a drop in temperature of 16°C below the Toff threshold programmed in TCOMP when CYCT = 85. Lower values of GAF will require proportionally more cycle counts to reach the same level of compensation reduction. The equation for the aged discharge compensation gain (ADCGN) is:

ADCGN = DCGN * (1 + TCGN * (CYCT/16) * GAF/32)

TCGN is the temperature compensation gain programmed in TCOMP. See the section on DCOMP for the complete discharge rate compensation equation. There will be no gain aging of the discharge compensation if GAF = 0. The recommended value for GAF if battery aging data is not available is GAF = 1.

The six least significant bits in address 0x7d set the EDV1 discharge rate compensation (DEDV) gain. The EDV1 threshold is impedance-based and will be reduced from the no-load EDV1 threshold programmed in SEDV1 as a function of load current. The EDV1 threshold is reduced linearly with AI at a rate of 8 mV per C-rate for each DEDV count. The DEDV rate compensation is also increased at cold temperature as described in the section on ISLC / EDVT. The actual EDV1 threshold used will be the greater of CEDV or EDVF + 32mV. The equation for the EDV1 threshold compensation is:

CEDV = EDV1 – 8 mV * DEDV * AI / DC * [1 + EDVT * (T_{off}– T) / 128] , where T < T_{off}

CEDV = EDV1 – 8 mV * DEDV * AI / DC, where T ≥ T_{off}

Discharge Rate Compensation Coefficients (DCOMP) – Address 0x7E

This register is used to set the basic discharge compensation coefficients. The basic discharge gain coefficient, DCGN, is increased at cold temperature and with age (cycle count) to achieve a combined impedance-based discharge rate, temperature, and age compensation of available capacity. This compensation determines the reduction in CAC from NAC and the reduction in FCAC from LMD.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DCGN[4]	DCGN[3]	DCGN[2]	DCGN[1]	DCGN[0]	DCOFF[2]	DCOFF[1]	DCOFF[0]

DCGN[4:0] The discharge rate compensation gain coefficient sets the slope of the capacity compensation with discharge current. The slope can be set in increments of 0.39% (DCGN / 256).

DCOFF[2:0] The discharge compensation offset coefficient sets the capacity offset threshold. There is no capacity compensation reduction if the compensation falls below this threshold. Table 3 lists shows the discharge compensation threshold is set in multiples of C/8. (A 1C-rate current is the current that equals the design capacity, or AI = ILMD * 256.)

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Discharge Rate Compensation Threshold

DCOFF[2:0]	DCOFF Threshold (1)
0	0
1	(DCGN / 256) * 1C / 8
2	(DCGN / 256) * 2C / 8
3	(DCGN / 256) * 3C / 8
4	(DCGN / 256) * 4C / 8
5	(DCGN / 256) * 5C / 8
6	(DCGN / 256) * 6C / 8
7	(DCGN / 256) * 7C / 8

(1) C = ILMD * 256

The discharge compensation capacity reduction (DCMP) is a function of discharge rate, temperature, and age (cycle count). There is no compensation if the DCGN factor increased for age and temperature times AI is less than the DCOFF threshold (DCMP ≥ 0). The following is the combined equation for the DCMP reduction:

DCMP = AI * (ADCGN / 256) * (1 + TCGN * (273 + TOFF – T) / 32) – DCGN * DCOFF * ILMD / 8

ADCGN = DCGN * (1 + TCGN * (CYCT / 16) * GAF / 32)

If PKCFG[1] = 1, the bqJUNIOR assumes a fixed value of 0x6C for DCOMP, giving a discharge rate compensation gain of 5.08% with a compensation offset threshold of C/2. This frees the EEPROM location of 0x7E for use as a programmable identification byte. If DCOMP is updated using the UPCOMP host command (see Device Control section), the value written by the host for DCOMP will be used regardless of the bit 1 value in PKCFG.

Temperature Compensation Coefficients (TCOMP) – Address 0x7F

This register is used to set the compensation coefficients for temperature. These coefficients are used to scale the aged discharge rate compensation for improved accuracy of predicted available capacity at cold temperatures.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	TCGN[4]	TCGN[3]	TCGN[2]	TCGN[1]	TCGN[0]	TOFF[2]	TOFF[1]	TOFF[0]

TCGN[4:0] The temperature compensation gain coefficient is used to scale DCGN when temperature drops below the T_{off} threshold. TCGN will increase the ADCGN value in increments of 3.125% (TCGN / 32) for each degree that temperature is below the T_{off} threshold.

TOFF[2:0] The temperature compensation offset threshold sets the temperature above which there is no temperature compensation applied to DCGN. This threshold is also used as the threshold for application of cold temperature compensation of EDV1 (see GAF/EDVT section) and the threshold to allow the NAC = LMD capacity adjustment to be made at IMIN detection (see Functional Description section). The T_{off} threshold in degrees Celsius is equal to 2 * TOFF.

If PKCFG[0] = 1, the bqJUNIOR assumes a fixed value of 0x46 for TCOMP. This will increase the DCGN factor by 25% per degree below T_{off} of 12°C. This frees the EEPROM location of 0x7F for use as a programmable identification byte. If TCOMP is updated using the UPCOMP host command (see Device Control section), the value written by the host for TCOMP will be used regardless of the bit 0 value in PKCFG.

Power Modes

The bqJUNIOR has five power modes: Active, Sleep, Ship, Hibernate, and Data Retention (RBI). Figure 5 shows the flow that moves the device between the Active, Sleep, and Ship modes. Hibernate and Data Retention are special modes not included in the flow. Detailed explanations of each mode follow the diagram in Figure 5.

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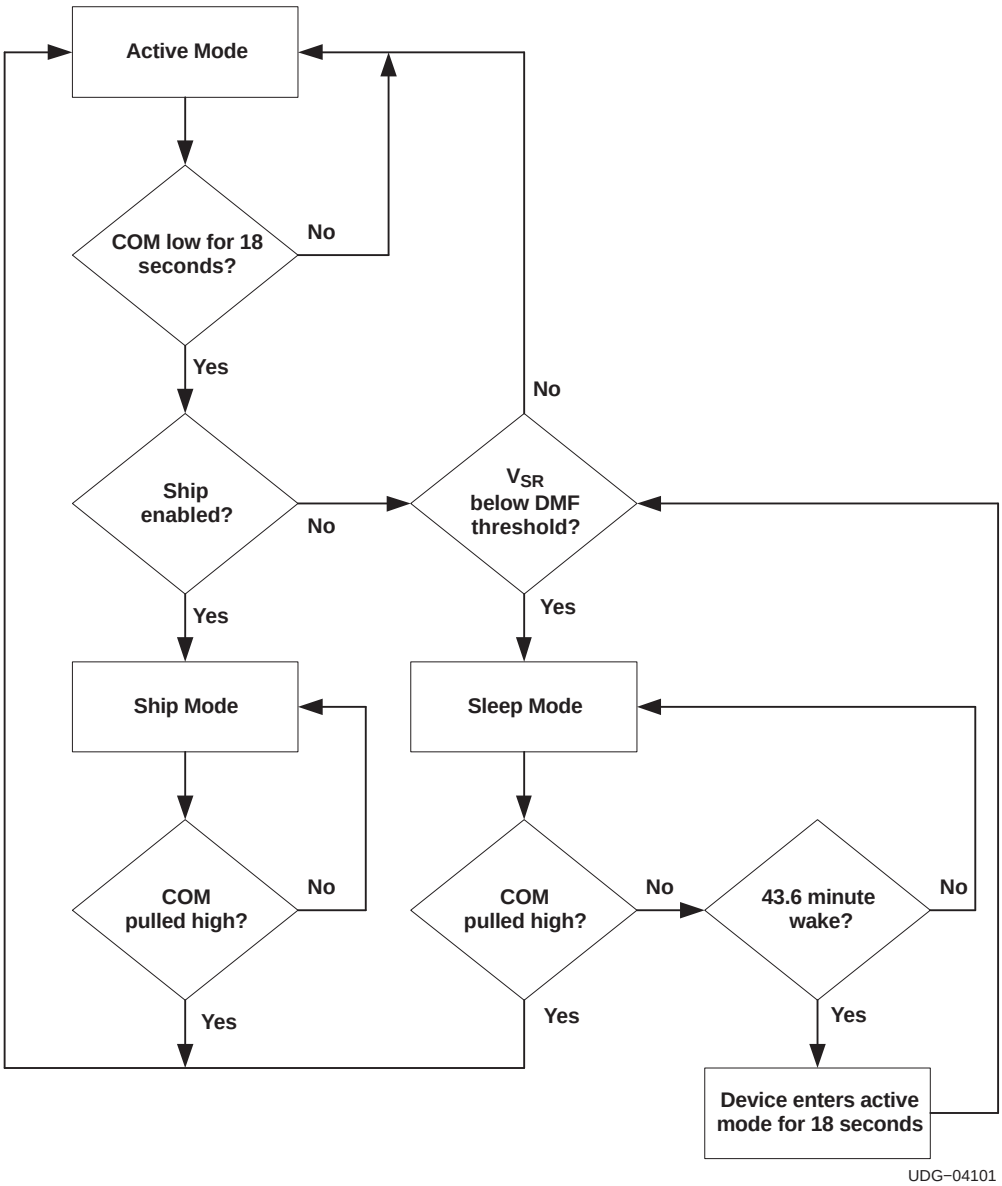

Figure 5. Power Mode Flow Chart

Active Mode

During normal operation, the device is in active mode, which corresponds to the highest power consumption. Normal gas gauging is performed in this mode. If system requirements mandate that bqJUNIOR should not enter Sleep or Ship modes, then an external pullup resistor from V_{CC} to keep HDQ or CLK and DTA at a logic *1* is required on the bqJUNIOR side of the system. The resistor value chosen should be small enough to force a logic *1* even with the internal pulldown current and any external ESD protection circuitry loading.

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Sleep Mode

This low power mode is entered when the HDQ or CLK and/or DTA line is pulled low for at least 18 seconds and the charge or discharge activity is below the DMF threshold. Normal gas gauging ceases, but battery self-discharge, based on the temperature when the device entered sleep mode, is maintained internally. The device wakes every 43.6 minutes to update the temperature measurement and goes back to sleep after about 18 seconds if the HDQ or CLK and/or DTA line is still low and the charge or discharge activity is still below the DMF threshold. The bqJUNIOR has an internal 3 µA pulldown current on each communication line, eliminating the need to add external pulldown resistors to force a logic *0* on open communication lines.

When the device wakes, it stays in active mode long enough to confirm that the charge or discharge activity is still below the digital magnitude filter threshold. This is meant to minimize possible error if the battery pack is removed from the end equipment for a short period of time and then reinserted, and there is not a transient on the communication lines to pull the device into the active mode. This is an issue only if the system has some current drain from the battery even though the communication lines are low. The gauge reenters sleep mode when the charge or discharge activity falls below the digital magnitude filter threshold.

When all communication lines are pulled high, the device leaves the sleep mode. If the DMF threshold is set to zero and a communication line is pulled low, the device does not enter sleep mode until the average current value is less than 3.57 µV/Rsr.

If the battery pack can be removed and placed on an external charger, the charger should have a pull-up resistor on the HDQ or SCL and SDA lines to wake the part from sleep. A 100 kΩ pullup resistor from communication line(s) to V_{CC} can be added in the battery pack to disable the sleep function.

Ship Mode (bq27010 only)

This low power mode is to be used when the pack manufacturer has completed assembly and test of the pack. The ship mode is enabled by setting the SHIP bit in the MODE register and issuing the control command (data 0xA9 to register 0x00). Ship mode is entered only when the ship mode is enabled and the HDQ or CLK and/or DTA line has been pulled low for at least 18 seconds. This allows the pack manufacturer to enable the ship mode and pull the pack from the test equipment without any additional overhead. Transients on a communication line after the ship mode has been enabled but before the device has entered ship mode, do not cause the device to stay in active mode. Transients on a communication line, after the device has entered ship mode can wake the part from ship mode, but if there is no charge or discharge activity above the DMF threshold, the part automatically enters the Sleep mode as previously described.

All device functionality stops in ship mode and it does not start again until the communication lines are pulled high or the battery voltage drops below and then rises above the $V_{(POR)}$ threshold. A full reset is forced when the part leaves ship mode. If the current NAC value must be retained after waking, ship mode should not be used.

Hibernate Mode

The device enters hibernate mode when V_{CC} drops below $V_{(POR)}$. V_{CC} must be raised above $V_{(POR)}$ in order to exit the hibernate mode. If RBI voltage does not drop below 1.3 V, RAM content is maintained and allows retention of NAC, LMD, CYCL, CYCT, and the CI flag after V_{CC} is raised above $V_{(POR)}$.

Programming the EEPROM

The bqJUNIOR has 10 bytes of EEPROM that are used for firmware control and application data (see the *bqJUNIOR Register Descriptions* section for more information). Programming the EEPROM should take place during pack manufacturing because a 21 V pulse is needed on the PROG pin. The programming mode must be enabled prior to writing any values to the EEPROM locations. The programming mode is enabled by writing to the EE_EN register (address 0x6E) with data 0xDD. Once the programming mode is enabled, the desired data can be written to the appropriate address. Figure 6 shows the method for programming all locations.

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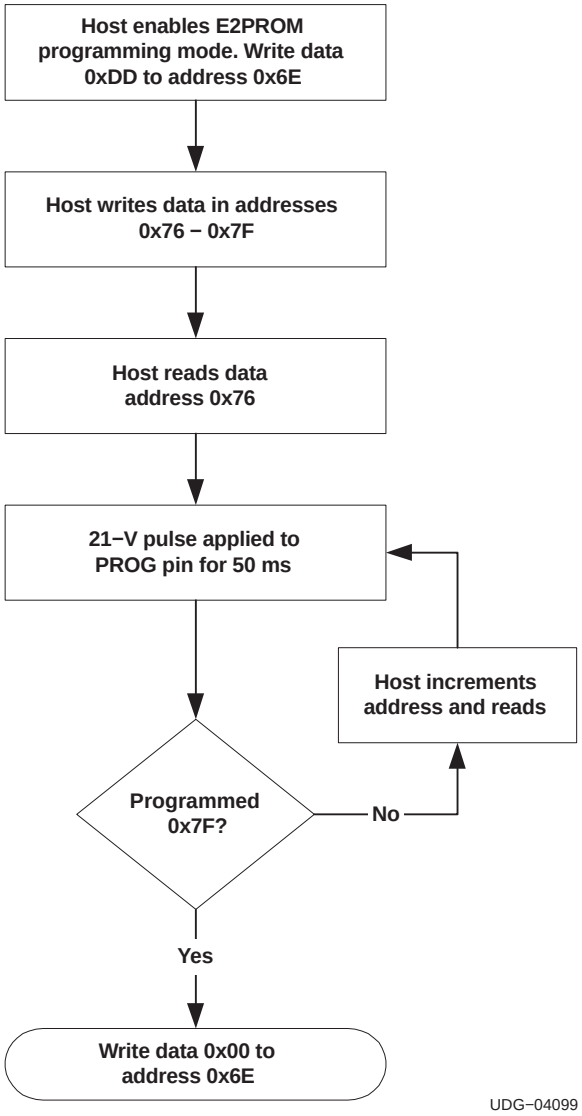

Figure 6. EEPROM Programming Flow

It is not required that addresses 0x76 — 0x7F be programmed at the same time or in any particular order. The programming method illustrated in Figure 6 can be used to program any of the bytes as long as the sequence of Enable, Write, Read, Apply Programming Pulse, and Disable is followed.

The bqJUNIOR must have a full reset to force the updated EEPROM values into RAM. A full reset will occur after a POR if RAM data is corrupted (failed checksum), or a full-reset command may be sent using the CTRL and MODE registers.

Communicating With the bq27010 (HDQ interface)

The bq27010 includes a single-wire HDQ serial data interface. Host processors, configured for either polled or interrupt processing, can use the interface to access various bq27010 registers. The HDQ pin is an open-drain device, which requires an external pullup resistor. The interface uses a command-based protocol, where the host processor sends a command byte to the bq27010. The command directs the bq27010 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data from a register specified by the command byte.

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The communication protocol is asynchronous return-to-one and is referenced to V_{SS}. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5 Kbits/s. The least-significant bit of a command or data byte is transmitted first. Data input from the bqJUNIOR can be sampled using the pulse-width capture timers available on some microcontrollers. A UART can also be configured to communicate with the bq27010.

If a communication timeout occurs (for example, if the host waits longer than $T_{(RSPS)}$ for the bq27010 to respond) or if this is the first access command, then a BREAK should be sent by the host. The host may then resend the command. The bq27010 detects a BREAK when the HDQ pin is driven to a logic-low state for a time $T_{(B)}$ or greater. The HDQ pin then returns to its normal ready-high logic state for a time $T_{(BR)}$.The bq27010 is then ready for a command from the host processor.

The return-to-one data-bit frame consists of three distinct sections:

1. The first section starts the transmission by either the host or the bq27010 taking the HDQ pin to a logic-low state for a period equal to $T_{(HW1)}$ or $T_{(DW1)}$.
2. The next section is the actual data transmission, where the data should be valid for $T_{(HW0)}$- $T_{(HW1)}$ or $T_{(DW0)}$- $T_{(DW1)}$.
3. The final section stops the transmission by returning the HDQ pin to a logic-high state and holding it high until the time from bit start to bit end is equal to $T_{(CYCH)}$ or $T_{(CYCD)}$.

The HDQ line can remain high for an indefinite period of time between each bit of address or between each bit of data on a write cycle. After the last bit of address is sent on a read cycle, the bq27010 starts outputting the data after $T_{(RSPS)}$ with timing as specified. The serial communication timing specification and illustration sections give the timings for data and break communication. Communication with the bq27010 always occurs with the least-significant bit being transmitted first.

Plugging in the battery pack can be seen as the start of a communication due to contact bounce. It is recommended that each communication or string of communications be preceded by a break to reset the HDQ engine.

Command byte

The Command byte of the bqJUNIOR consists of eight contiguous valid command bits. The command byte contains two fields: W/R Command and address. The Command byte values are shown as follows:

7	6	5	4	3	2	1	0
W/R	AD6	AD5	AD4	AD3	AD2	AD1	AD0

W/R Indicates whether the command bytes is a read or write command. A *1* indicates a write command and that the following eight bits should be written to the register specified by the address field of the Command byte, whereas a *0* indicates that the command is a read. On a read command, the bqJUNIOR outputs the requested register contents specified by the address field portion of the Command byte.

AD6-AD0 The seven bits labeled AD6—AD0 containing the address portion of the register to be accessed.

Reading 16-bit Registers

Because 16-bit values are read only 8 bits at a time with the HDQ interface, it is possible that the device can update the register value between the time the host reads the first and second bytes. To prevent any system issues, any 16-bit values read by the host should be read with the following procedure.

1. Read high byte (H0).
2. Read low byte (L0).
3. Read high byte (H1).
4. If H1=H0, then valid result is H0, L0.
5. Otherwise, read low byte (L1) and valid result is H1, L1.

This procedure assumes that the 3 or 4 reads are made more quickly than the update rate of the value. The maximum update rate of any value in the bq27010/bq27210 is 1.28 seconds.

The bq27210 circumvents this issue if a 16-bit value is read using the I^2C incremental read procedure. Both low and high bytes are captured simultaneously when the low byte is read.

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Communicating with the bq27210 (I^2C interface - Product Preview)

The bq27210 supports the standard I^2C read, incremental read, quick read, and one byte write functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively. (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop)

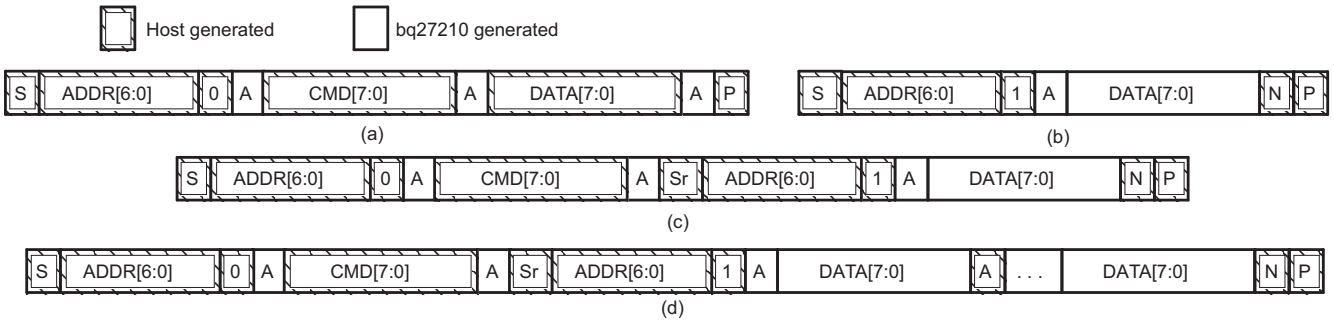
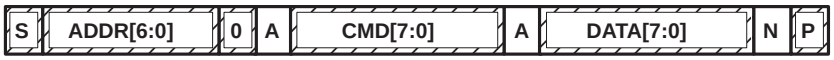


Figure 7. Supported I2C formats :
(a) 1-byte write; (b) quick read; (c) 1-byte read; (d) incremental read

The incremental read protocol is recommended for reading all 16-bit values, as this ensures that the 16-bit value is not updated during the time interval between reading the two bytes of data (see previous section on reading 16-bit values). The quick read returns data at the address indicated by the internal address pointer. The address pointer is incremented after each data byte is read or written. Reading an even address causes the communication engine to simultaneously capture the data byte from the requested even address and the data byte from the next odd address, and the address pointer is incremented twice. The data byte captured from the next odd address is output if the communication continues, without a stop, after the host acknowledges the even address byte.

Due to the memory map setup of the device, several boundary conditions must be enforced by the communication engine.

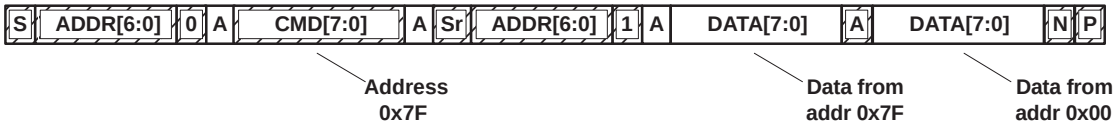
Attempt to write a read-only address (NACK after data sent by master):



Attempt to read an address above 0x7F (NACK command):

Attempt at incremental writes (NACK all extra data bytes sent):

Incremental read at the maximum allowed read address:



The I^2C engine releases both SDA and SCL if the I^2C bus is held low for $T_{(BUSERR)}$. If the bq27210 is holding the lines, releasing them frees the master to drive the lines. If an external condition is holding either of the lines low, the I^2C engine enters the low-power sleep mode if the measured charge/discharge activity level is less than the DMF threshold.

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PACKAG

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
BQ27010DRKR	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
BQ27010DRKRG4	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
BQ27210DRKR	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
BQ27210DRKRG4	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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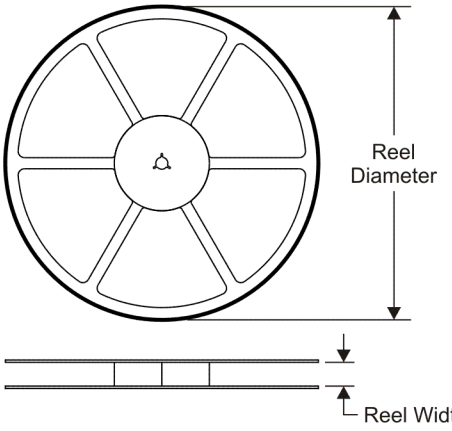
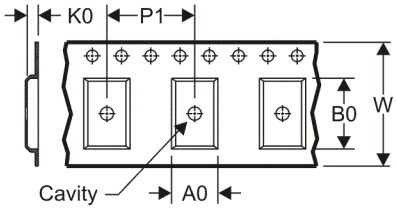
TAPE AND REEL INFORMATION

REEL DIMENSIONS

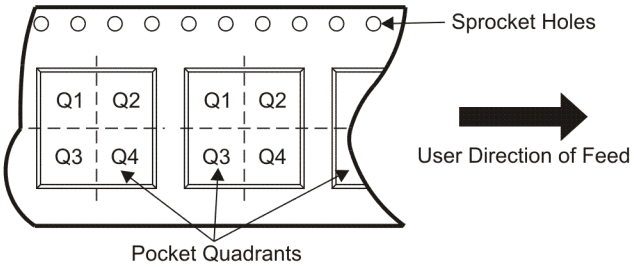


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27210DRKR	VSON	DRK	10	3000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q2

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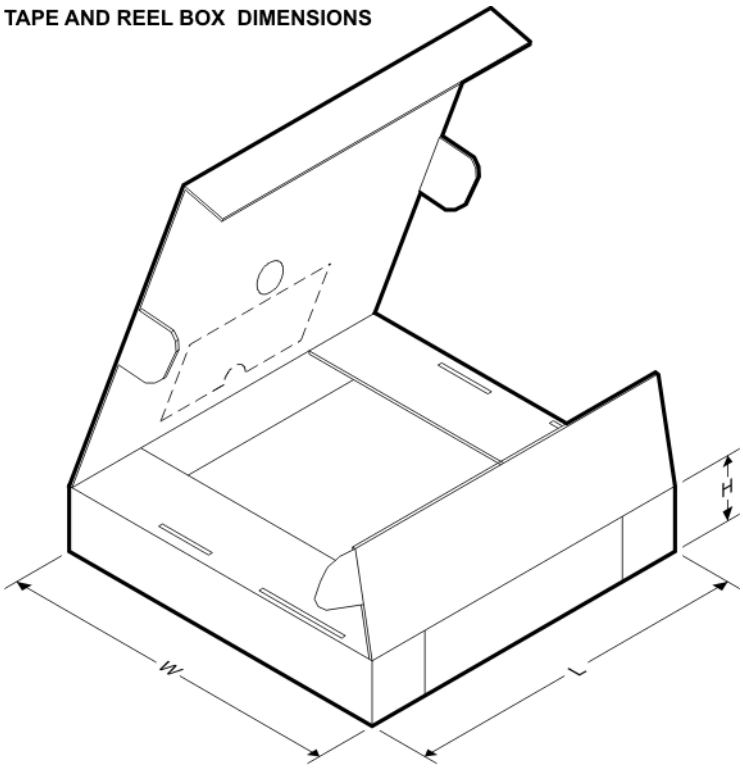
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27210DRKR	VSON	DRK	10	3000	340.5	333.0	20.6

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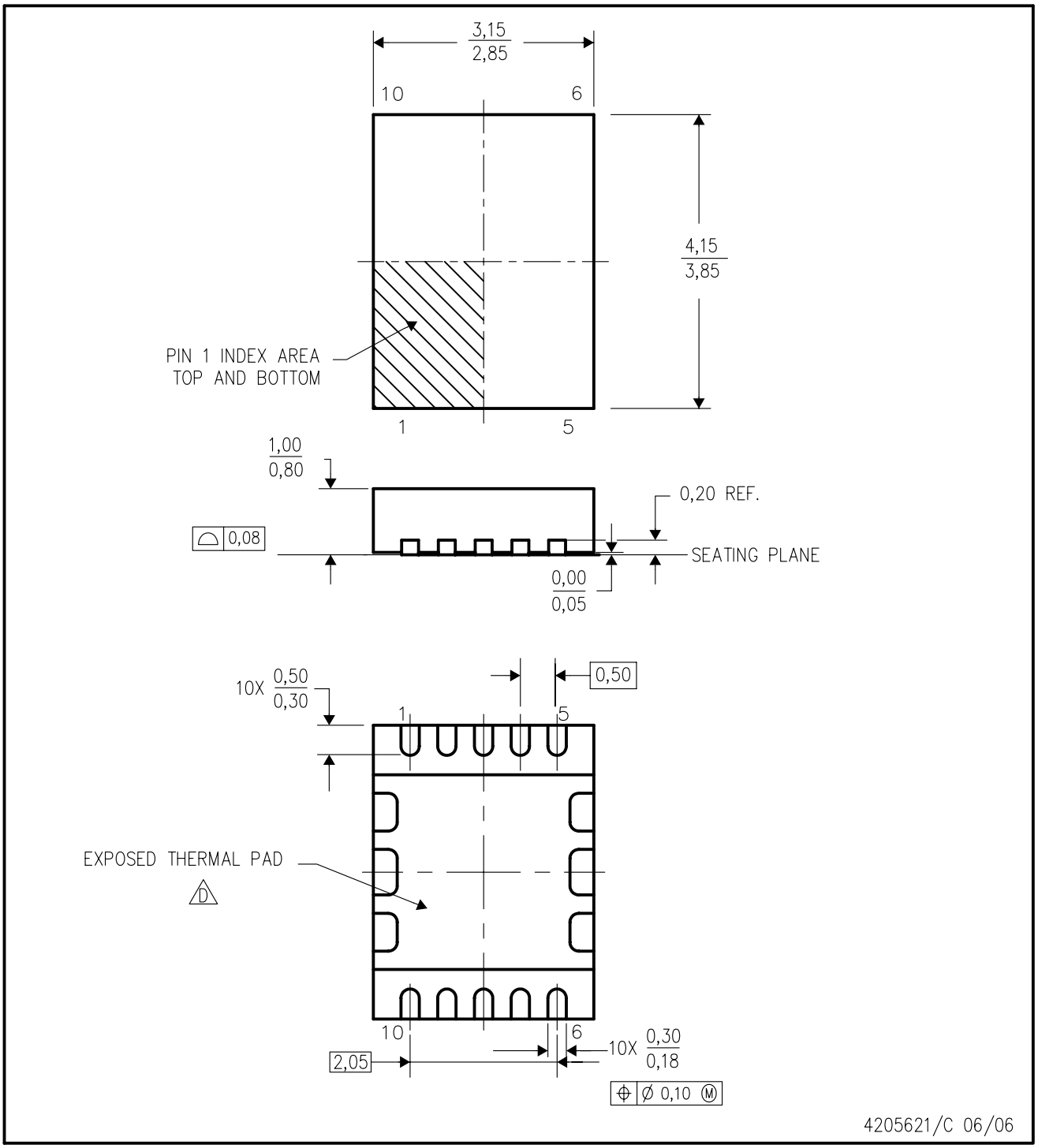
DRK (S–PDSO–N10) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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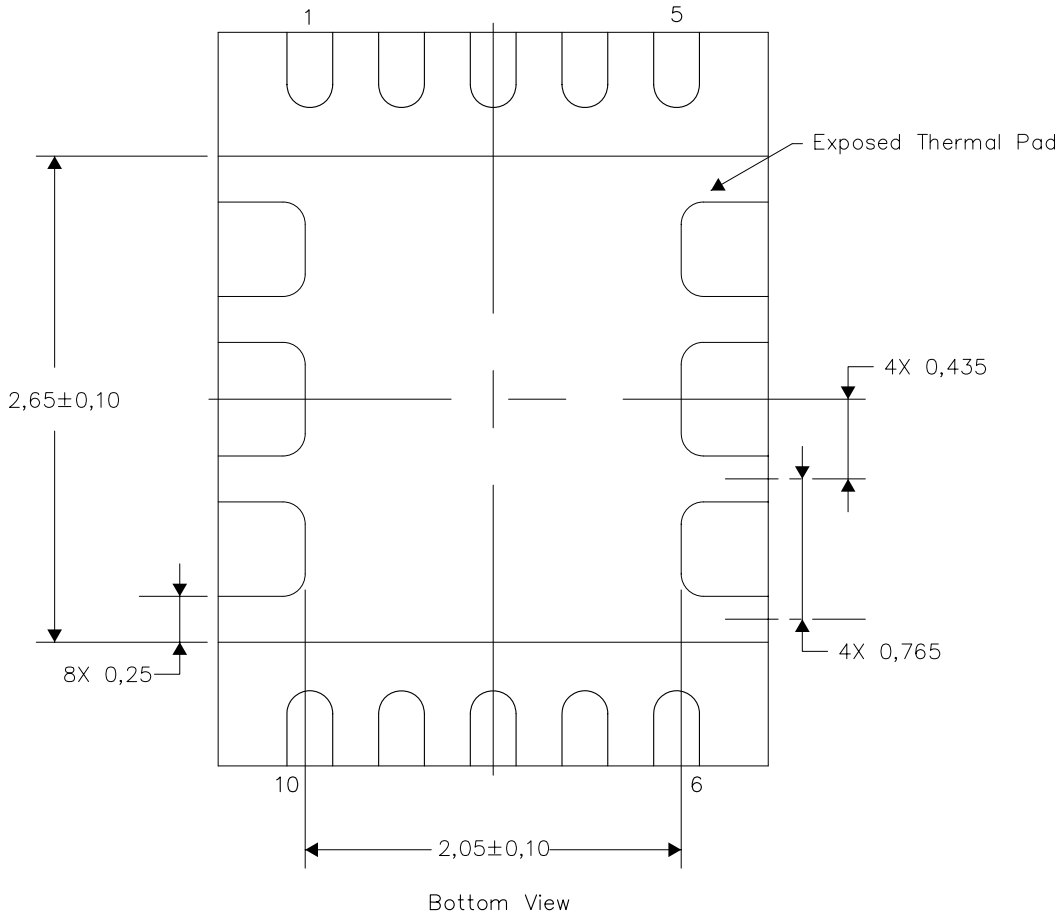
DRK (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206317/F 08/10

NOTE: A. All linear dimensions are in millimeters

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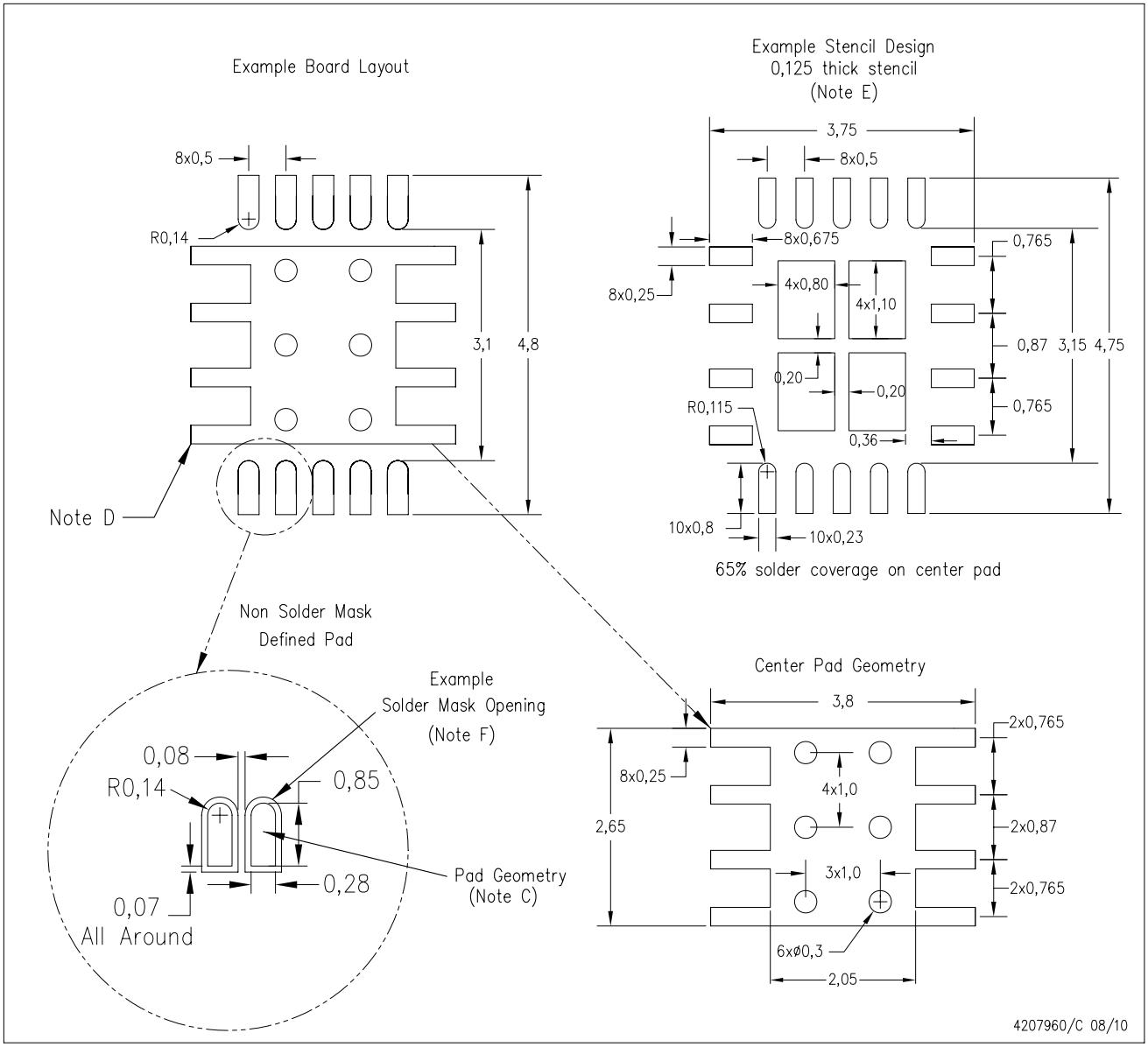
DRK (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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