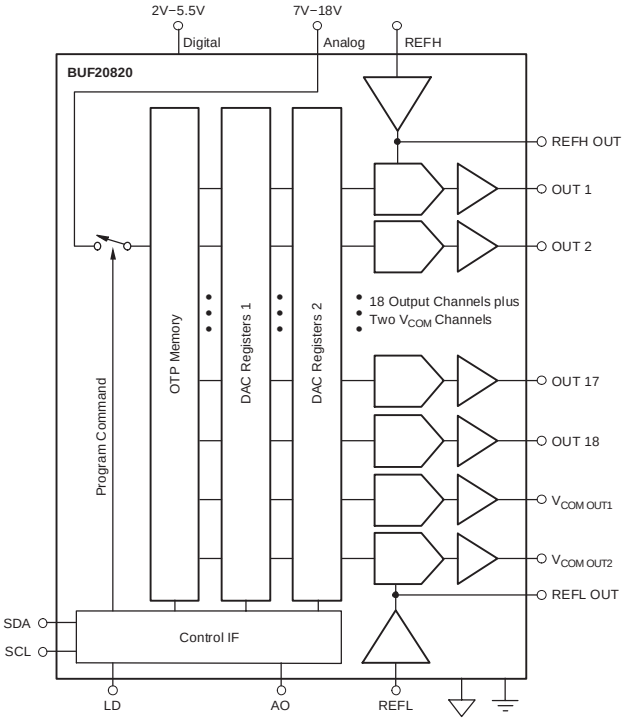
SBOS330C − DECEMBER 2005 − REVISED OCTOBER 2006

18-Channel GAMMA VOLTAGE GENERATOR with Two Programmable V_{COM} Channels

FEATURES

- 18-CHANNEL GAMMA CORRECTION
- 2-CHANNEL PROGRAMMABLE V_{COM}: 100mA I_{OUT}
- ON-CHIP OTP MEMORY
- 10-BIT RESOLUTION
- RAIL-TO-RAIL OUTPUT
- LOW SUPPLY CURRENT: 900μA/ch
- SUPPLY VOLTAGE: 7V to 18V
- DIGITAL SUPPLY: 2.0V to 5.5V
- INDUSTRY-STANDARD, TWO-WIRE INTERFACE: 3.4MHz HIGH-SPEED MODE
- HIGH ESD RATING: 4kV HBM, 1kV CDM, 200V MM
- DEMO BOARD AND SOFTWARE AVAILABLE



APPLICATIONS

- REPLACES RESISTOR-BASED GAMMA SOLUTIONS
- TFT-LCD REFERENCE DRIVERS
- DYNAMIC GAMMA CONTROL

DESCRIPTION

The BUF20820 is a programmable voltage reference generator designed for gamma correction in TFT-LCD panels. It provides 18 programmable outputs for gamma correction and two channels for V_{COM} adjustment, each with 10-bit resolution. It offers on-chip One-Time Programmable (OTP) memory that allows the user to store the gamma voltages on-chip. This eliminates the need for an external EEPROM.

This programmability replaces the traditional, time-consuming process of changing resistor values to optimize the various gamma voltages and allows designers to determine the correct gamma voltages for a panel very quickly. Required voltage changes can also be easily implemented without hardware changes.

The BUF20820 uses TI's latest, small-geometry analog CMOS process, which makes it a very competitive choice for full production, not just evaluation.

Programming of each output occurs through an industry-standard, two-wire serial interface. Unlike existing programmable buffers, the BUF20820 offers a high-speed mode that allows clock speeds up to 3.4MHz.

For lower or higher channel count, please contact your local sales or marketing representative.

The BUF20820 is available in an HTSSOP-38 PowerPAD™ package. It is specified from −40°C to +85°C.

BUF20820 RELATED PRODUCTS

FEATURES	PRODUCT
18-Channel Programmable, Two V_{COM}	BUF20800
12-Channel Programmable Buffer, 10-Bit	BUF12800
Programmable V_{COM} with Memory	BUF01900
10-Channel Gamma Correction Buffer, Int V_{COM}, 18V Operating Supply Voltage	BUF11704
High-Speed V_{COM}, 1 and 2 Channels	SN10501
Complete LCD DC/DC Solution	TPS651xx

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V_S	+19V
Supply Voltage, V_{SD}	+6V
Signal Input Terminals, SCL, SDA, AO, LD:	
Voltage	−0.5V to +6V
Current	±10mA
Output Short Circuit(2)	Continuous
Operating Temperature	−40°C to +95°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+125°C
ESD Rating:	
Human Body Model (HBM)	4kV
Charged-Device Model (CDM)	1kV
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Short-circuit to ground.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
BUF20820	HTSSOP-38	DCP	BUF20820

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = −40°C to +85°C.**

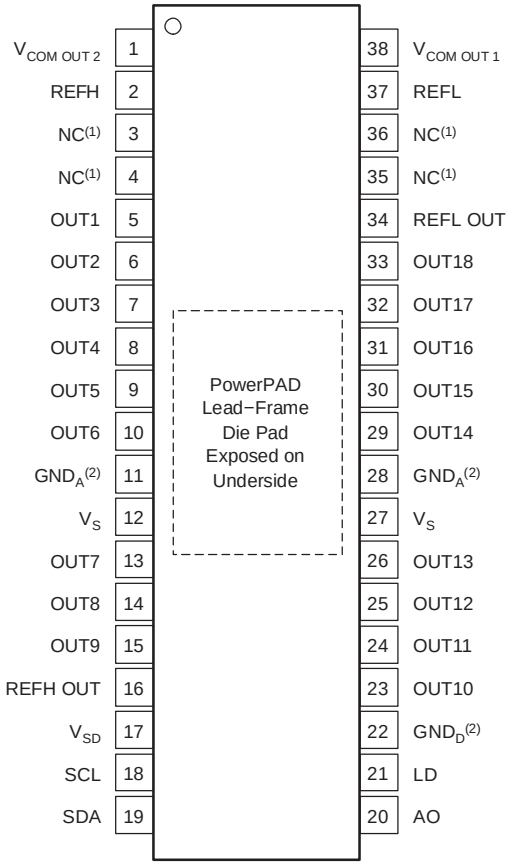
At T_A = +25°C, V_S = 18V, V_{SD} = 5V, V_{REFH} = 17V, V_{REFL} = 1V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF20820 MIN	BUF20820 TYP	BUF20820 MAX	UNIT
ANALOG						
Gamma Output Swing—High		**OUT1−9, REFH OUT, Sourcing 10mA, V_{REFH} = 17.8V, Code 1023**	**17.7**	**17.8**		**V**
		OUT10−18, REFL OUT, Sourcing 10mA, V_{REFH} = 17.8V, Code 1023	**17.0**	**17.2**		**V**
Gamma Output Swing—Low		**OUT1−9, REFH OUT, Sinking 10mA, V_{REFL} = 0.2V, Code 00**		**0.6**	**1.0**	**V**
		OUT10−18, REFL OUT, Sinking 10mA, V_{REFL} = 0.2V, Code 00		**0.2**	**0.3**	**V**
V_{COM} Buffer Output Swing—High		**V_{COM}, Sourcing 100mA, V_{REFH} = 17.8V**	**13**	**15.5**		**V**
V_{COM} Buffer Output Swing—Low		**V_{COM}, Sinking 100mA, V_{REFL} = 0.2V**		**1**	**2.0**	**V**
Output Current			See Typical Characteristics Curve			
REFH Input Range(1)			4		V_S	V
REFL Input Range(1)			GND		V_S − 4	V
Integral Nonlinearity	INL	No Load, V_{REFH} = 17V, V_{REFL} = 1V		0.3	1.5	Bits
Differential Nonlinearity	DNL	No Load, V_{REFH} = 17V, V_{REFL} = 1V		0.3	1	Bits
Gain Error				0.12		%
Program to Out Delay	t_D			5		µs
Output Accuracy		No Load, V_{REFH} = 17V, V_{REFL} = 1V		±20	±50	mV
over Temperature				**±25**		**mV**
Input Resistance at V_{REFH} and V_{REFL}	R_{INH}			100		MΩ
Load Regulation, All References	REG	V_{OUT} = V_S/2, I_{OUT} = +5mA to −5mA Step		0.5	1.5	mV/mA
40mA, All Channels		V_{OUT} = V_S/2, $I_{SINKING}$ = 40mA, $I_{SOURCING}$ = 40mA		0.5	1.5	mV/mA
ANALOG POWER SUPPLY						
Operating Range(2)	V_S		7		18	V
Total Analog Supply Current	I_S	No Load		18	28	mA
over Temperature					**28**	**mA**
DIGITAL						
Logic 1 Input Voltage	V_{IH}		0.7 × V_{SD}			V
Logic 0 Input Voltage	V_{IL}				0.3 × V_{SD}	V
Logic 0 Output Voltage	V_{OL}	I_{SINK} = 3mA		0.15	0.4	V
Input Leakage				±0.01	±10	µA
Clock Frequency	**f_{CLK}**	**Standard/Fast Mode**			**400**	**kHz**
		High-Speed Mode			**3.4**	**MHz**
DIGITAL POWER SUPPLY						
Operating Voltage Range	V_{SD}		2.0		5.5	V
Digital Supply Current(3)	I_{SD}	No-Load, Two-Wire Bus Inactive		25	50	µA
over Temperature				**100**		**µA**
TEMPERATURE						
Specified Temperature Range			−40		+85	°C
Operating Temperature Range		Junction Temperature < 125°C	−40		+95	°C
Storage Temperature Range			−65		+150	°C
Thermal Resistance, HTSSOP-38						
Junction-to-Ambient	θ_{JA}			30		°C/W
Junction-to-Case	θ_{JC}			15		°C/W

(1) See Applications Information section *REFH and REFL Input Range*.
(2) Minimum analog supply voltage is 8.5V when programming OTP memory.
(3) See typical characteristic curve, *Digital Supply Current vs Two-Wire Bus Activity*.

PIN CONFIGURATIONS

Top View **HTSSOP**



(1) NC denotes no connection.
(2) GND_D and GND_A are internally connected and must be at the same voltage potential.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = 18V, V_{SD} = 5V, V_{REFH} = 17V, V_{REFL} = 1V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

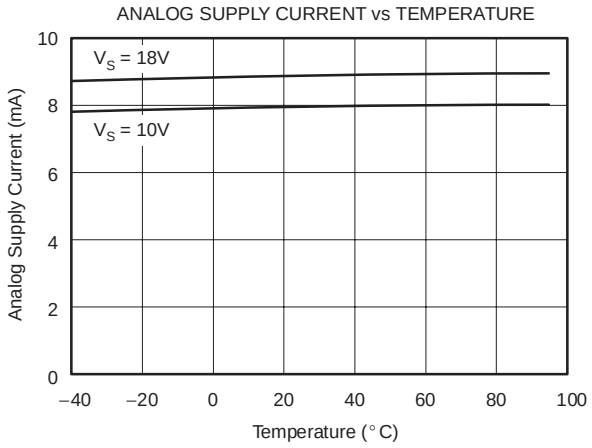


Figure 1

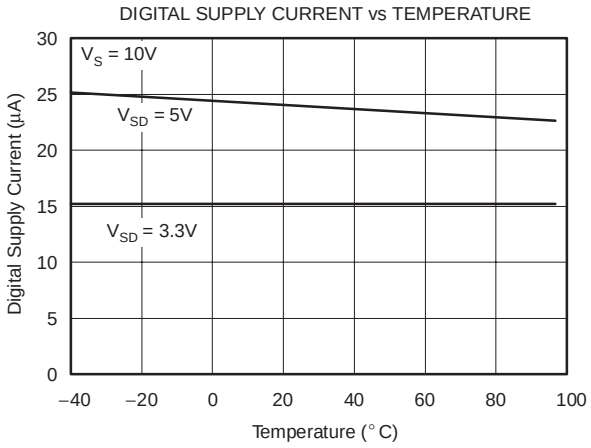


Figure 2

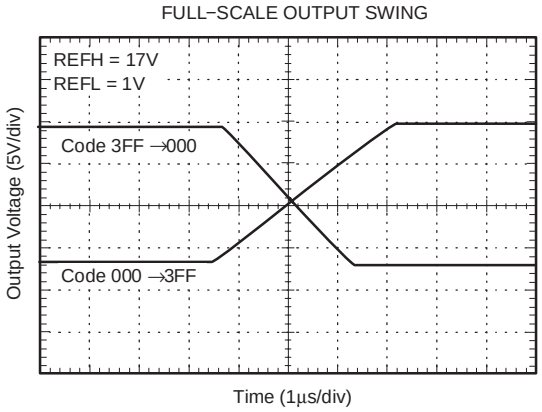


Figure 3

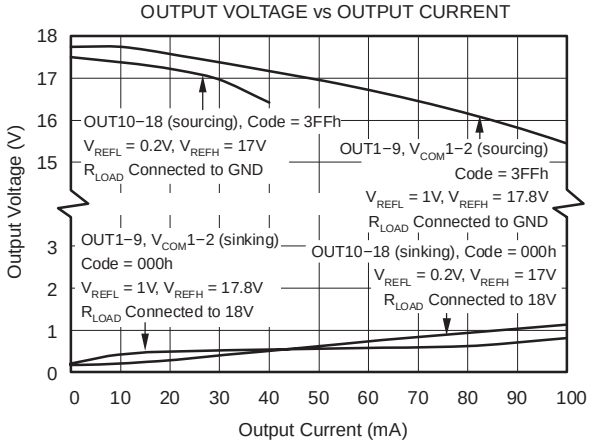


Figure 4

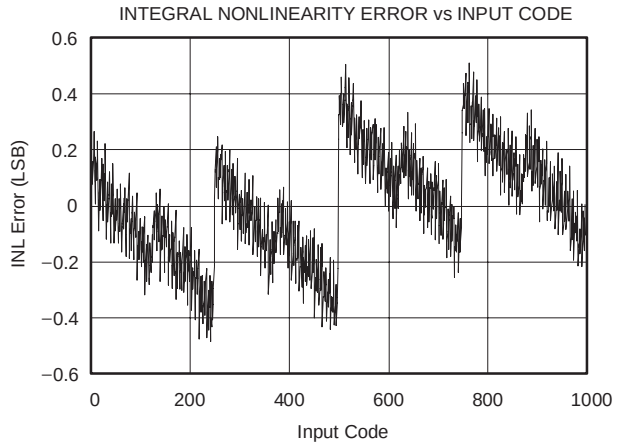


Figure 5

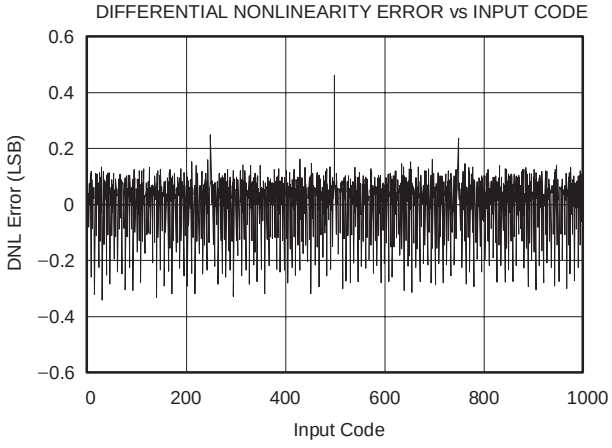


Figure 6

APPLICATIONS INFORMATION

The BUF20820 programmable voltage reference allows fast and easy adjustment of 18 programmable reference outputs and two channels for V_{COM} adjustment, each with 10-bit resolution. It allows very simple, time-efficient adjustment of the gamma reference and V_{COM} voltages. The BUF20820 is programmed through a high-speed, standard, two-wire interface. The BUF20820 features a double-register structure for each DAC channel to simplify the implementation of dynamic gamma control. This design allows pre-loading of register data and rapid updating of all channels simultaneously.

Buffers 1−9 are able to swing to within 200mV of the positive supply rail, and to within 0.6V of the negative supply rail. Buffers 10−18 are able to swing to within 0.8V of the positive supply rail and to within 200mV of the negative supply rail.

The BUF20820 can be powered using an analog supply voltage from 7V to 18V, and a digital supply from 2V to 5.5V. The digital supply must be applied prior to or simultaneously with the analog supply to avoid excessive current and power consumption; damage to the device may occur if it is left connected only to the analog supply for extended periods of time. Figure 7 shows the power supply timing requirements.

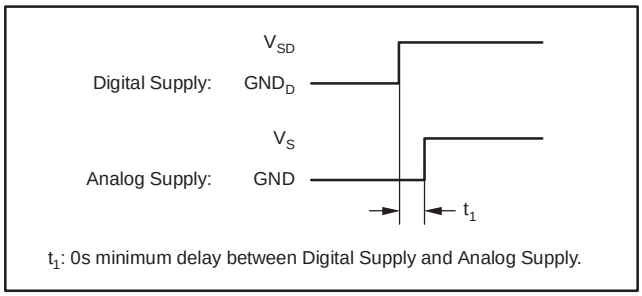


Figure 7. Power Supply Timing Requirements

Figure 8 shows the BUF20820 in a typical configuration. In this configuration, the BUF20820 device address is 74h. The output of each digital-to-analog converter (DAC) is immediately updated as soon as data is received in the corresponding register (LD = 0). For maximum dynamic range, set $V_{REFH} = V_S - 0.2V$ and $V_{REFL} = GND + 0.2V$.

TWO-WIRE BUS OVERVIEW

The BUF20820 communicates through an industry-standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the 9th clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent followed by an Acknowledge Bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH will be interpreted as a START or STOP condition.

Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

The BUF20820 can act only as a slave device; therefore, it never drives SCL. SCL is only an input for the BUF20820. Table 1 and Table 2 summarize the address and command codes, respectively, for the BUF20820.

ADDRESSING THE BUF20820

The address of the BUF20820 is 111010x, where *x* is the state of the A0 pin. When the A0 pin is LOW, the device will acknowledge on address 74h (1110100). If the A0 pin is HIGH, the device will acknowledge on address 75h (1110101).

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. Quick-Reference Table of BUF20820 Addresses

DEVICE/COMPONENT	ADDRESS
BUF20820 Address:	
A0 pin is LOW (device will acknowledge on address 74h)	1110100
A0 pin is HIGH (device will acknowledge on address 75h)	1110101

Table 2. Quick-Reference Table of Command Codes

COMMAND	CODE
General Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

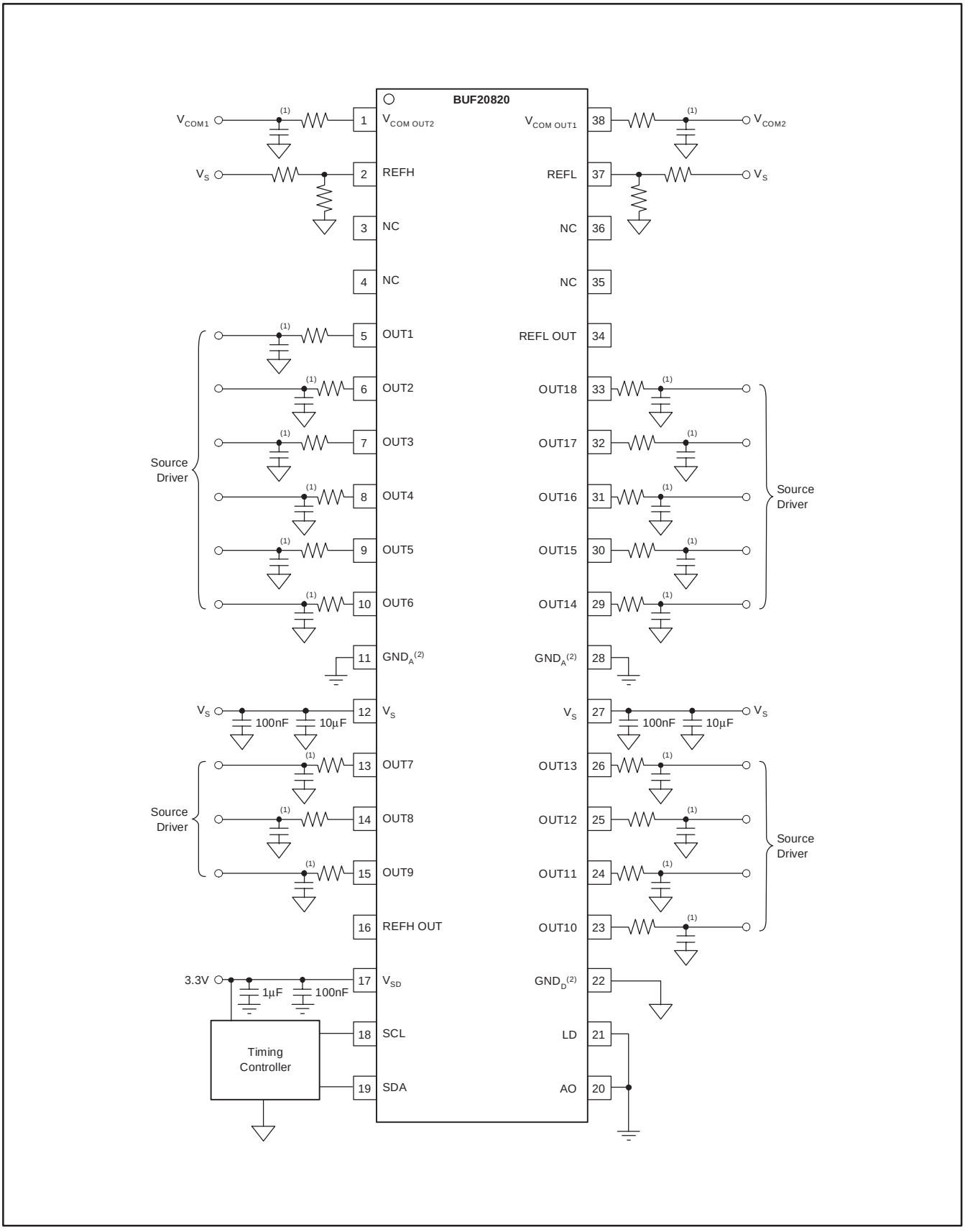


Figure 8. Typical Application Configuration

DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (or Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF20820 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001xxx, with SCL = 400kHz, following the START condition; *xxx* are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. (Note that this is different from normal address bytes—the low bit does not indicate read/write status.) The BUF20820 will respond to the High-speed command regardless of the value of these last three bits. The BUF20820 will not acknowledge this byte; the communication protocol prohibits acknowledgement of the Hs master code. On receiving a master code, the BUF20820 will switch on its Hs mode filters, and communicate at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF20820 will switch out of Hs mode with the next STOP condition.

GENERAL CALL RESET AND POWER-UP

The BUF20820 responds to a General Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF20820 acknowledges both bytes. Upon receiving a General Call Reset, the BUF20820 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General Call address byte of 00h (0000 0000), but does not acknowledge any General Call data bytes other than 06h (0000 0110).

The BUF20820 automatically performs a reset upon power-up. As part of the reset, the BUF20820 is configured for all outputs to change to the programmed OTP memory values, or (V_{REFH} − V_{REFL})/2 if the OTP values have not been programmed.

The BUF20820 resets all outputs to the OTP memory values (or to (V_{REFH} − V_{REFL})/2 if the OTP values have not been programmed) when the device address is sent, followed by a valid DAC address with bits D7 to D5 set to '100'. If these bits are set to '010', only the DAC being addressed will be reset.

OUTPUT VOLTAGE

Buffer output values are determined by the reference voltages (V_{REFH} and V_{REFL}) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = \left[\frac{V_{REFH} - V_{REFL}}{1024} \times \text{Decimal Value of Code}\right] + V_{REFL} \quad (1)$$

The valid voltage ranges for the reference voltages are:

$$4V \le V_{REFH} \le V_S - 0.2V \text{ and } 0.2V \le V_{REFL} \le V_S - 4V \quad (2)$$

The BUF20820 outputs are capable of a full-scale voltage output change in typically 5µs—no intermediate steps are required.

OUTPUT LATCH

Updating the DAC register is not the same as updating the DAC output voltage, because the BUF20820 features a double-buffered register structure. There are three methods for latching transferred data from the storage registers into the DACs to update the DAC output voltages.

Method 1 requires externally setting the latch pin (LD) LOW, LD = LOW, which will update each DAC output voltage whenever its corresponding register is updated.

Method 2 externally sets LD = HIGH to allow all DAC output voltages to retain their values during data transfer and until LD = LOW, which will then simultaneously update the output voltages of all DACs to the new register values. Use this method to transfer a future data set in advance to prepare for a very fast output voltage update.

Method 3 uses software control. LD is maintained HIGH, and all DACs are updated when the master writes a 1 in bit 15 and a 0 in bit 14 of any DAC register. The update will occur after receiving the 16-bit data for the currently-written register.

The General Call Reset and the power-up reset will update the DAC regardless of the state of the latch pin.

ACQUIRE OF OTP MEMORY

A general acquire command will update all registers and DAC outputs to the values stored in OTP memory.

A single channel acquire command will update only the register and DAC output of the DAC corresponding to the DAC address used in the command.

General Acquire Command

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send a DAC address byte. Bits D7−D5 must be set to 100. Bits D4−D0 are any valid DAC address. Only addresses 00000 to 10100 are valid and will be acknowledged. Table 3 shows the valid addresses.
4. Send a STOP condition on the bus.

Following this command, all DAC registers and DAC outputs will change to the OTP memory values.

Table 3. DAC Addresses

DAC	ADDRESS
DAC_1	0 0000
DAC_2	0 0001
DAC_3	0 0010
DAC_4	0 0011
DAC_5	0 0100
DAC_6	0 0101
DAC_7	0 0110
DAC_8	0 0111
DAC_9	0 1000
DAC_10	0 1001
DAC_11	0 1010
DAC_12	0 1011
DAC_13	0 1100
DAC_14	0 1101
DAC_15	0 1110
DAC_16	0 1111
DAC_17	1 0000
DAC_18	1 0001
$V_{COM\ OUT1}$	1 0010
$V_{COM\ OUT2}$	1 0011
Write Disable Bit	1 0100

Single Channel Acquire Command

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send a DAC address byte using the DAC address corresponding to the DAC output and register to update with the OTP memory value. Bits D7−D5 must be set to 010. Bits D4−D0 are the DAC address. Only DAC addresses 00000 to 10100 are valid and will be acknowledged. Table 3 shows the valid addresses.
4. Send a STOP condition on the bus.

See Figure 9 for the timing diagrams for the acquire commands.

READ/WRITE OPERATIONS

Single or multiple read and write operations can be done in a single communication transaction. Writing to a DAC register differs from writing to the OTP memory. Bits D15−D14 of the most significant byte of data will determine if data will be written to the DAC register or the OTP memory. See Figure 10 through Figure 12 for the timing diagrams and timing requirements for the read/write commands.

Read/Write: DAC register

The BUF20820 is able to read from a single DAC, or multiple DACs, or write to the register of a single DAC, or multiple DACs in a single communication transaction. DAC addresses begin with 00000, which corresponds to DAC_1, through 10011, which corresponds to $V_{COM\ OUT2}$.

Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH will perform a read transaction.

Writing:

To write to a single DAC register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send a DAC or write disable bit address byte. Bits D7−D5 must be set to 0. Bits D4−D0 are the DAC address. Only addresses 00000 to 10100 are valid and will be acknowledged. Table 3 shows valid addresses.
4. Send two bytes of data for the specified DAC register. Begin by sending the most significant byte first (bits D15−D8, of which only bits D9 and D8 are used, and bits D15−D14 must not be 01), followed by the least significant byte (bits D7−D0). For address 10100, only D0 has meaning. This bit is the write disable bit. The register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF20820 will acknowledge each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register will not be updated. Updating the DAC register is not the same as updating the DAC output voltage. See the *Output Latch* section.

The process of updating multiple DAC registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the

addressed register, the master continues to send data for the next register. The BUF20820 automatically and sequentially steps through subsequent registers as additional data is sent. The process continues until all desired registers have been updated or a STOP condition is sent.

To write to multiple DAC registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the first DAC, or send the address byte for whichever DAC will be the first in the sequence of DACs to be updated. The BUF20820 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning, and bits D15−D14 must not be 01), followed by the least significant byte (bits D7−D0). The first two bytes are for the DAC addressed in step 3 above. Its register is automatically updated after receiving the second byte. The next two bytes are for the following DAC. That DAC register is updated after receiving the fourth byte. This process continues until the registers of all following DACs have been updated. The last address, 10100, is the address of the write disable bit and cannot be accessed using this method. It must be written using the *write to a single DAC register* procedure.
5. Send a STOP condition on the bus.

The BUF20820 will acknowledge each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data will be updated.

Reading:

Reading a DAC register will return the data stored in the DAC. This data can differ from the data stored in the DAC register. See the *Output Latch* section.

To read the DAC value:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send the DAC address byte. Bits D7−D5 must be set to 0; Bits D4−D0 are the DAC address. Only DAC addresses 00000 to 10100 are valid and will be acknowledged. For address 10100, only D0 has meaning. This bit is the write disable bit.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF20820 will acknowledge this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, only bits D9 and D8 have meaning), the next byte is the least significant byte (bits D7−D0).
7. Acknowledge after receiving the first byte.
8. Do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

To Read Multiple DACs:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the first DAC, or send the address byte for whichever DAC will be the first in the sequence of DACs to be read. The BUF20820 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF20820 will acknowledge this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, only bits D9 and D8 have meaning), the next byte is the least significant byte (bits D7−D0).
7. Acknowledge after receiving each byte of data except for the last byte. The acknowledge bit of the last byte should be HIGH to end the read operation.
8. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

Write: OTP Memory for the DAC Register

The BUF20820 is able to write to the OTP memory of a single DAC, or multiple DACs in a single communication transaction. DAC addresses begin with 00000 (which corresponds to DAC_1) through 10011 (which corresponds to $V_{COM\ OUT2}$).

When programming the OTP memory, the analog supply voltage must be between 8.5V and 18V.

Write commands are performed by setting the read/write bit LOW.

To write to a single OTP register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send a DAC address byte. Bits D7−D5 must be set to 0. Bits D4−D0 are the DAC address. Only DAC addresses 00000 to 10100 are valid and will be acknowledged. See Table 3 for DAC addresses.
4. Send two bytes of data for the OTP register of the specified DAC. Begin by sending the most significant byte first (bits D15−D8, of which only bits D9 and D8 are data bits, and bits D15−D14 must be 01), followed by the least significant byte (bits D7−D0). For address 10100, only D0 has meaning. This bit is the write disable bit. The register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF20820 will acknowledge each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified OTP register will not be updated. Writing an OTP register will also update the DAC register and output voltage.

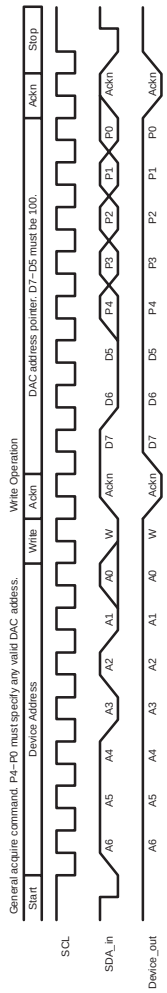
To write to multiple OTP registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF20820 will acknowledge this byte.
3. Send either the DAC_1 address byte to start at the OTP register of the first DAC, or send the address byte for whichever DAC will be the first in the sequence to be updated. The BUF20820 will begin with the OTP register of this DAC and step through subsequent registers in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning, and bits D15−D14 must be 01), followed by the least significant byte (bits D7−D0). The first two bytes are for the OTP register of the DAC addressed in step 3 above. This OTP register is automatically updated after receiving the second byte. The next two bytes are for the OTP register of the following DAC (bits D15−D14 must again be 01). That DAC OTP register is updated after receiving the fourth byte. This process continues until the registers of all following DAC OTP registers have been updated. The last address, 10100, is the address of the write disable bit and cannot be accessed using this method. It must be written using the *write to a single OTP register* procedure.
5. Send a STOP condition on the bus.

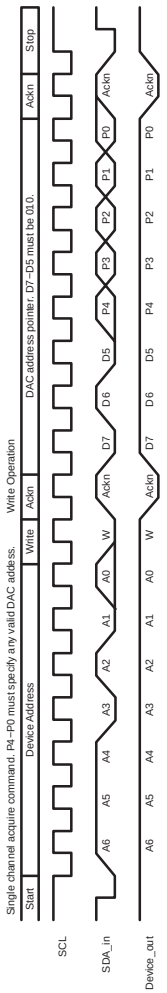
The BUF20820 will acknowledge each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data will be programmed.

OTP WRITE DISABLE

Writing a ‘1’ in bit D0 of register 10100 disables all future writes. The state of this bit can be accessed the same as any other data bit. It is important to set this bit to 1 after the OTP registers have been programmed to prevent accidental changes to the OTP registers. Until bit D0 of register 10100 is set to 1, any OTP register bit can be changed from 0 to 1; however, once a bit is set to a 1, it cannot be set back to 0.



a) General Acquire



b) Single-Channel Acquire

Figure 9. Timing Diagram for Acquire Operation

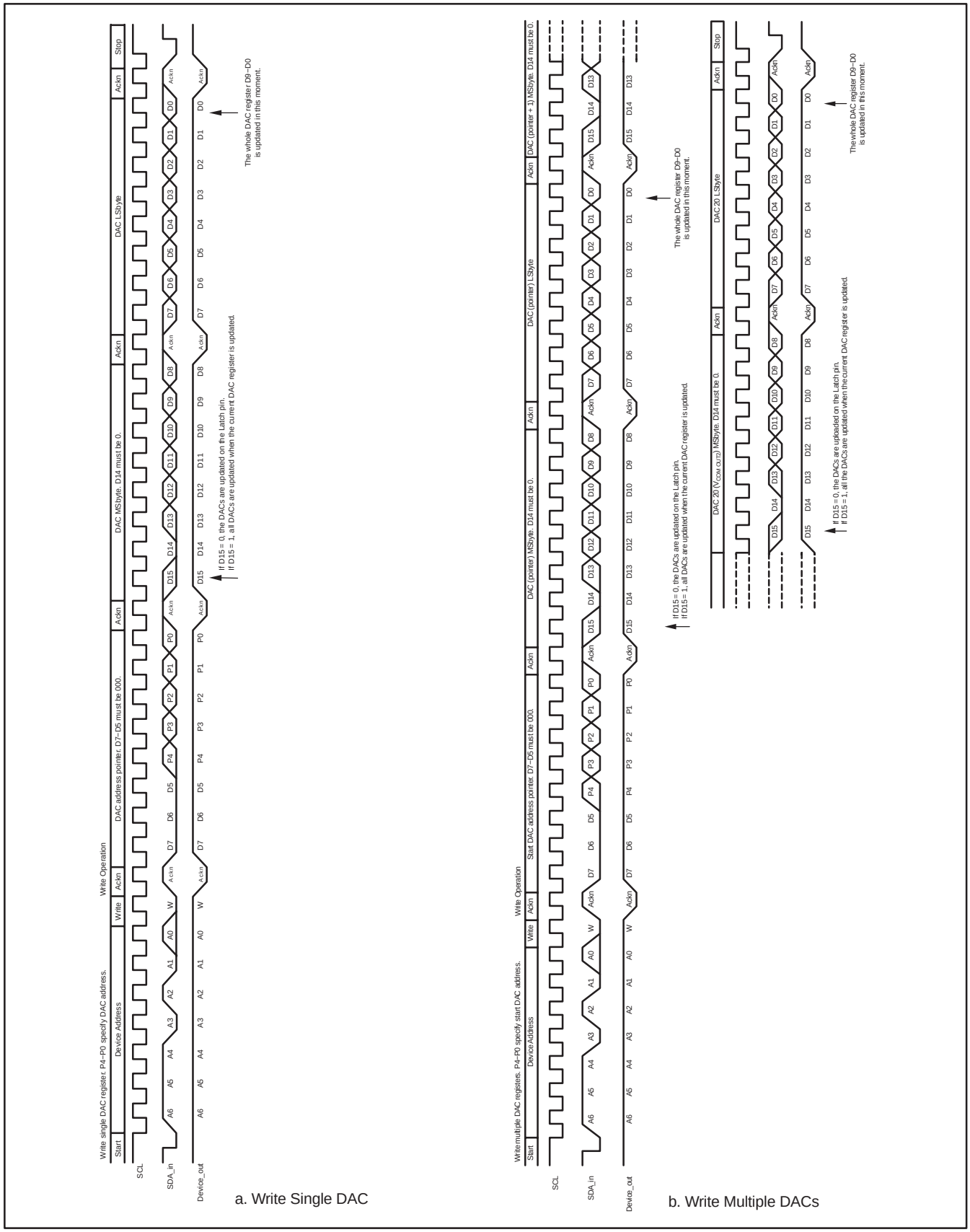


Figure 10. Timing Diagram for Write DAC Register

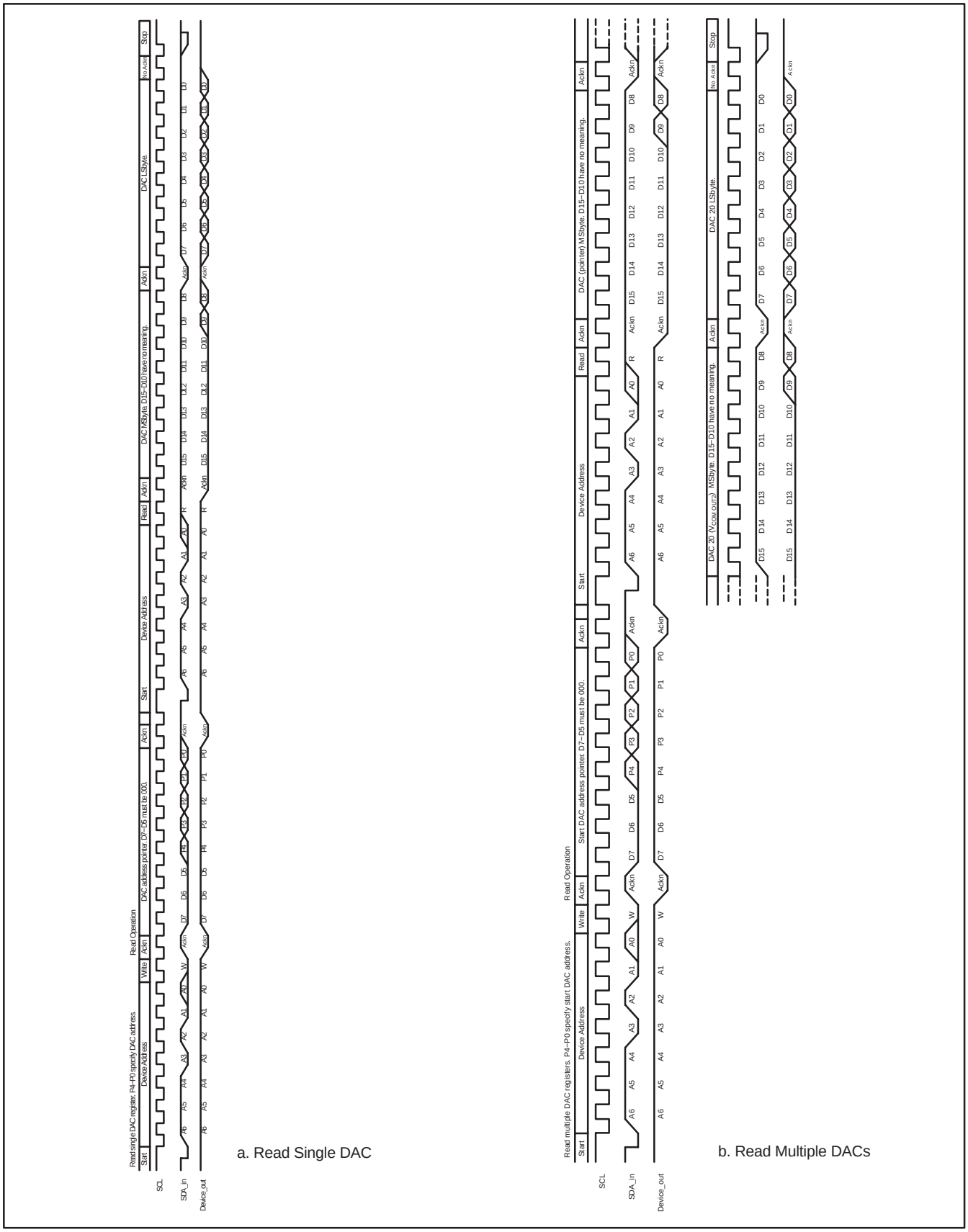


Figure 11. Timing Diagram for Read DAC Register

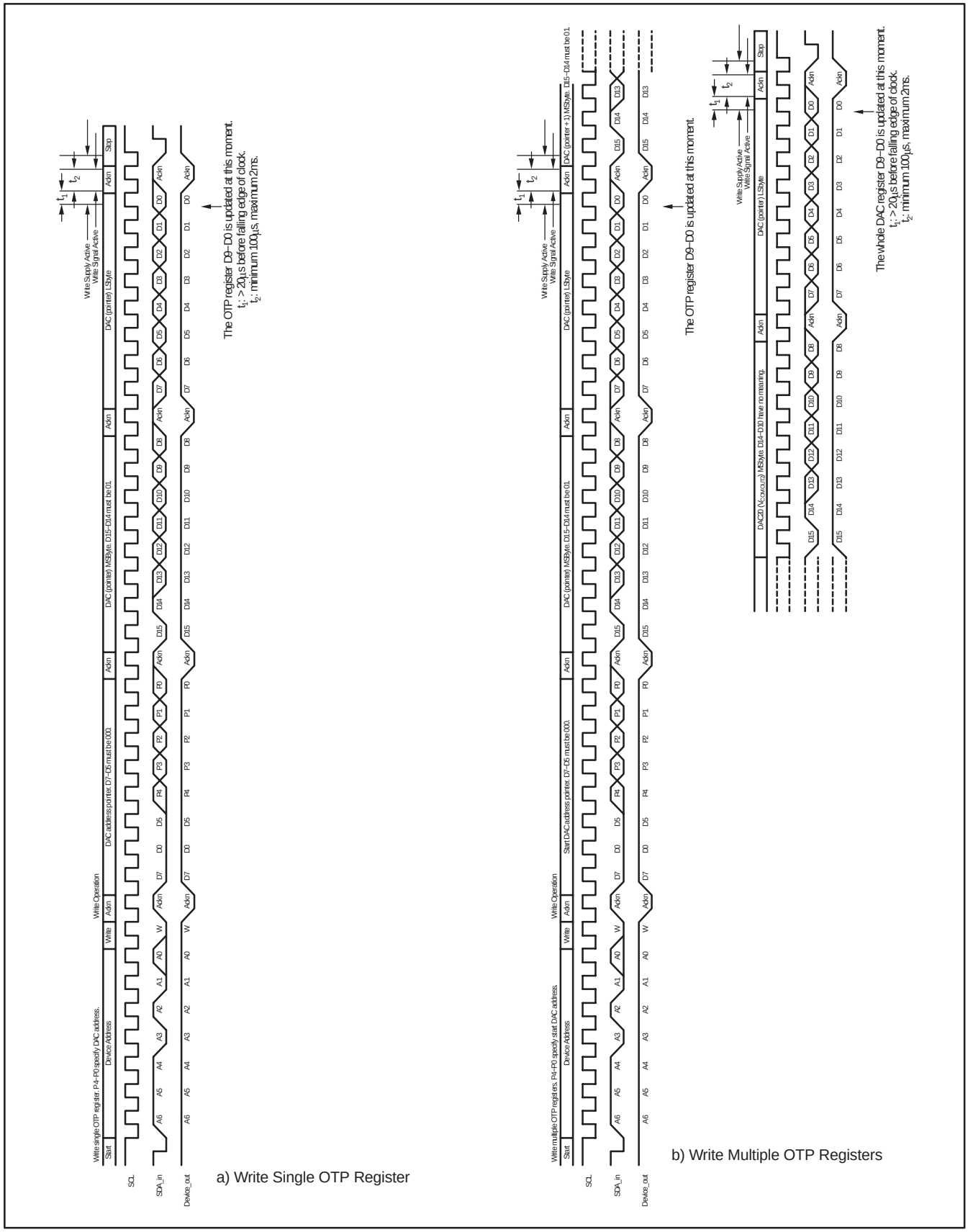


Figure 12. Timing Diagram for Write OTP Register

REPLACEMENT OF TRADITIONAL GAMMA BUFFER

Traditional gamma buffers rely on a resistor string (often using expensive 0.1% resistors) to set the gamma voltages. During development, the optimization of these gamma voltages can be time consuming. Programming these gamma voltages with the BUF20820 can significantly reduce the time required for gamma voltage optimization. The final gamma values can be written into the internal OTP memory to replace a traditional gamma buffer solution. Figure 13a shows the traditional resistor string; Figure 13b shows the more efficient alternative method using the BUF20820.

The BUF20820 uses the most advanced high-voltage CMOS process available today, which allows it to be competitive with traditional gamma buffers.

Programmability offers the following advantages:

- It shortens development time significantly.
- It eliminates manufacturing variance between panels.
- It allows a single panel to be built for multiple customers, with loading of customer-dependent gamma curves during final production. This significantly lowers inventory cost and risk and simplifies inventory management.
- It allows demonstration of various gamma curves to LCD monitor makers by simply uploading a different set of gamma values.
- It provides a simple means of adjusting gamma curves during final production improve picture quality and accommodate changes in the panel manufacturing process or end-customer requirements.
- It decreases cost and space.

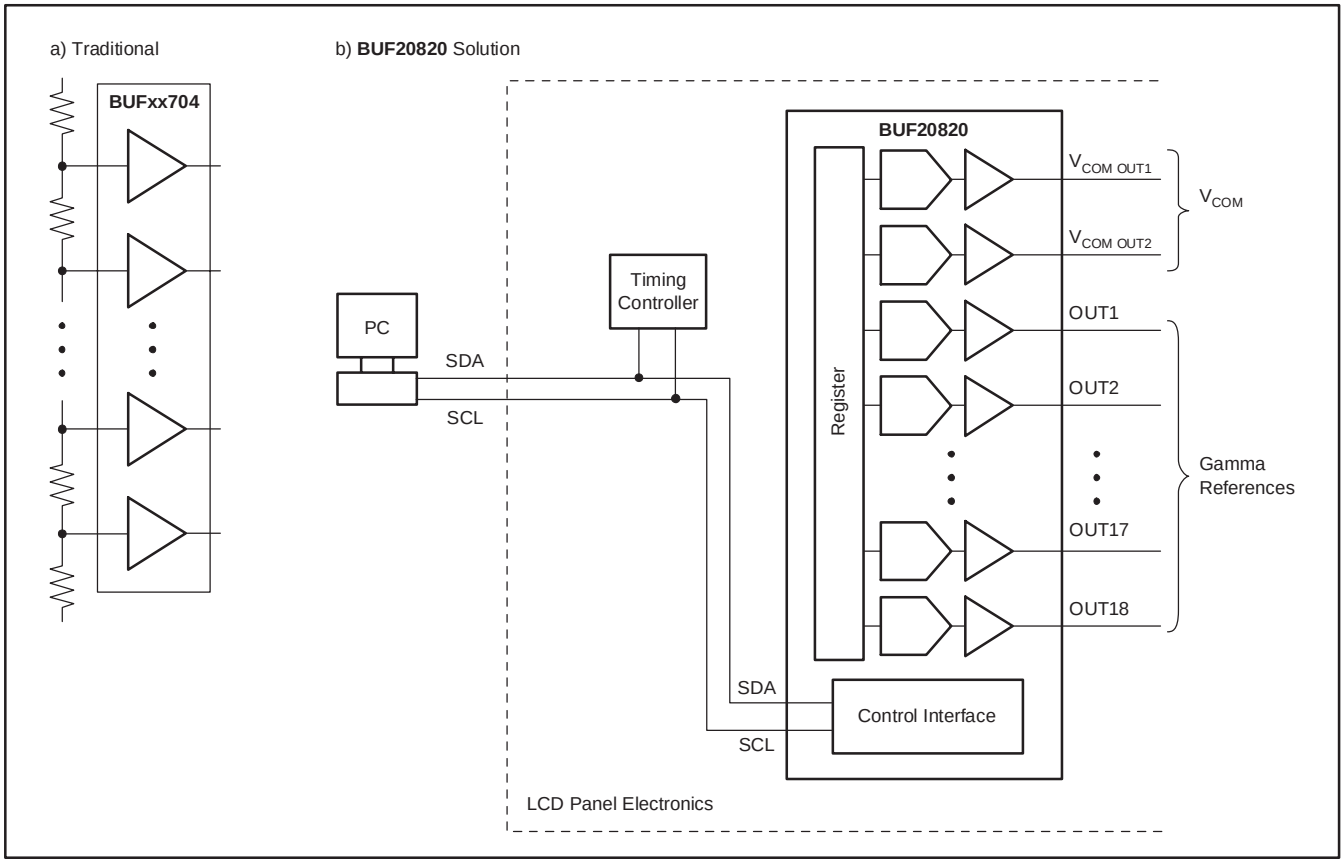


Figure 13. Replacement of the Traditional Gamma Buffer

PROGRAMMABLE V_{COM}

The V_{COM} channels of the BUF20820 can swing to 2.5V from the positive supply rail while sourcing 100mA, and to 1V above the negative rail while sinking 100mA (see Figure 4, typical characteristic *Output Voltage vs Output Current*). The gamma and the V_{COM} values can be permanently stored in the internal OTP memory. The V_{COM} channels can be programmed independently from the gamma channels. Figure 14 shows the BUF20820 being used for V_{COM} voltages.

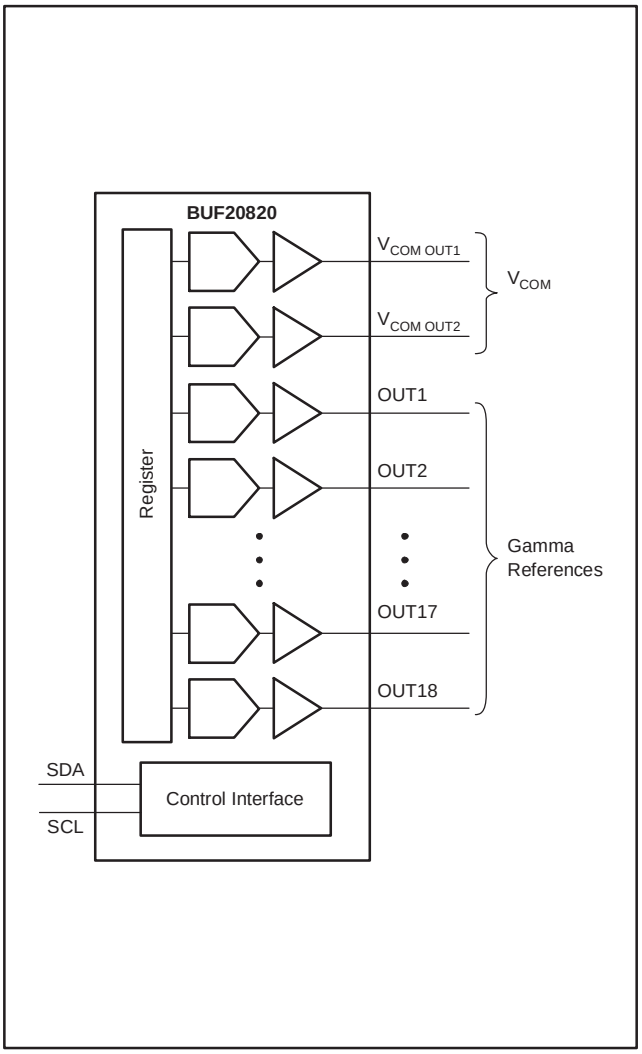


Figure 14. BUF20820 Used for Programmable V_{COM}

REFH AND REFL INPUT RANGE

Best performance and output swing range of the BUF20820 are achieved by applying REFH and REFL voltages that are slightly below the power-supply voltages. Most specifications have been tested at REFH = V_S − 200mV and REFL = GND + 200mV. The REFH internal buffer is designed to swing very closely to V_S and the REFL internal buffer to GND. However, there is a finite limit on how close they can swing before saturating. To avoid saturation of the internal REFH and REFL buffers, the REFH voltage should not be greater than V_S −100mV and REFL voltage should not be lower than GND + 100mV. Figure 15 shows the swing capability of the REFH and REFL buffers.

The other consideration when trying to maximize the output swing capability of the gamma buffers is the limitation in the swing range of output buffers (OUT1−18, $V_{COM}1$, and $V_{COM}2$), which depends on the load current. A typical load in the LCD application is 5−10mA. For example, if OUT1 is sourcing 10mA, the swing is typically limited to about V_S − 200mV. The same applies to OUT18, which typically limits at GND + 200mV when sinking 10mA. An increase in output swing can only be achieved for much lighter loads. For example, a 3mA load typically allows the swing to be increased to approximately V_S − 100mV and GND + 100mV.

Connecting REFH directly to V_S and REFL directly to GND does not damage the BUF20820. As discussed above however, the output stages of the REFH and REFL buffers will saturate. This condition is not desirable and can result in a small error in the measured output voltages of OUT1−18, $V_{COM\,OUT1}$, and $V_{COM\,OUT2}$. As described above, this method of connecting REFH and REFL does not help to maximize the output swing capability.

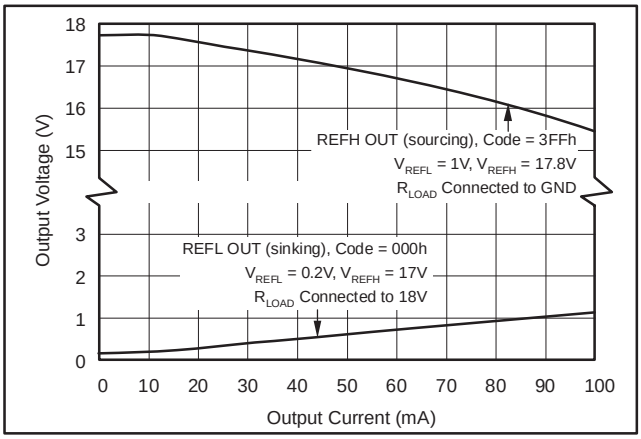


Figure 15. Reference Buffer Output Voltage vs Output Current

CONFIGURATION FOR 20 GAMMA CHANNELS

The V_{COM} outputs can be used as additional gamma references in order to achieve two additional gamma channels (20 total). The V_{COM} outputs will behave the same as the OUT1−9 outputs when sourcing or sinking smaller currents (see the Typical Characteristics, Figure 4). The V_{COM} outputs are better able to swing to the positive rail than to the negative rail. Therefore, it is better to use the V_{COM} outputs for higher reference voltages; see Figure 16.

CONFIGURATION FOR 22 GAMMA CHANNELS

In addition to the V_{COM} outputs, the REFH and REFL OUT outputs can also be used as fixed gamma references. The output voltage will be set by the REFH and REFL input voltages, respectively. Therefore, REFH OUT should be used for the highest voltage gamma reference, and REFL OUT for the lowest voltage gamma reference. A 22-channel solution can be created by using all 18 outputs, the two V_{COM} outputs, and both REFH/L OUT outputs for gamma references—see Figure 17. However, the REFH and REFL OUT buffers were designed to only drive light loads on the order of 5−10mA. Driving capacitive loads is not recommended with these buffers. In addition, the REFH and REFL buffers must not be allowed to saturate from sourcing/sinking too much current from REFH OUT or REFL OUT. Saturation of the REFH and REFL buffers results in errors in the voltages of OUT1−18 and V_{COM} OUT1−2. The BUF01900, which is anticipated to be released in Q1 '06, can be used to provide a programmable V_{COM} output.

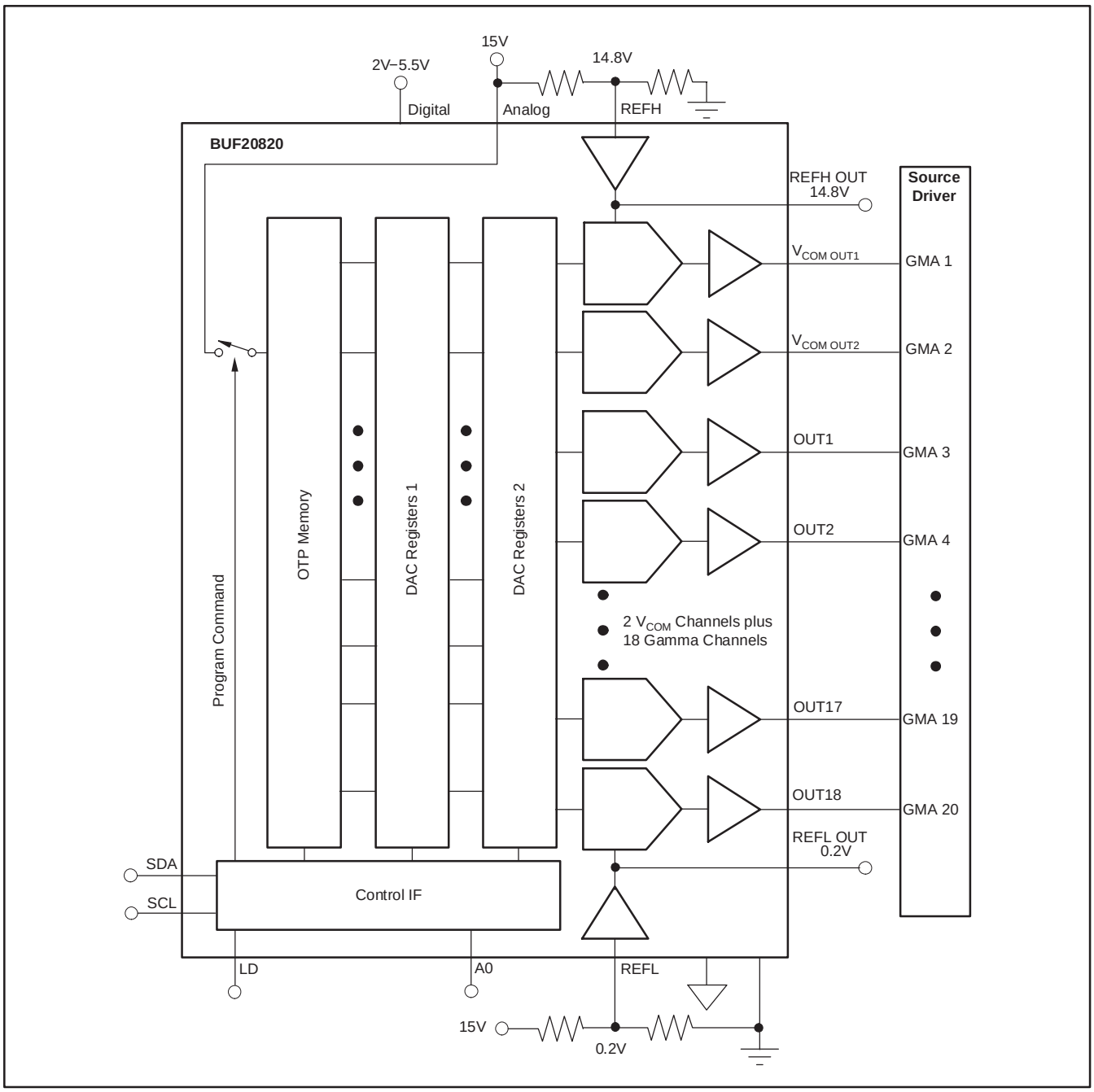


Figure 16. 20-Gamma Channel Solution—2 V_{COM} Channels Used as Additional Gamma Channels

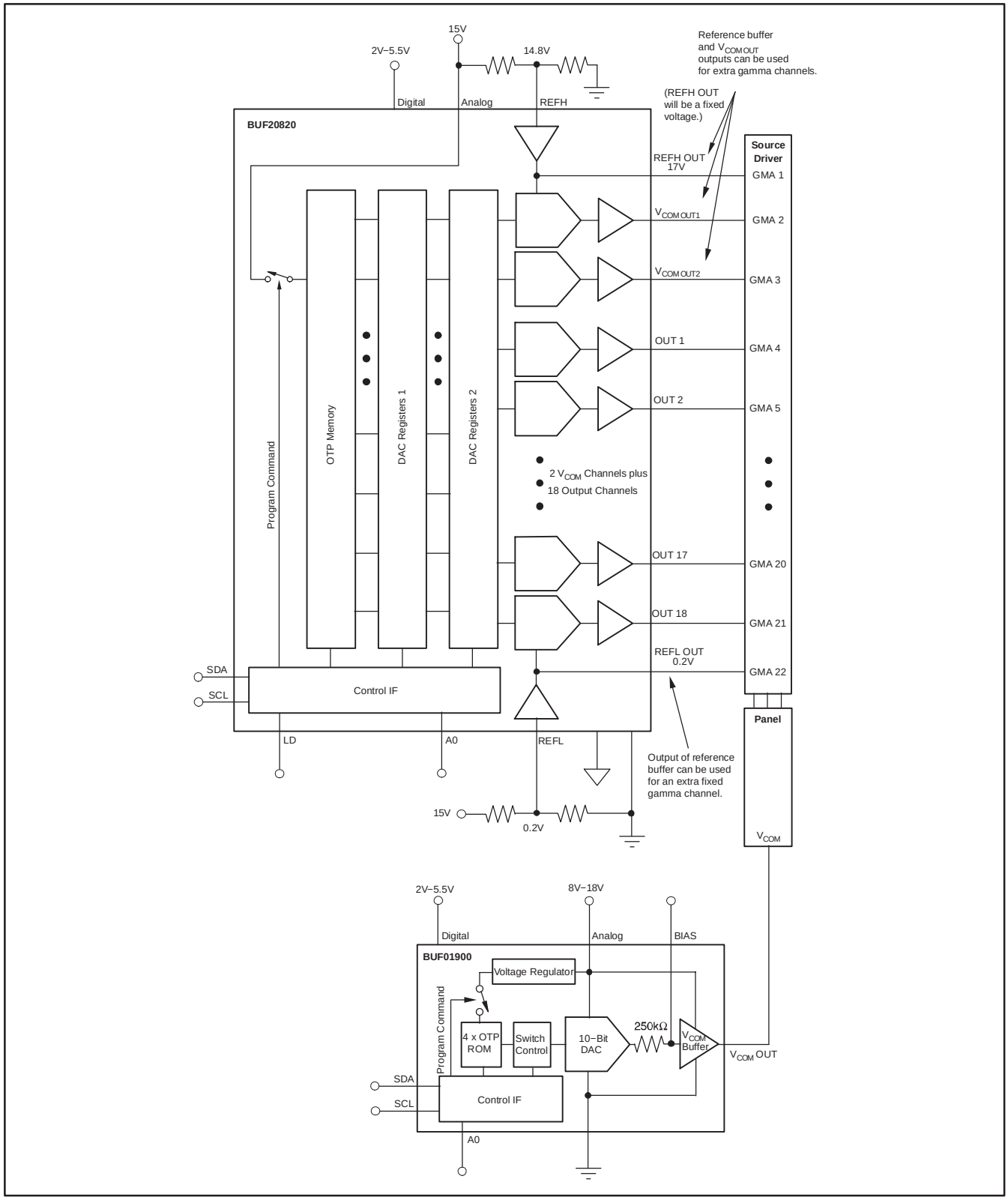


Figure 17. 22-Gamma Channel Solution

DYNAMIC GAMMA CONTROL

Dynamic gamma control is a technique used to improve the picture quality in LCD TV applications. The brightness in each picture frame is analyzed and the gamma curves are adjusted on a frame-by-frame basis. The gamma curves are typically updated during the short vertical blanking period in the video signal. Figure 18 shows a block diagram using the BUF20820 for dynamic gamma control and V_{COM} output.

The BUF20820 is ideally suited for rapidly changing the gamma curves because of its unique topology:

- double register input structure to the DAC;
- fast serial interface;
- simultaneous updating of all DACs by software. See the *Read/Write Operations* to write to all registers and the *Output Latch* sections.

The double register input structure saves programming time by allowing updated DAC values to be pre-loaded into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data is only stored into the first register bank, the DAC output values remain unchanged—the display is unaffected. During the vertical sync period, the DAC outputs (and therefore, the gamma voltages) can be quickly updated either by using an additional control line connected to the LD pin, or through software—writing a '1' in bit 15 of any DAC register. For the details on the operation of the double register input structure, see the *Output Latch* section.

Example: Update all 18 gamma registers simultaneously via software.

Step 1: Check if LD pin is placed in HIGH state.

Step 2: Write DAC Registers 1−18 with bit 15 always '0'.

Step 3: Write any DAC register a second time with identical data. Make sure that bit 15 is '1'. All DAC channels will be updated simultaneously after receiving the last bit of data. (Note: this step may be eliminated by setting bit 15 of DAC 18 to '1' in the previous step.)

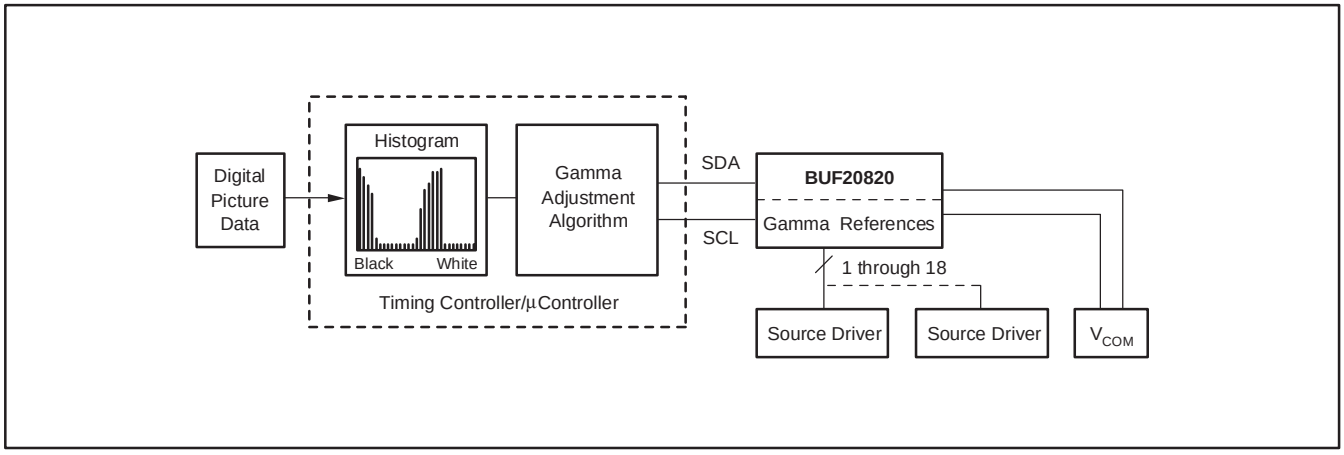


Figure 18. Dynamic Gamma Control

TOTAL TI PANEL SOLUTION

In addition to the BUF20820 programmable voltage reference, TI offers a complete set of ICs for the LCD panel market, including gamma correction buffers, various power-supply solutions, and audio power solutions. See Figure 19 for the total IC solution from TI.

THE BUF20820 IN INDUSTRIAL APPLICATIONS

The wide supply range, high output current, and very low cost make the BUF20820 attractive for a range of medium accuracy industrial applications such as programmable power supplies, multi-channel data acquisition systems, data-loggers, sensor excitation and linearization, power-supply generation, and others. Each DAC channel features 1LSB DNL and INL.

Many systems require different levels of biasing and power supply for various components as well as sensor excitation, control-loop set-points, voltage outputs, current outputs, and other functions. The BUF20820, with its 20 total programmable DAC channels, provides great flexibility to the entire system by allowing the designer to change all these parameters via software.

Figure 20 provides various ideas on how the BUF20820 can be used in applications. A micro-controller with two-wire serial interface controls the various DACs of the BUF20820. The BUF20820 can be used for:

- sensor excitation
- programmable bias/reference voltages
- variable power-supplies
- high-current voltage output
- 4-20mA output
- set-point generators for control loops.

NOTE: At power-up, the output voltages of the BUF20820 DACs are configured to the programmed OTP memory values, or $(V_{REFH} - V_{REFL})/2$ if the OTP values have not been programmed.

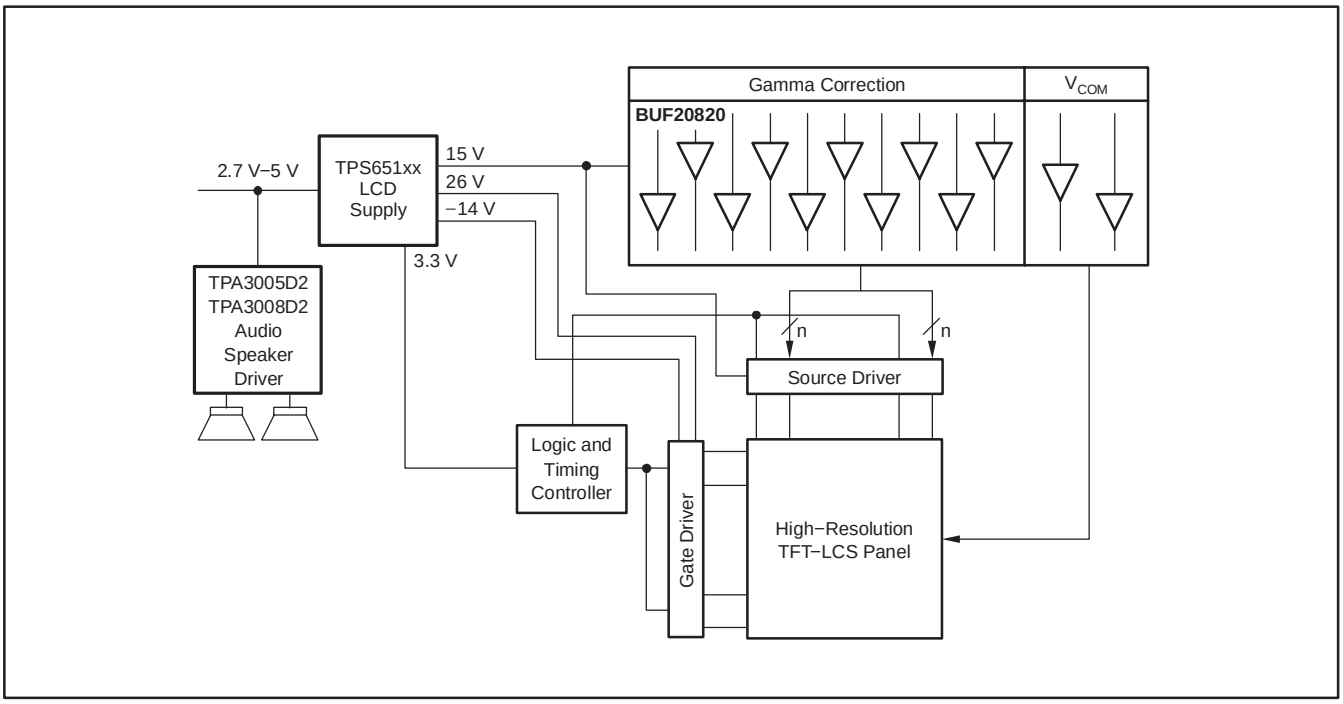


Figure 19. TI LCD Solution

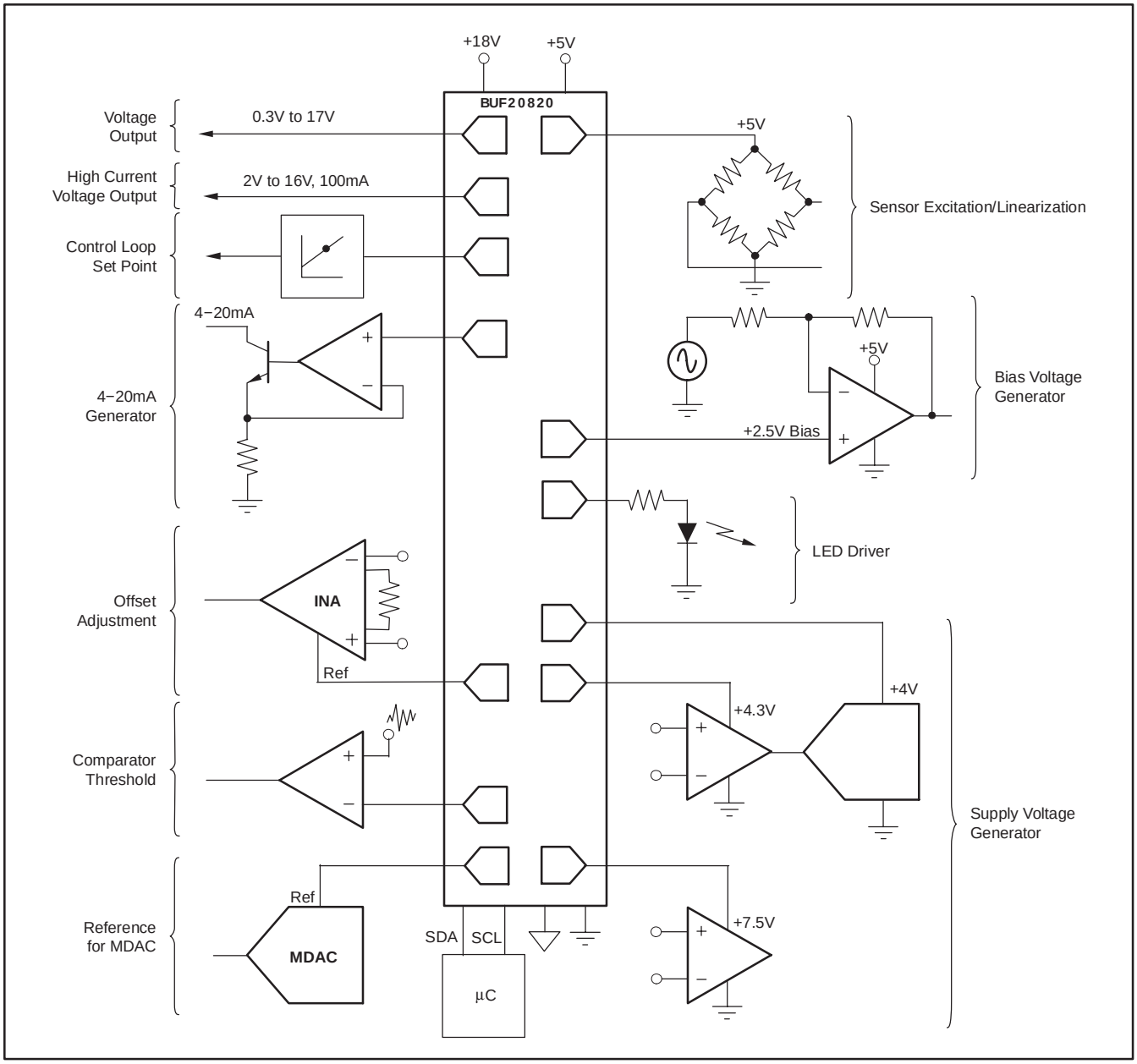


Figure 20. Industrial Applications for the BUF20820

EVALUATION BOARD AND SOFTWARE

An evaluation board is available for the BUF20820, as shown in Figure 21. The evaluation board features easy-to-use software that allows individual channel voltages to be set. Configurations can be quickly evaluated to determine optimal codes for a given application. Contact your local TI representative for more information regarding the evaluation board.

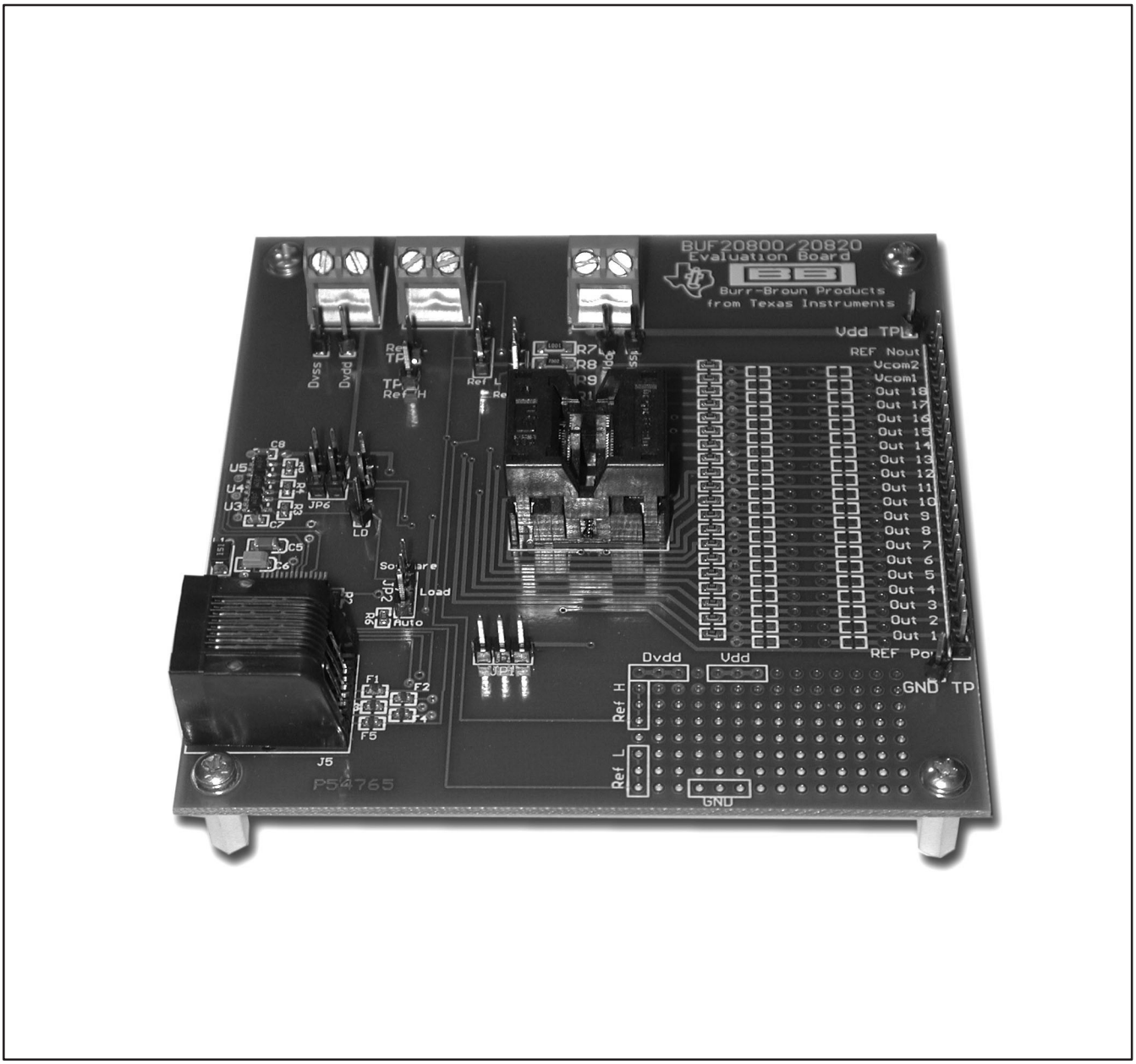


Figure 21. BUF208x0 Evaluation Board

GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF20820 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted, as shown in Figure 22(a) and Figure 22(b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 22(c). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. **Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation.** This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device, GND_A and GND_D.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns (2x5) for the HTSSOP-38 DCP package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUF20820 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.
5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF20820 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its eight holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUF20820 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

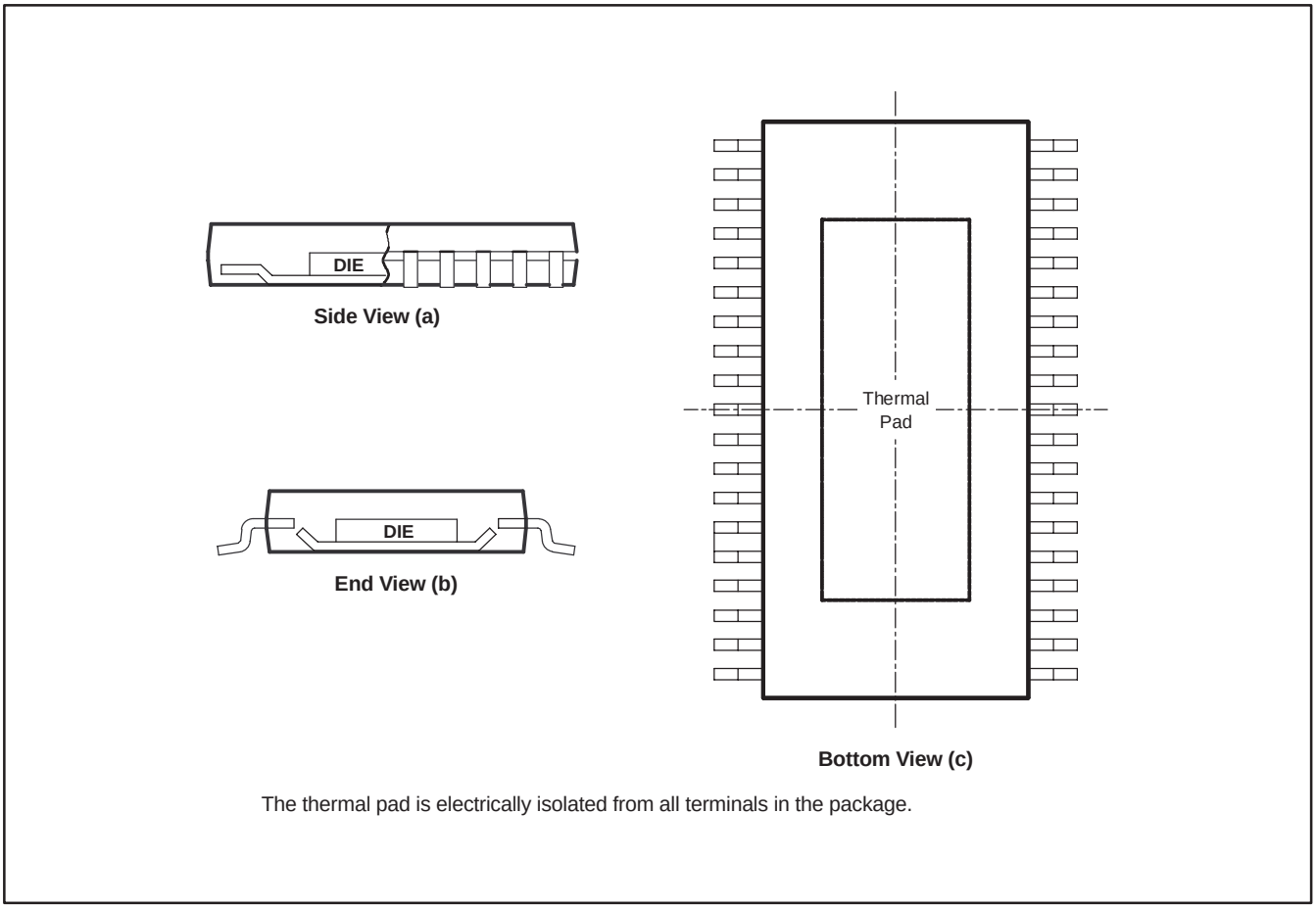


Figure 22. Views of Thermally-Enhanced DCP Package

For a given θ_{JA}, the maximum power dissipation is shown in Figure 23, and is calculated by Equation 3:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right) \quad (3)$$

Where:

P_D = maximum power dissipation (W)

T_{MAX} = absolute maximum junction temperature (125°C)

T_A = free-ambient air temperature (°C)

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = thermal coefficient from junction-to-case (°C/W)

θ_{CA} = thermal coefficient from case-to-ambient air (°C/W)

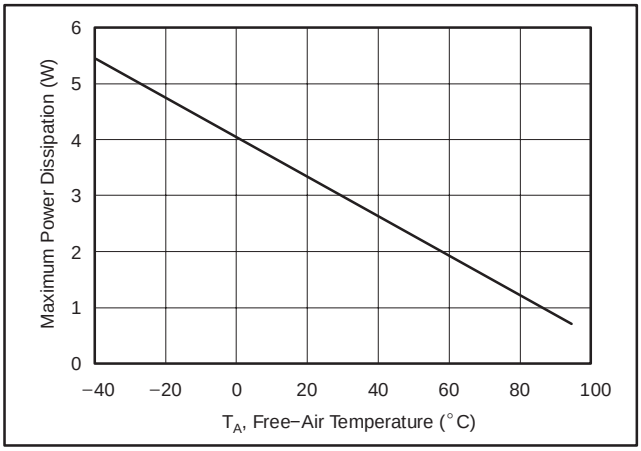


Figure 23. Maximum Power Dissipation vs Free-Air Temperature (with PowerPAD soldered down)

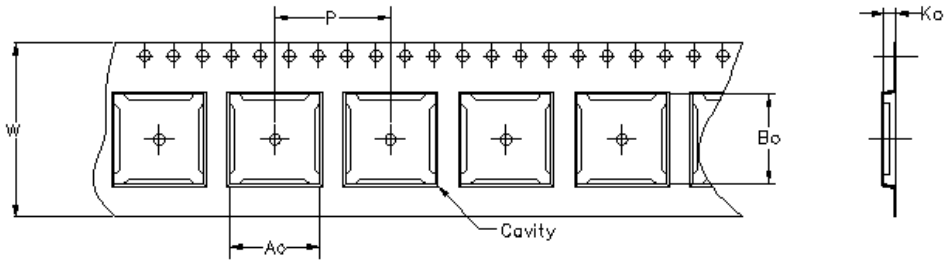
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BUF20820AIDCPR	ACTIVE	HTSSOP	DCP	38	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR
BUF20820AIDCPRE4	ACTIVE	HTSSOP	DCP	38	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

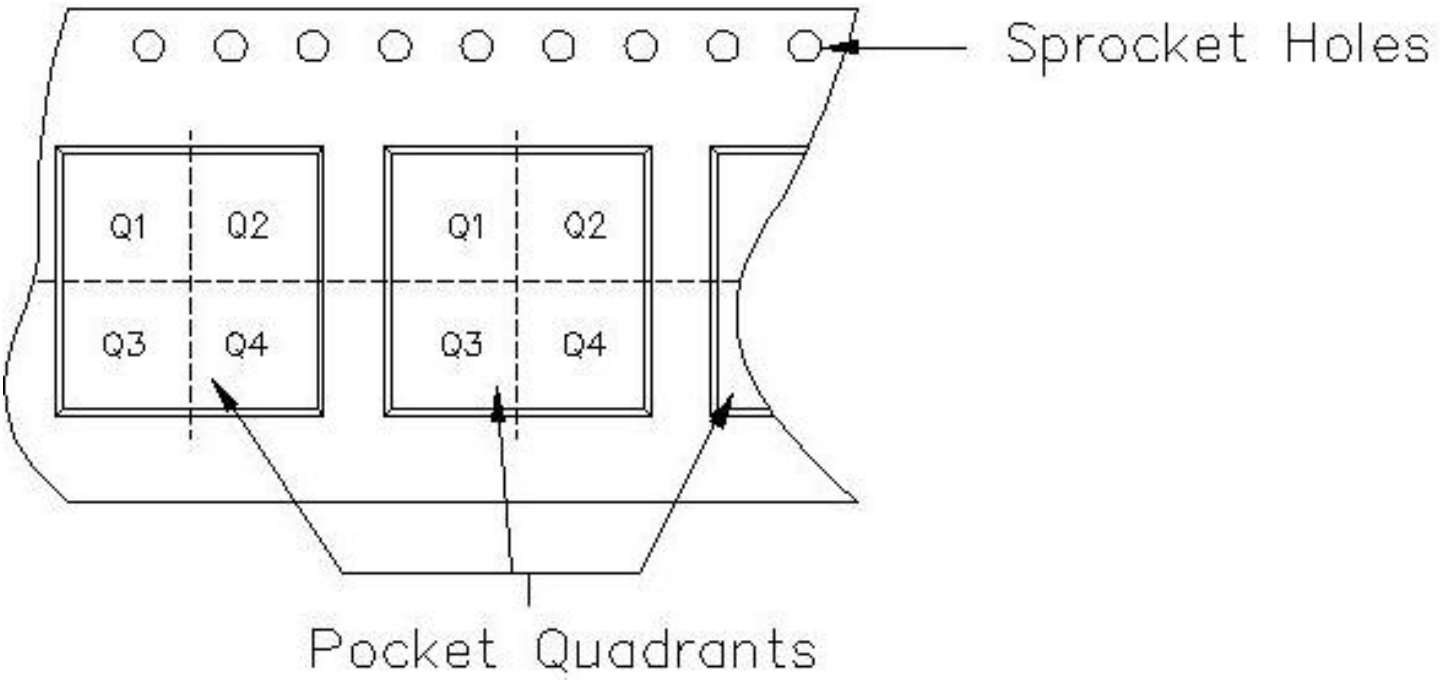
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



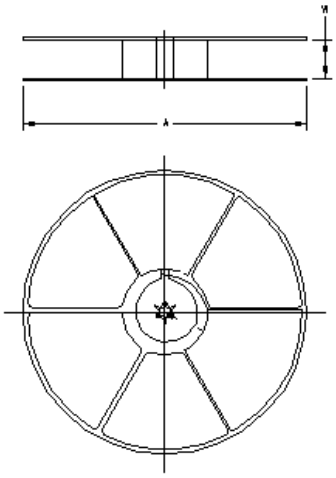
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



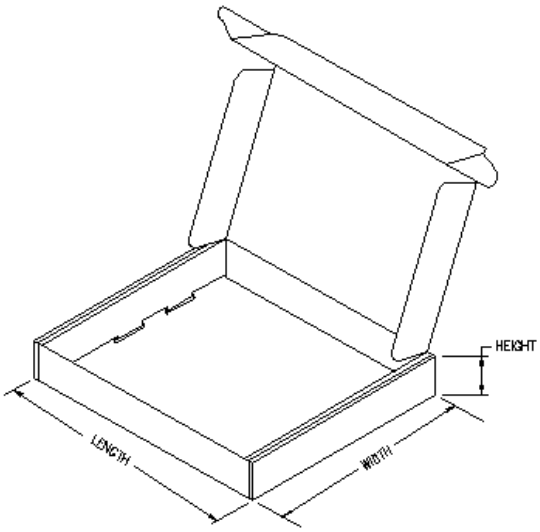
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF20820AIDCPR	DCP	38	TAI	330	16	6.9	10.2	1.8	12	16	PKGORNT1TR-MSP



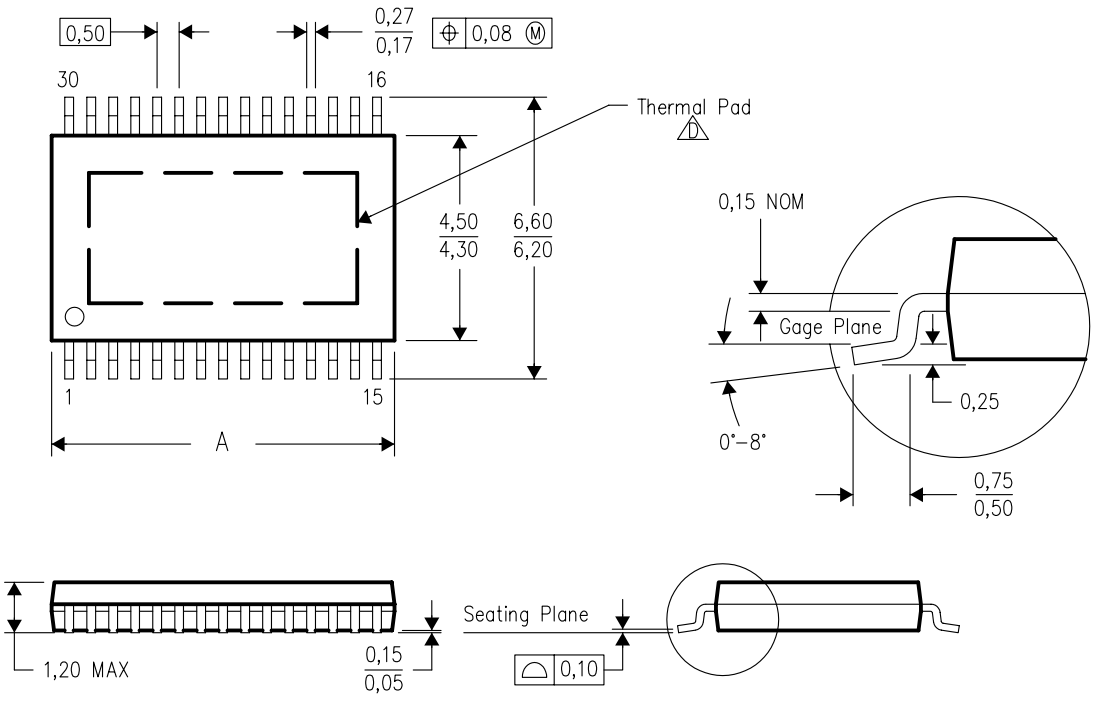
TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
BUF20820AIDCPR	DCP	38	TAI	346.0	346.0	33.0



DCP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

30 PIN SHOWN



DIM \ PINS **	28	30	38	44	50
A MAX	7,90	7,90	9,80	11,40	12,60
A MIN	7,70	7,70	9,60	11,20	12,40

4073267/C 03/05

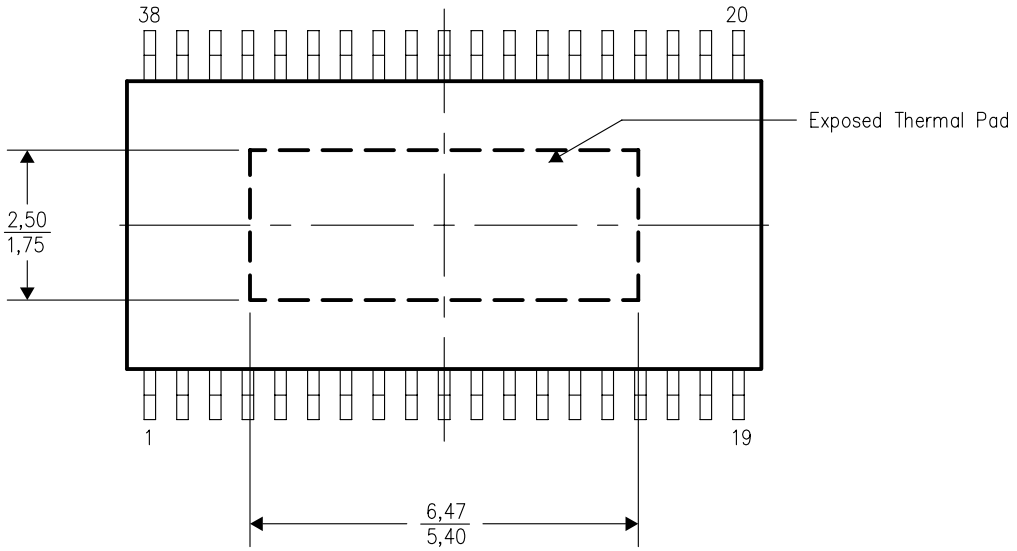
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protusions, mold flash not to exceed 0.15mm.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–153

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

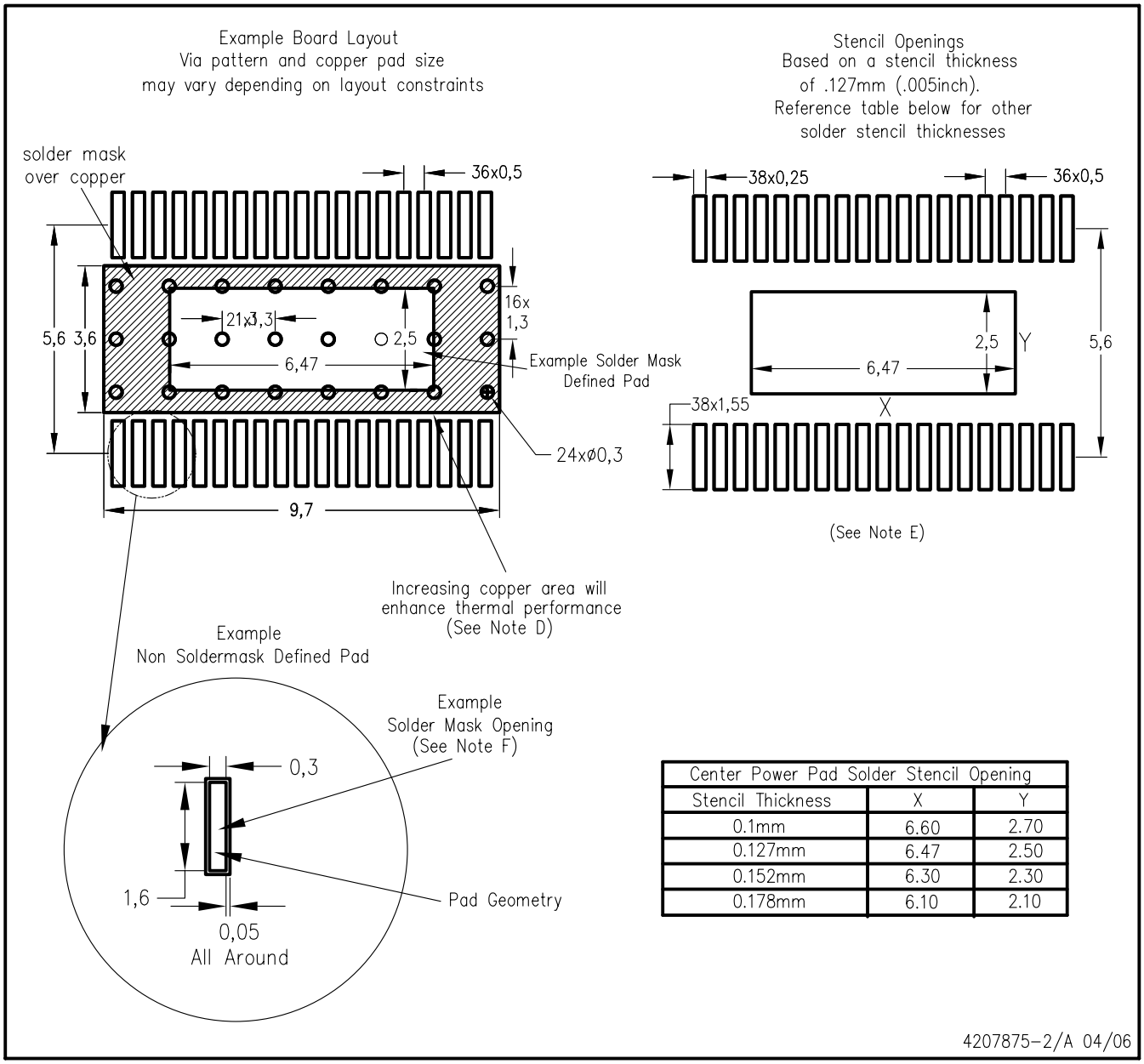


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DCP (R–PDSO–G38) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.60	2.70
0.127mm	6.47	2.50
0.152mm	6.30	2.30
0.178mm	6.10	2.10

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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